Ultra-Low Power, 12-Bit, 1-MSPS, SAR ADC

1 FEATURES

- **Ultra-Low-Power SAR ADC:**
  - **243 µW at 1 MSPS with 1.8-V AVDD**
  - **720 µW at 1 MSPS with 3-V AVDD**
  - **78 µW at 100 kSPS with 3-V AVDD**
  - **Less than 1 µW at 1 kSPS with 3-V AVDD**
- **1-MSPS Throughput with Zero Data Latency**
- **Wide Operating Range:**
  - **AVDD: 1.65 V to 3.6 V**
  - **DVDD: 1.65 V to 3.6 V (Independent of AVDD)**
  - **Temperature Range: –40°C to 125°C**
- **Excellent Performance:**
  - **12-Bit Resolution with NMC**
  - **68 dB SNR with 3-V AVDD (Typical)**
  - **–79 dB THD with 3-V AVDD (Typical)**
- **Unipolar Input Range: 0 V to AVDD**
- **Integrated Offset Calibration**
- **SPI ™-Compatible Serial Interface: 16 MHz**
- **JESD8-7A Compliant Digital I/O**

2 APPLICATIONS

- **Low-Power Data Acquisition**
- **Battery-Powered Handheld Equipment**
- **Level Sensors**
- **Ultrasonic Flow Meters**
- **Motor Control**
- **Wearable Fitness**
- **Portable Medical Equipment**
- **Hard Drives**
- **Glucose Meters**

3 DESCRIPTIONS

The RS1461LP is a 12-bit, 1-MSPS, analog-to-digital converter (ADC). The device supports a wide analog input voltage range (1.65 V to 3.6 V) and includes a capacitor-based, successive-approximation register (SAR) ADC with an inherent sample-and-hold circuit. The SPI-compatible serial interface is controlled by the $\overline{CS}$ and SCLK signals. The input signal is sampled with the $\overline{CS}$ falling edge and SCLK is used for conversion and serial data output. The device supports a wide digital supply range (1.65 V to 3.6 V), enabling direct interface to a variety of host controllers. The RS1461LP complies with the JESD8-7A standard for a normal DVDD range (1.65 V to 1.95 V).

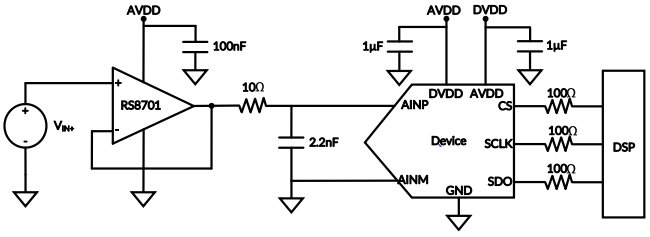
The RS1461LP is available in the VSSOP8 package and is specified for operation from –40°C to 125°C. Miniature form-factor and extremely low-power consumption make this device suitable for space-constrained, battery-powered applications.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS1461LP	VSSOP8	2.30 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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4 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version

VERSION	Change Date	Change Item
A.0	2026/08/07	Preliminary version completed

5 PACKAGE/ORDERING INFORMATION (1)

Orderable Device	Package Type	Op Temp(°C)	Device Marking (2)	MSL (3)	Package Qty
RS1461LPXVS8	VSSOP8	-40°C ~+125°C	1461	MSL1	Tape and Reel, 3000

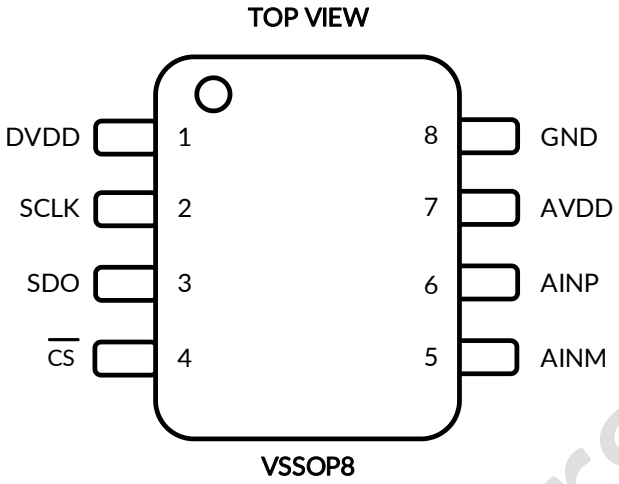
NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

6 PIN CONFIGURATION AND FUNCTIONS



Pin Description

NAME	PIN	TYPE	DESCRIPTION
DVDD	1	Supply	Digital I/O supply voltage
SCLK	2	Digital input	Serial clock
SDO	3	Digital output	Serial data out
$\overline{CS}$	4	Digital input	Chip-select signal, active low
AINM	5	Analog input	Analog signal input, negative
AINP	6	Analog input	Analog signal input, positive
AVDD	7	Supply	Analog power-supply input, also provides the reference voltage to the ADC
GND	8	Supply	Ground for power supply, all analog and digital signals are referred to this pin

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
AVDD to GND		-0.3	3.9	V
DVDD to GND		-0.3	3.9	V
AINP to GND		-0.3	AVDD + 0.3	V
AINM to GND		-0.3	0.3	V
Digital input voltage to GND		-0.3	DVDD + 0.3	V
Package thermal impedance (2), θ_{JA}	VSSOP8		205	°C/W
Storage temperature, T_{stg}		-60	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The package thermal impedance is calculated in accordance with JESD-51.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-Device Model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
AVDD	Analog supply voltage range	1.65	3.6	V
DVDD	Digital supply voltage range	1.65	3.6	V
T_A	Operating free-air temperature	-40	125	°C

7.4 Electrical Characteristics

At T_A = –40°C to 125°C, AVDD = 3 V, DVDD = 1.65 V to 3.6 V, f_{SAMPLE} = 1 MSPS, and V_{AINM} = 0 V, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
ANALOG INPUT							
	Full-scale input voltage span (1)			0		AVDD	V
	Absolute input voltage range		AINP to GND	-0.1		AVDD+0.1	V
			AINM to GND	-0.1		0.1	V
C_S	Sampling capacitance				15		pF
SYSTEM PERFORMANCE							
	Resolution				12		Bits
NMC	No missing codes			12			Bits
INL	Integral nonlinearity		AVDD = 3 V		±1.2		LSB (2)
			AVDD = 1.8 V		±1.8		
DNL	Differential nonlinearity		AVDD = 3 V		-0.9/1.1		LSB
			AVDD = 1.8 V		-0.98/1.2		
E_O	Offset error	Uncalibrated	AVDD = 1.65 V to 3.6 V		±12		LSB
		Calibrated (3)	AVDD = 3V		±1		
			AVDD = 1.8 V		±2		
dV_{OS}/dT	Offset error drift with temperature				±3		ppm/°C
E_G	Gain error		AVDD = 3 V		±0.1		%FS
			AVDD = 1.8 V		±0.05		
	Gain error drift with temperature				±3		ppm/°C
SAMPLING DYNAMICS							
t_{ACQ}	Acquisition time			200			ns
	Maximum throughput rate		16-MHz SCLK, AVDD = 1.65 V to 3.6 V			1	MHz
DYNAMIC CHARACTERISTICS							
SNR	Signal-to-noise ratio (4)		f_{IN} = 2 kHz, AVDD = 3 V		68		dB
			f_{IN} = 2 kHz, AVDD = 1.8 V		66		dB
THD	Total harmonic distortion(4)(5)		f_{IN} = 2 kHz, AVDD = 3 V		-79		dB
SINAD	Signal-to-noise and distortion (4)		f_{IN} = 2 kHz, AVDD = 3 V		67.5		dB
			f_{IN} = 2 kHz, AVDD = 1.8 V		65.5		dB
SFDR	Spurious-free dynamic range (4)		f_{IN} = 2 kHz, AVDD = 3 V		80		dB

(1) Ideal input span; does not include gain or offset error.
(2) LSB means least significant bit.
(3) Refer to the Offset Calibration section for more details.
(4) All specifications expressed in decibels (dB) refer to the full-scale input (FSR) and are tested with an input signal 0.5 dB below full-scale, unless otherwise specified.
(5) Calculated on the first nine harmonics of the input frequency.

Electrical Characteristics (continued)

At T_A =–40°C to 125°C, AVDD = 3 V, DVDD = 1.65 V to 3.6 V, f_{SAMPLE} = 1 MSPS, and V_{AINM} = 0 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
DIGITAL INPUT/OUTPUT (CMOS Logic Family)						
V_{IH}	High-level input voltage (6)	–40°C ≤ T_A ≤ 125°C	0.65 DVDD		DVDD+0.3	V
V_{IL}	Low-level input voltage (6)	–40°C ≤ T_A ≤ 125°C	-0.3		0.35 DVDD	V
V_{OH}	High-level output voltage (6)	At I_{SOURCE} = 500 µA	0.8 DVDD		DVDD	V
		At I_{SOURCE} = 2 mA	DVDD-0.45		DVDD	
V_{OL}	Low-level output voltage (6)	At I_{SINK} = 500 µA	0		0.2 DVDD	V
		At I_{SINK} = 2 mA	0		0.45	
POWER-SUPPLY REQUIREMENTS						
AVDD	Analog supply voltage		1.65	3	3.6	V
DVDD	Digital I/O supply voltage		1.65	3	3.6	V
I_{AVDD}	Analog supply current	At 1 MSPS with AVDD = 3 V		240		µA
		At 100 kSPS with AVDD = 3 V		26		
		At 1 MSPS with AVDD = 1.8 V		135		µA
P_D	Power dissipation	At 1 MSPS with AVDD = 3 V		720		µW
		At 100 kSPS with AVDD = 3 V		78		µW
		At 1 MSPS with AVDD = 1.8 V		243		

(6) Digital voltage levels comply with the JESD8-7A standard for DVDD from 1.65 V to 1.95 V. See the Digital Voltage Levels section for more details.

7.5 Timing Characteristics

All specifications are at T_A = −40°C to 125°C, AVDD = 1.65 V to 3.6 V, DVDD = 1.65 V to 3.6 V, and C_{LOAD} on SDO = 20 pF, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIMING SPECIFICATIONS					
$f_{THROUGHPU}$	Throughput			1	MSPS
t_{CYCLE}	Cycle time	1			µs
t_{CONV}	Conversion time		12.5 × t_{SCLK} + t_{SU_CSCK}		ns
t_{DV_CSDO}	Delay time: $\overline{CS}$ falling to data enable		10		ns
t_{D_CKDO}	Delay time: SCLK falling to (next) data valid on DOUT, AVDD = 1.8 V to 3.6 V		30		ns
	Delay time: SCLK falling to (next) data valid on DOUT, AVDD = 1.65 V to 1.8 V		20		ns
t_{DZ_CSDO}	Delay time: $\overline{CS}$ rising to DOUT going to 3-state		25		ns
TIMING REQUIREMENTS					
t_{ACQ}	Acquisition time	200			ns
f_{SCLK}	SCLK frequency	0.016		16	MHz
t_{SCLK}	SCLK period	62.5			ns
t_{PH_CK}	SCLK high time	0.45		0.55	t_{SCLK}
t_{PL_CK}	SCLK low time	0.45		0.55	t_{SCLK}
t_{PH_CS}	$\overline{CS}$ high time		30		ns
t_{SU_CSCK}	Setup time: $\overline{CS}$ falling to SCLK falling		10		ns
t_{D_CKCS}	Delay time: last SCLK falling to CS rising		15		ns

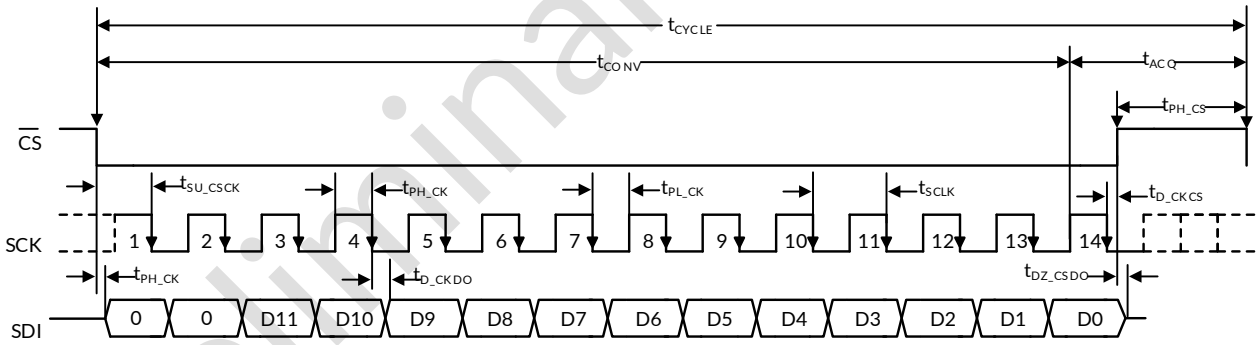


Figure 1. Timing Diagram

7.6 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.
At T_A = 25°C, AVDD = 3 V, DVDD = 1.8 V, and f_{SAMPLE} = 1 MSPS, unless otherwise noted.

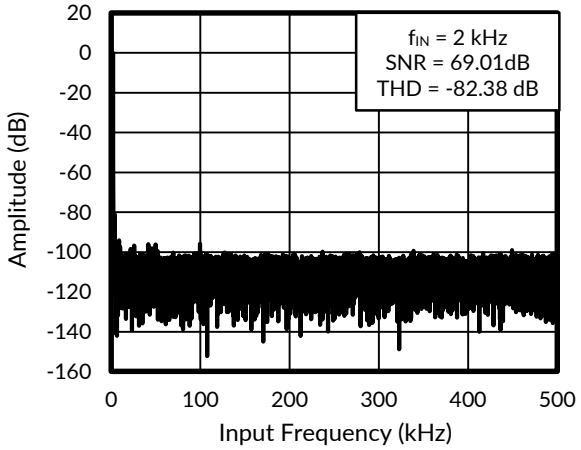


Figure 2. Typical FFT

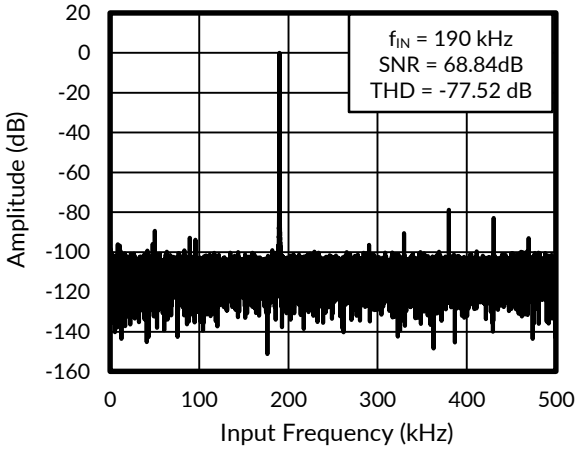


Figure 3. Typical FFT

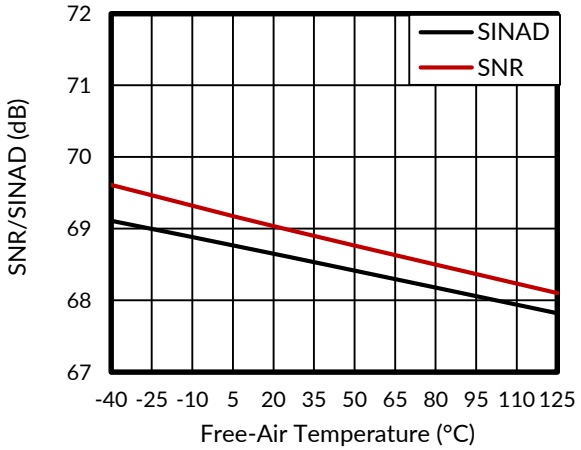


Figure 4. SNR and SINAD vs Temperature

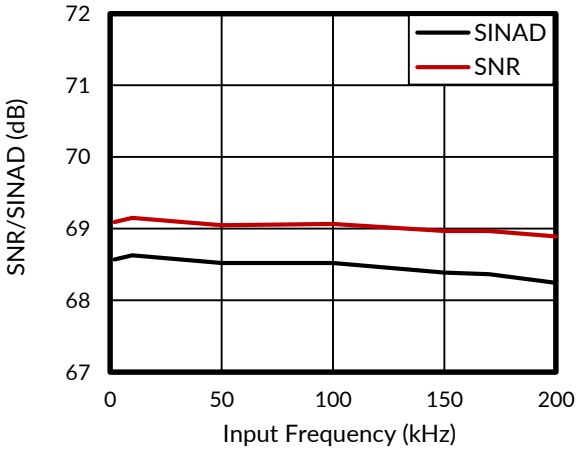


Figure 5. SNR and SINAD vs Input Frequency

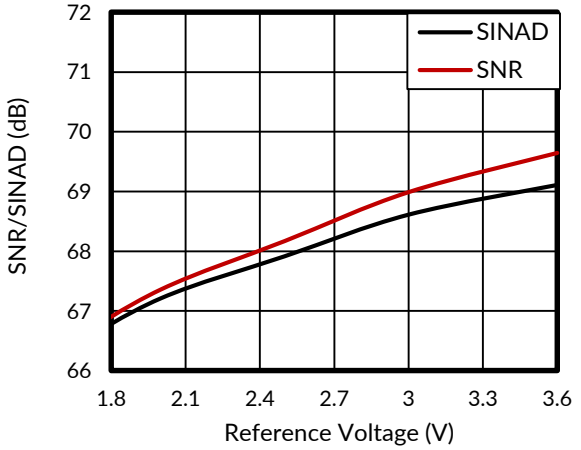


Figure 6. SNR and SINAD vs Reference Voltage (AVDD)

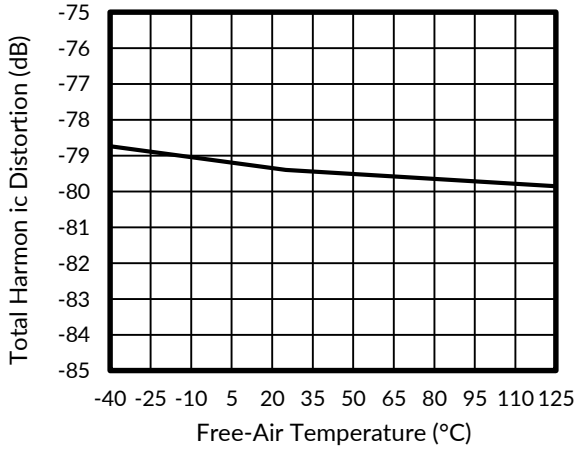


Figure 7. THD vs Free-Air Temperature

Typical Characteristics (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A = 25°C, AVDD = 3 V, DVDD = 1.8 V, and f_{SAMPLE} = 1 MSPS, unless otherwise noted.

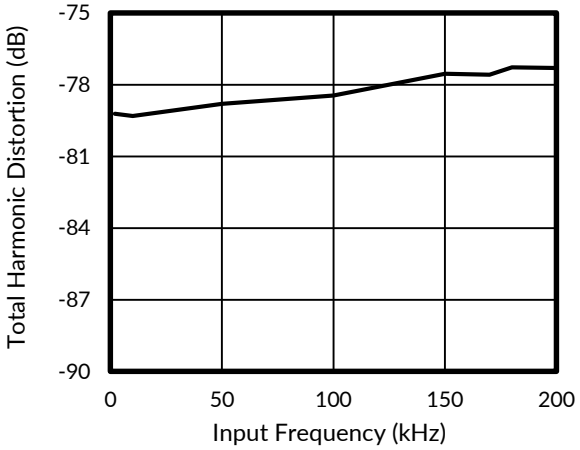


Figure 8. THD vs Input Frequency

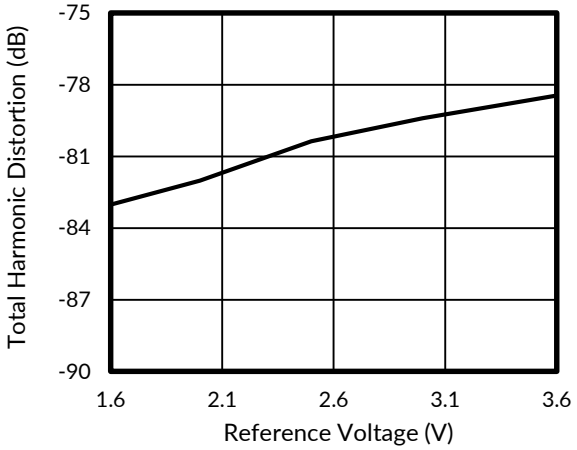


Figure 9. THD vs Reference Voltage (AVDD)

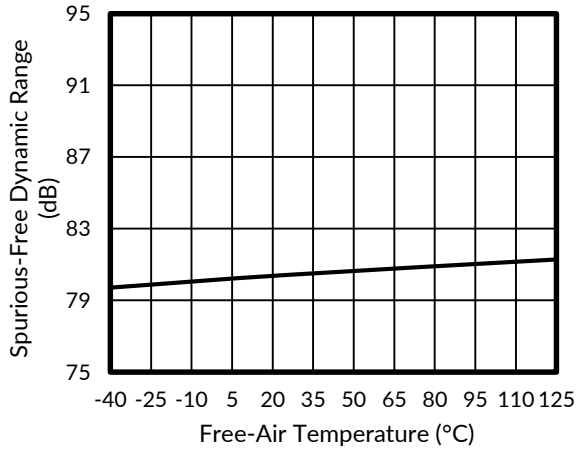


Figure 10. SFDR vs Free-Air Temperature

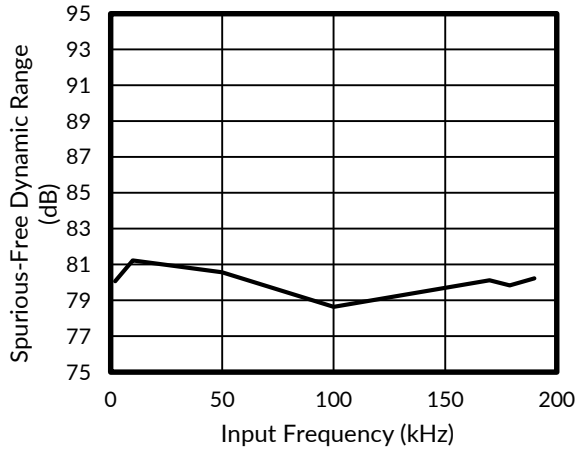


Figure 11. SFDR vs Input Frequency

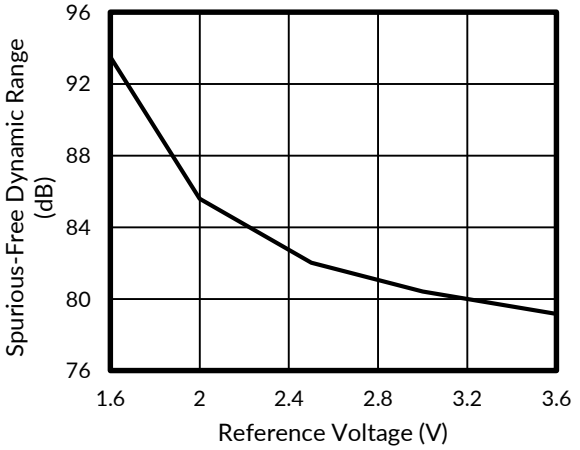


Figure 12. SFDR vs Reference Voltage (AVDD)

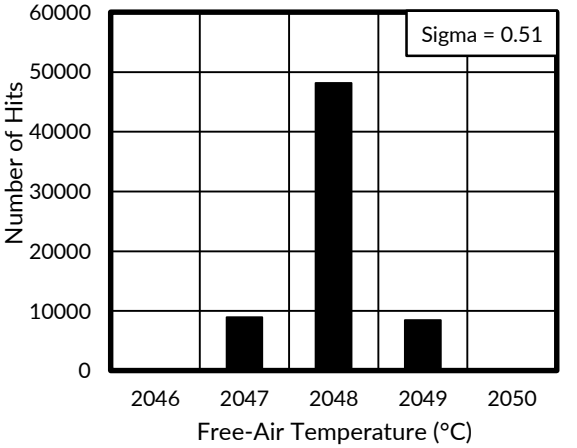


Figure 13. DC Input Histogram

Typical Characteristics (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A = 25°C, AVDD = 3 V, DVDD = 1.8 V, and f_{SAMPLE} = 1 MSPS, unless otherwise noted.

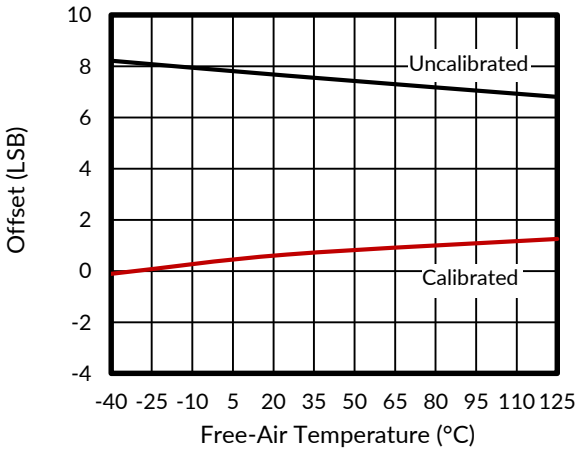


Figure 14. Offset vs Free-Air Temperature

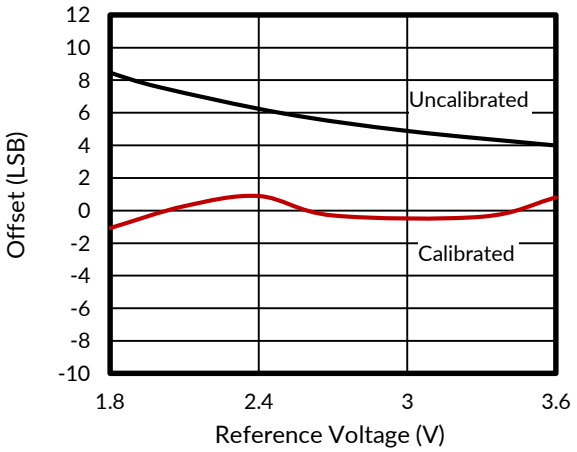


Figure 15. Offset vs Reference Voltage (AVDD)

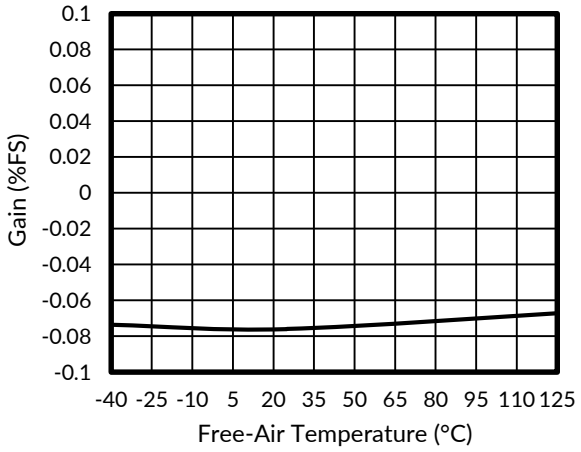


Figure 16. Gain Error vs Free-Air Temperature

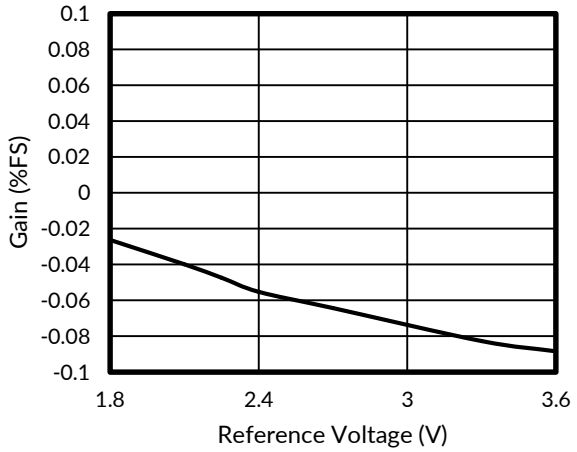


Figure 17. Gain Error vs Reference Voltage (AVDD)

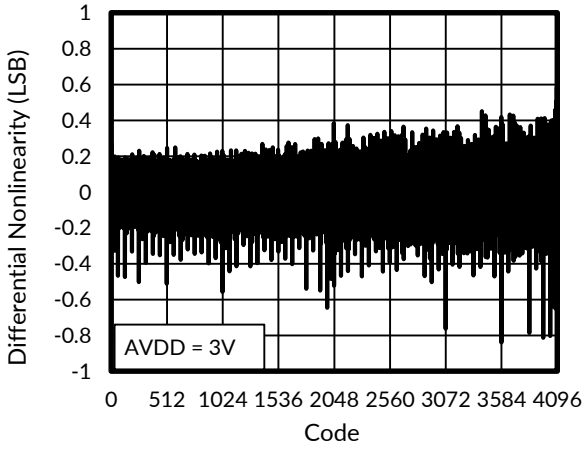


Figure 18. Typical DNL

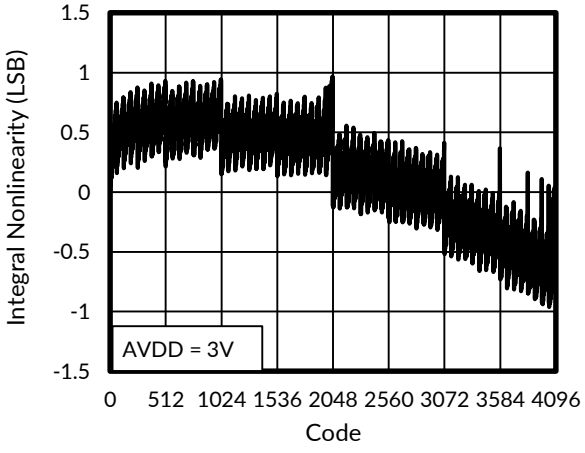


Figure 19. Typical INL

Typical Characteristics (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A = 25°C, AVDD = 3 V, DVDD = 1.8 V, and f_{SAMPLE} = 1 MSPS, unless otherwise noted.

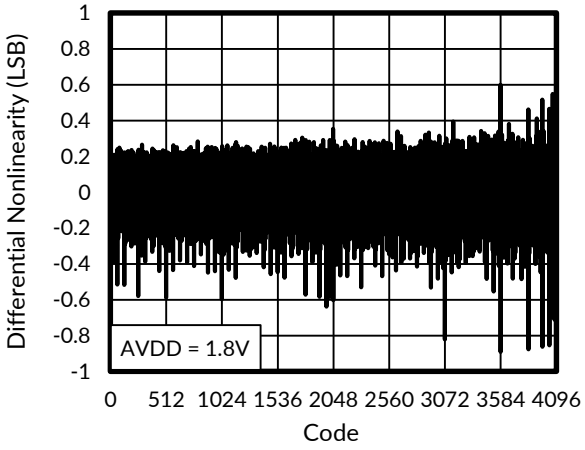


Figure 20. Typical DNL

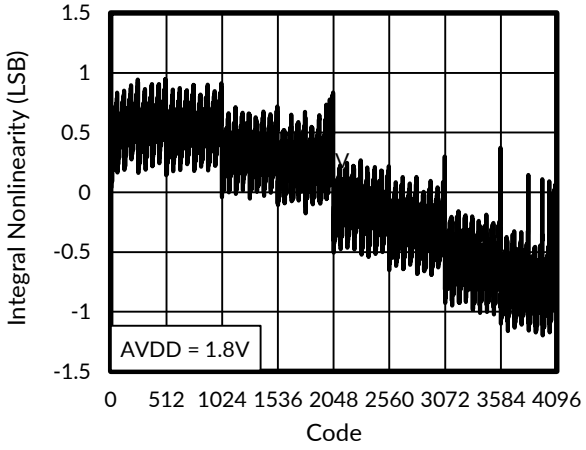


Figure 21. Typical INL

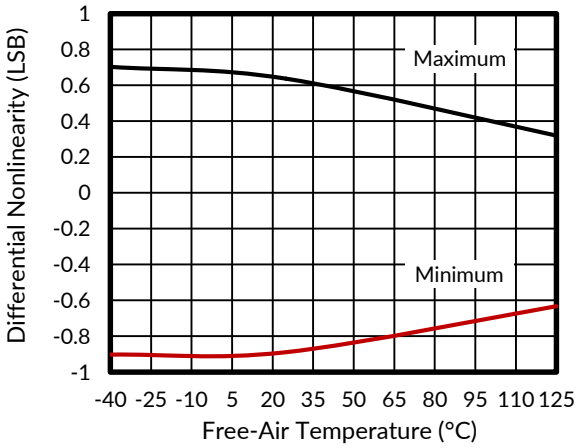


Figure 22. DNL vs Free-Air-Temperature

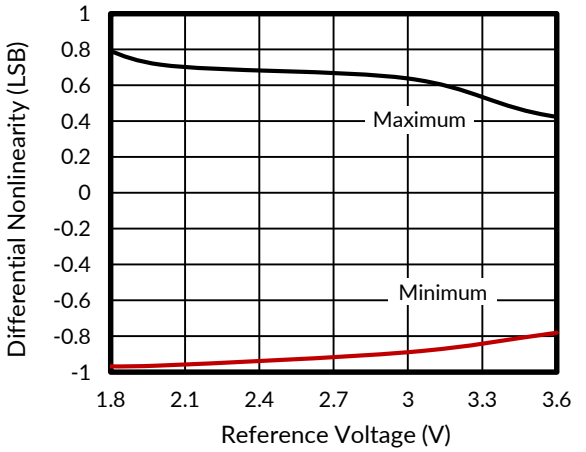


Figure 23. DNL vs Reference Voltage (AVDD)

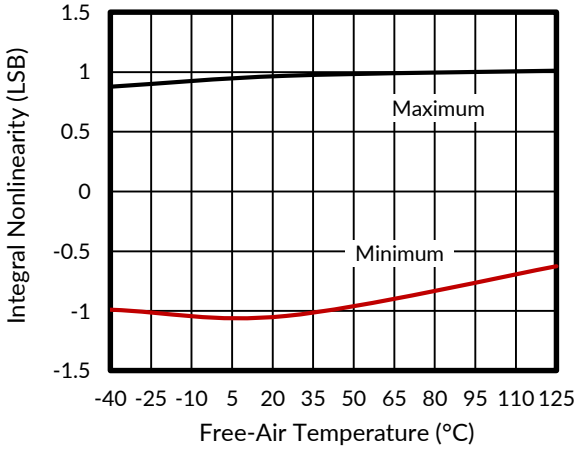


Figure 24. INL vs Free-Air-Temperature

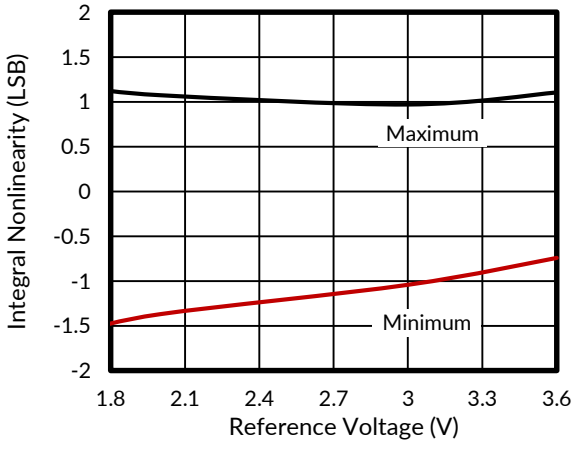


Figure 25. INL vs Reference Voltage (AVDD)

Typical Characteristics (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A = 25°C, AVDD = 3 V, DVDD = 1.8 V, and f_{SAMPLE} = 1 MSPS, unless otherwise noted.

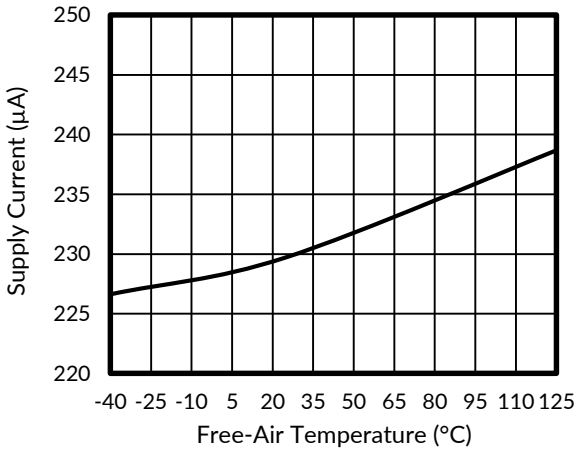


Figure 26. AVDD Supply Current vs Free-Air Temperature

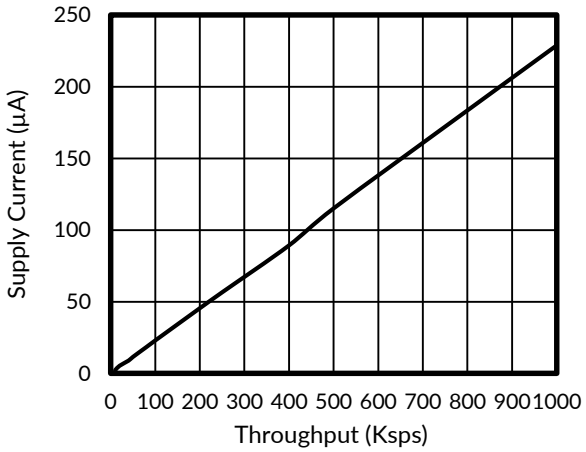


Figure 27. AVDD Supply Current vs Throughput

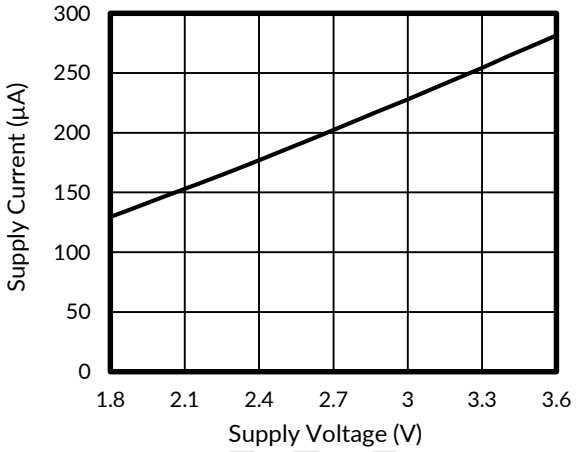


Figure 28. AVDD Supply Current vs AVDD Voltage

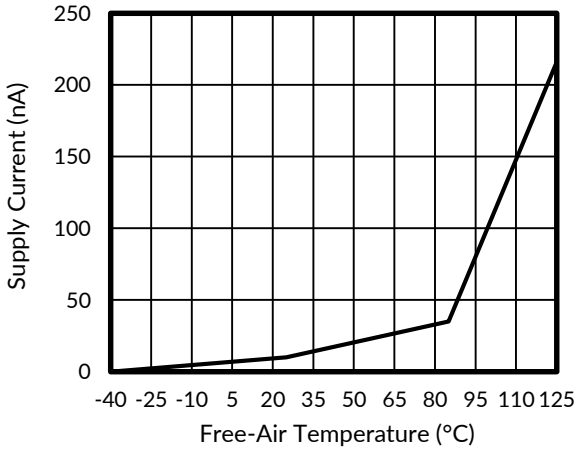


Figure 29. AVDD Static Current vs Free-Air Temperature

8 PARAMETER MEASUREMENT INFORMATION

8.1 Digital Voltage Levels

The device complies with the JESD8-7A standard for DVDD from 1.65 V to 1.95 V. Figure 30 shows voltage levels for the digital input and output pins.

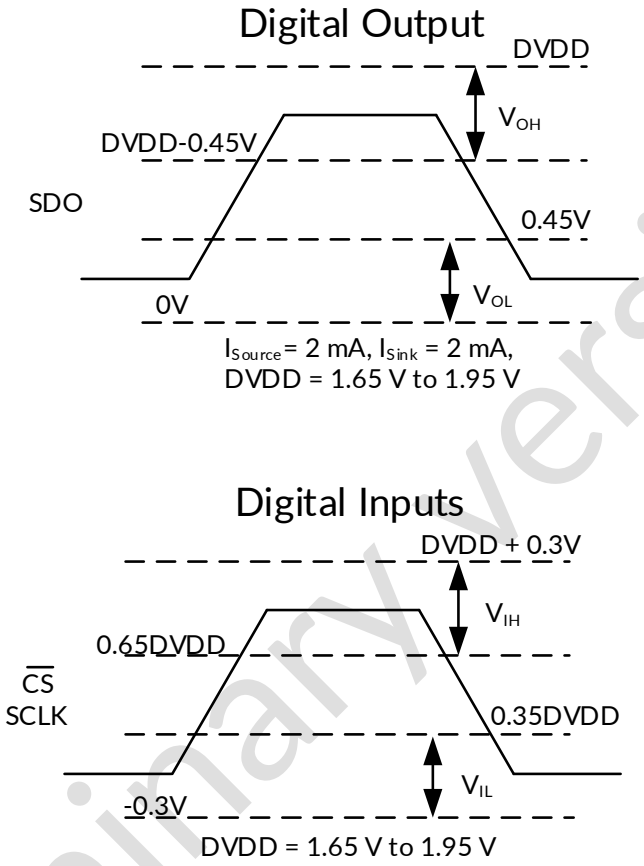


Figure 30. Digital Voltage Levels as per the JESD8-7A Standard

9 DETAILED DESCRIPTION

9.1 Overview

The RS1461LP is an ultralow-power, ultra-small analog-to-digital converter (ADC) that supports a wide analog input range. The analog input range for the device is defined by the AVDD supply voltage. The device samples the input voltage across the AINP and AINM pins on the $\overline{CS}$ falling edge and starts the conversion. The clock provided on the SCLK pin is used for conversion and data transfer. During conversions, both the AINP and AINM pins are disconnected from the sampling circuit. After the conversion completes, the sampling capacitors are reconnected across the AINP and AINM pins and the RS1461LP enters acquisition phase.

The device has an internal offset calibration. The offset calibration can be initiated by the user either on power-up or during normal operation; see the Offset Calibration section for more details.

The device also provides a simple serial interface to the host controller and operates over a wide range of digital power supplies. The RS1461LP requires only a 16-MHz SCLK for supporting a throughput of 1 MSPS. The digital interface also complies with the JESD8-7A (normal range) standard. The Functional Block Diagram section provides a block diagram of the device.

9.2 Functional Block Diagram

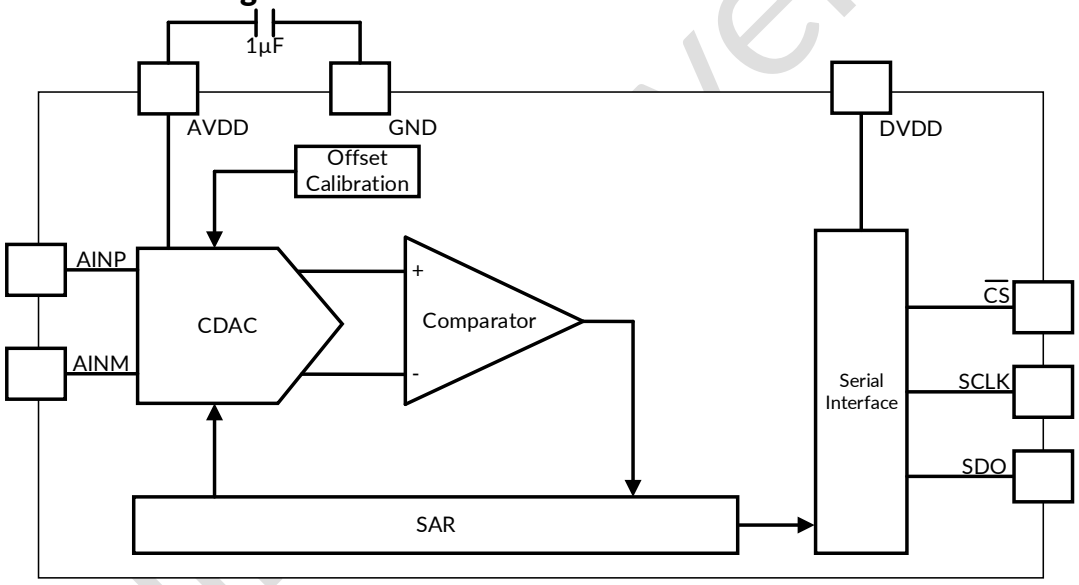


Figure 31. Reference for the Device

9.3 Feature Description

9.3.1 Reference

The device uses the analog supply voltage (AVDD) as a reference, as shown in Figure 31. RS recommends decoupling the AVDD pin with a 1-µF, low equivalent series resistance (ESR) ceramic capacitor. The minimum capacitor value required for AVDD is 200 nF. The AVDD pin functions as a switched capacitor load to the source powering AVDD. The decoupling capacitor provides the instantaneous charge required by the internal circuit and helps in maintaining a stable dc voltage on the AVDD pin. RS recommends powering the AVDD pin with a low output impedance and low-noise regulator.

9.3.2 Analog Input

The device supports single-ended analog inputs. The ADC samples the difference between AINP and AINM and converts for this voltage. The device is capable of accepting a signal from −100 mV to 100 mV on the AINM input and is useful in systems where the sensor or signal-conditioning block is far from the ADC. In such a scenario, there can be a difference between the ground potential of the sensor or signal conditioner and the ADC ground. In such cases, use separate wires to connect the ground of the sensor or signal conditioner to the AINM pin. The AINP input is capable of accepting signals from 0 V to AVDD. Figure 32 represents the equivalent analog input circuits for the sampling stage. The device has a low-pass filter followed by the sampling switch and sampling capacitor. The sampling switch is represented by an Rs (typically 50 Ω) resistor in series with an ideal switch and Cs (typically 15 pF) is the sampling capacitor. The ESD diodes are connected from both analog inputs to AVDD and ground.

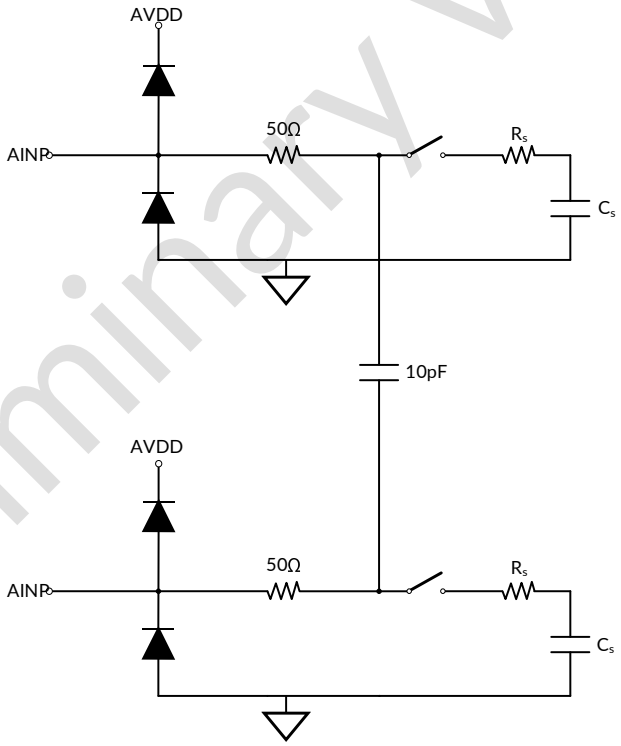


Figure 32. Equivalent Input Circuit for the Sampling Stage

The analog input full-scale range (FSR) is equal to the reference voltage of the ADC. The reference voltage for the device is equal to the analog supply voltage (AVDD). Thus, the device FSR can be determined by Equation 1:

$$FSR = V_{REF} = AVDD \quad (1)$$

9.3.3 ADC Transfer Function

The device output is in straight binary format. The device resolution for a single-ended input can be computed by Equation 2:

$1\ LSB = V_{REF} / 2^N$

where:

- V_{REF} = AVDD and
- N = 12 (2)

Figure 33 and Table 1 show the ideal transfer characteristics for the device.

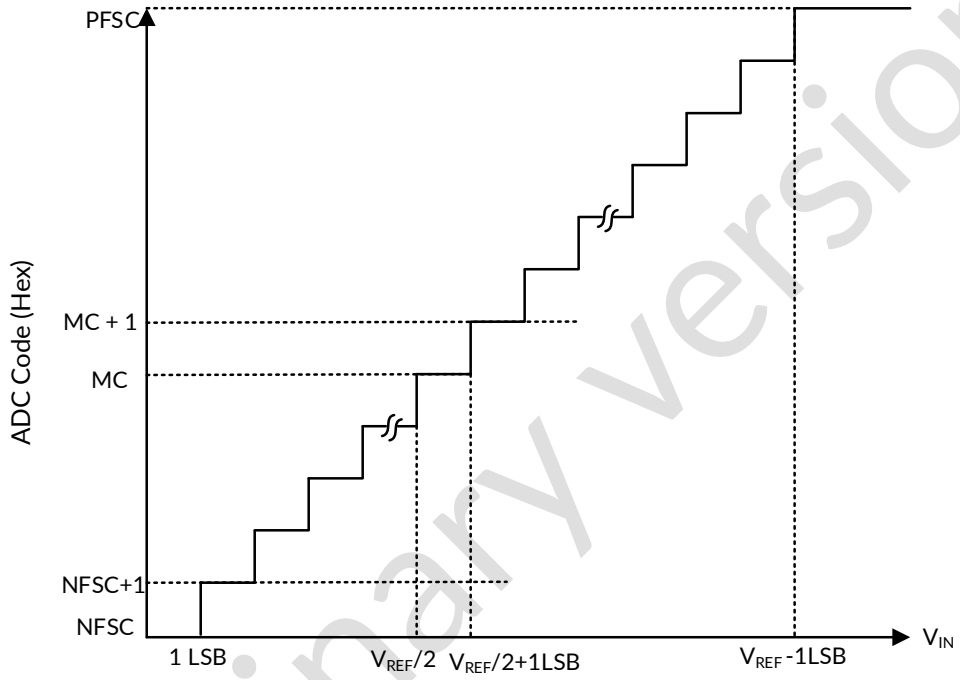


Figure 33. Ideal Transfer Characteristics

Table 1. Transfer Characteristics

INPUT VOLTAGE (AINP – AINM)	CODE	DESCRIPTION	IDEAL OUTPUT CODE
≤1 LSB	NFSC	Negative full-scale code	000
1 LSB to 2 LSBs	NFSC + 1	—	001
(V_{REF} / 2) to (V_{REF} / 2) + 1 LSB	MC	Mid code	800
(V_{REF} / 2) + 1 LSB to (V_{REF} / 2) + 2 LSBs	MC + 1	—	801
≥ V_{REF} – 1 LSB	PFSC	Positive full-scale code	FFF

9.3.4 Serial Interface

The device supports a simple, SPI-compatible interface to the external host. The $\overline{CS}$ signal defines one conversion and serial transfer frame. A frame starts with a $\overline{CS}$ falling edge and ends with a $\overline{CS}$ rising edge. The SDO pin outputs the ADC conversion results. Figure 34 shows a detailed timing diagram for the serial interface.

A minimum delay of t_{SU_CSCK} must elapse between the $\overline{CS}$ falling edge and the first SCLK falling edge. The device uses the clock provided on the SCLK pin for conversion and data transfer. The conversion result is available on the SDO pin with the first two bits set to 0, followed by 12 bits of the conversion result. The first zero is launched on the SDO pin on the $\overline{CS}$ falling edge. Subsequent bits (starting with another 0 followed by the conversion result) are launched on the SDO pin on subsequent SCLK falling edges. The SDO output remains low after 14 SCLKs. A $\overline{CS}$ rising edge ends the frame and brings the serial data bus to 3-state. For acquisition of the next sample, a minimum time of t_{ACQ} must be provided after the conversion of the current sample is completed. For details on timing specifications, see the Timing Characteristics table.

The device initiates an offset calibration on the first $\overline{CS}$ falling edge after power-up and the SDO output remains low during the first serial transfer frame after power-up. For further details, refer to the Offset Calibration section.

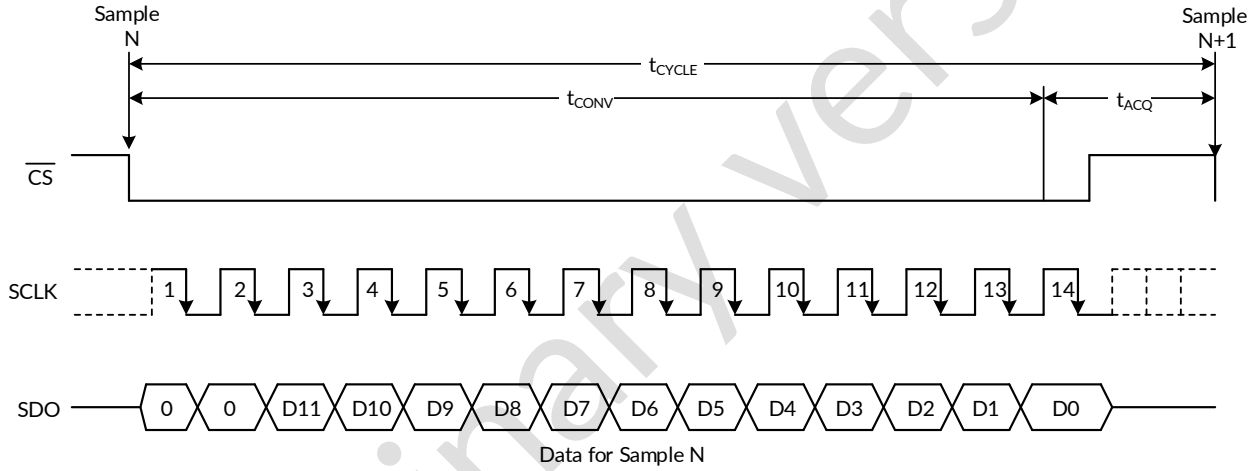
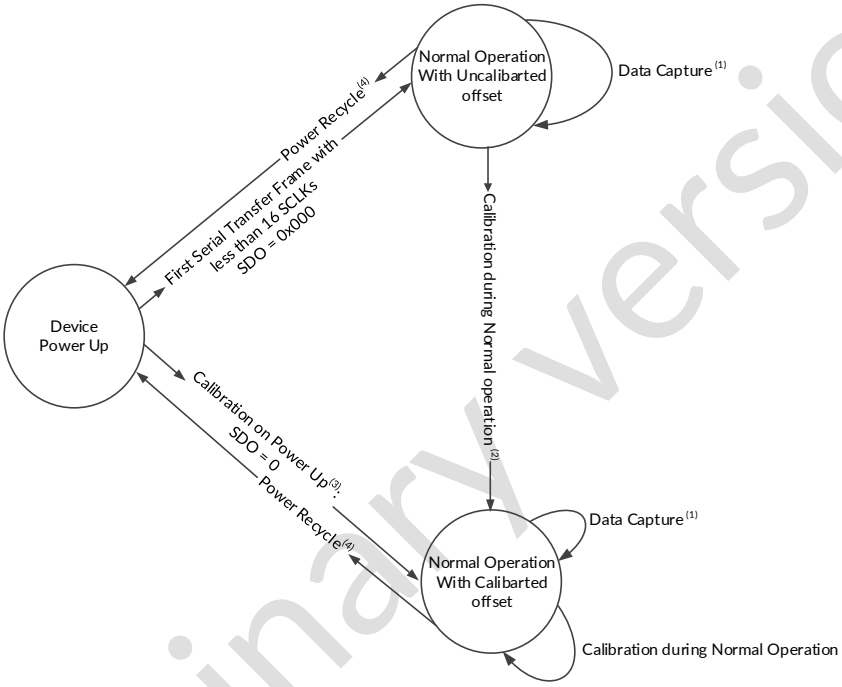


Figure 34. Serial Interface Timing Diagram

9.4 Device Functional Modes

9.4.1 Offset Calibration

The RS1461LP includes a feature to calibrate the device internal offset. During offset calibration, the analog input pins (AINP and AINM) are disconnected from the sampling stage. The device includes an internal offset calibration register (OCR) that stores the offset calibration result. The OCR is an internal register and cannot be accessed by the user through the serial interface. The OCR is reset to zero on power-up. Therefore, RS recommends calibrating the offset on power-up to bring the offset within the specified limits. If the operating temperature or analog supply voltage reflect a significant change, the offset can be recalibrated during normal operation. Figure 35 shows the offset calibration process.



(1) See the Timing Characteristics section for timing specifications.
(2) See the Offset Calibration During Normal Operation section for details.
(3) See the Offset Calibration on Power-Up section for details.
(4) The power recycle on the AVDD supply is required to reset the offset calibration and to bring the device to a power-up state.

Figure 35. Offset Calibration

9.4.1.1 Offset Calibration on Power-Up

The device initiates offset calibration on the first $\overline{CS}$ falling edge after power-up and calibration completes if the $\overline{CS}$ pin remains low for at least 16 SCLK falling edges after the first $\overline{CS}$ falling edge. The SDO output remains low during calibration. The minimum acquisition time must be provided after calibration for acquiring the first sample. If the device is not provided with at least 16 SCLKs during the first serial transfer frame after power-up, the OCR is not updated. Table 2 provides the timing parameters for offset calibration on power-up.

For subsequent samples, the device adjusts the conversion results with the value stored in the OCR. The conversion result adjusted with the value stored in OCR is provided by the device on the SDO output. Figure 36 shows the timing diagram for offset calibration on power-up.

Table 2. Offset Calibration on Power-Up

		MIN	TYP	MAX	UNIT
$f_{CLK-CAL}$	SCLK frequency for calibration for 2.25 V <AVDD < 3.6 V			16	MHz
$f_{CLK-CAL}$	SCLK frequency for calibration for 1.65 V < AVDD <2.25V			12	MHz
$t_{POWERUP-CAL}$	Calibration time at power-up	15 t_{SCLK}			ns
t_{ACQ}	Acquisition time	200			ns
t_{PH_CS}	$\overline{CS}$ high time	t_{ACQ}			ns
t_{SU_CSCK}	Setup time: $\overline{CS}$ falling to SCLK falling	15			ns
t_{D_CKCS}	Delay time: last SCLK falling to $\overline{CS}$ rising	10			ns

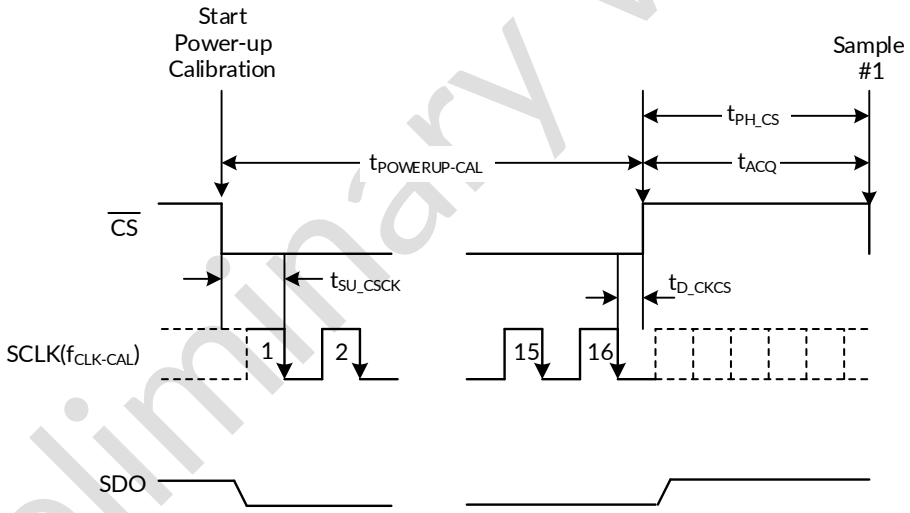


Figure 36. Offset Calibration on Power-Up Timing Diagram

9.4.1.2 Offset Calibration During Normal Operation

Offset calibration can be done during normal device operation if at least 32 SCLK falling edges are provided in one serial transfer frame. During the first 14 SCLKs, the device converts the sample acquired on the $\overline{CS}$ falling edge and provides data on the SDO output. The device initiates the offset calibration on the 17th SCLK falling edge and calibration completes on the 32nd SCLK falling edge. The SDO output remains low after the 14th SCLK falling edge and SDO goes to 3-state after $\overline{CS}$ goes high. If the device is provided with less than 32 SCLKs during a serial transfer frame, the OCR is not updated. Table 3 provides the timing parameters for offset calibration during normal operation.

For subsequent samples, the device adjusts the conversion results with the value stored in the OCR. The conversion result adjusted with the value stored in the OCR is provided by the device on the SDO output. Figure 37 shows the timing diagram for offset calibration during normal operation.

Table 3. Offset Calibration During Normal Operation

		MIN	TYP	MAX	UNIT
$f_{CLK-CAL}$	SCLK frequency for calibration for 2.25 V <AVDD < 3.6 V			16	MHz
$f_{CLK-CAL}$	SCLK frequency for calibration for 1.65 V < AVDD <2.25V			12	MHz
t_{CAL}	Calibration time during normal operation	15 t_{SCLK}			ns
t_{ACQ}	Acquisition time	200			ns
t_{PH_CS}	$\overline{CS}$ high time	t_{ACQ}			ns
t_{SU_CSCK}	Setup time: $\overline{CS}$ falling to SCLK falling	15			ns
t_{D_CKCS}	Delay time: last SCLK falling to $\overline{CS}$ rising	10			ns

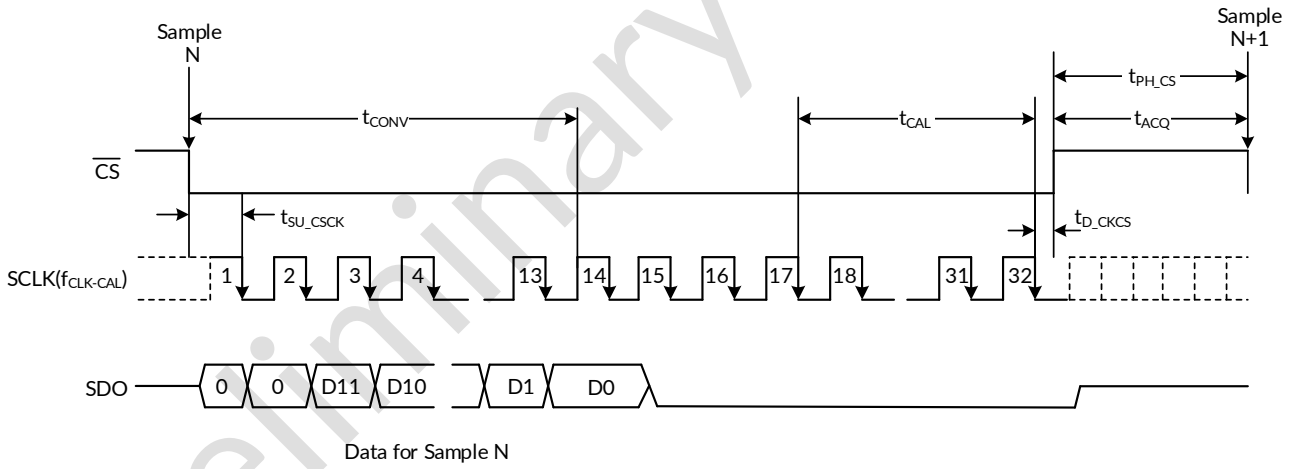


Figure 37. Offset Calibration During Normal Operation Timing Diagram

10 APPLICATION AND IMPLEMENTATION

A differential RC filter is placed at the analog inputs AINP and AINM of the device, consisting of a series resistor R_{FLT} and a shunt capacitor C_{FLT}. In the typical application circuit shown in Figure 38, a 10Ω resistor and a 2.2nF capacitor are used. This filter serves two critical functions. First, it acts as an anti-aliasing low-pass filter to limit the bandwidth of the input signal, attenuating high-frequency noise and preventing aliasing components from folding back into the passband during sampling. Second, the capacitor C_{FLT} acts as a charge bucket to supply the instantaneous charge required by the internal switched-capacitor sampling stage of the ADC. This ensures the input voltage settles accurately within the acquisition time window. The value of C_{FLT} is selected to be significantly larger than the internal sampling capacitance to minimize voltage kickback. The series resistor R_{FLT} isolates the operational amplifier from the capacitive load, ensuring amplifier stability while allowing sufficient bandwidth for fast signal settling.

Series resistors, typically 100Ω, are placed on the digital interface lines including Chip Select $\overline{CS}$, Serial Clock SCLK, and Serial Data Out SDO. These resistors act as source termination to dampen signal reflections and filter out digital overshoot caused by impedance mismatches or parasitic inductance on the PCB traces. The exact resistor values should be optimized based on the specific layout, conversion speed, and the rise and fall times of the digital signals to ensure signal integrity.

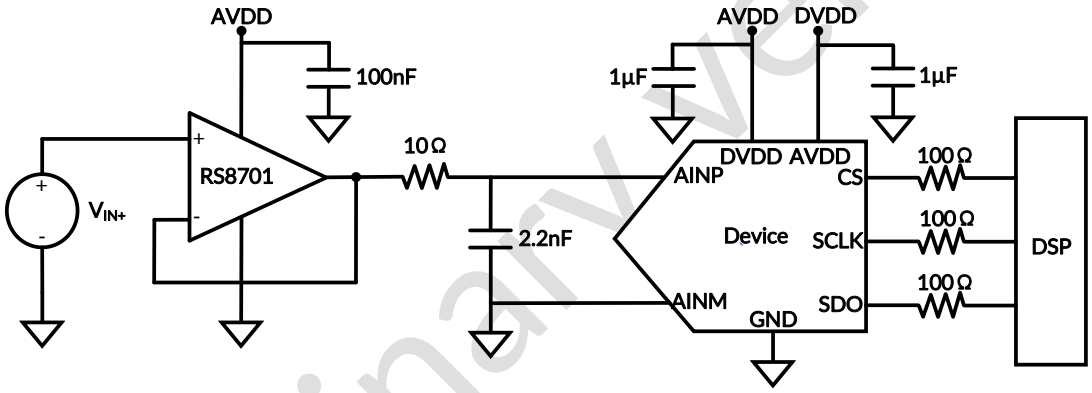


Figure 38. Typical Application Circuits

11 POWER SUPPLY RECOMMENDATIONS

11.1 AVDD and DVDD Supply Recommendations

The RS1461LP has two separate power supplies: AVDD and DVDD. The device operates on AVDD; DVDD is used for the interface circuits. AVDD and DVDD can be independently set to any value within the permissible ranges. The AVDD supply also defines the full-scale input range of the device. Always set the AVDD supply to be greater than or equal to the maximum input signal to avoid saturation of codes. Decouple the AVDD and DVDD pins individually with 1-µF ceramic decoupling capacitors, as shown in Figure 39. The minimum capacitor value required for AVDD and DVDD is 200 nF and 20 nF, respectively. If both supplies are powered from the same source, a minimum capacitor value of 220 nF is required for decoupling.

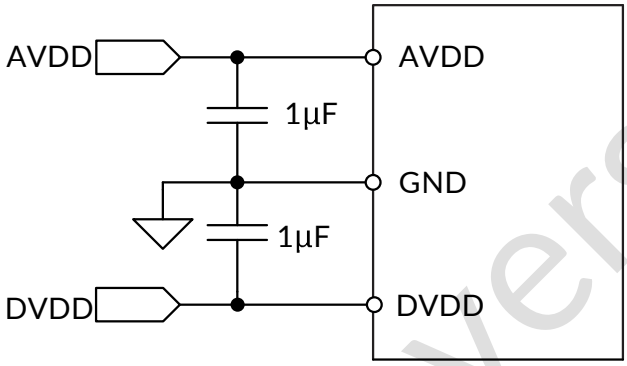


Figure 39 Power-Supply Decoupling

11.2 Estimating Digital Power Consumption

The current consumption from the DVDD supply depends on the DVDD voltage, load capacitance on the SDO line, and the output code. The load capacitance on the SDO line is charged by the current from the SDO pin on every rising edge of the data output and is discharged on every falling edge of the data output. The current consumed by the device from the DVDD supply can be calculated by Equation 3:

$I_{DVDD} = C \times V \times f$

where:

- C = Load capacitance on the SDO line,
- V = DVDD supply voltage, and
- f = Number of transitions on the SDO output. (3)

The number of transitions on the SDO output depends on the output code, and thus changes with the analog input. The maximum value of f occurs when data output on the SDO change on every SCLK. SDO changing on every SCLK results in an output code of AAAh or 555h. For an output code of AAAh or 555h at a 1-MSPS throughput, the frequency of transitions on the SDO output is 6MHz.

For the current consumption to remain at the lowest possible value, keep the DVDD supply at the lowest permissible value and keep the capacitance on the SDO line as low as possible.

11.3 Optimizing Power Consumed by the Device

- Keep the analog supply voltage (AVDD) as close as possible to the analog input voltage. Set AVDD to be greater than or equal to the analog input voltage of the device.
- Keep the digital supply voltage (DVDD) at the lowest permissible value.
- Reduce the load capacitance on the SDO output.
- Run the device at the optimum throughput. Power consumption reduces with throughput.

12 LAYOUT

12.1 Layout Guidelines

Figure 40 shows a board layout example for the RS1461LP. Use a ground plane underneath the device and partition the PCB into analog and digital sections. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources. In Figure 40, the analog inputs are routed on the left side of the device, while the digital connections are routed on the right side.

The power sources to the device must be clean and well-bypassed. Use 1-µF ceramic bypass capacitors in close proximity to the analog (AVDD) and digital (DVDD) power-supply pins. Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors. Connect all ground pins to the ground plane using short, low-impedance paths. The AVDD supply voltage for the RS1461LP also functions as a reference for the device. Place the decoupling capacitor (C_{REF}) for AVDD close to the device AVDD and GND pins and connect C_{REF} to the device pins with thick copper tracks, as shown in Figure 40.

The fly-wheel RC filters are placed close to the device. Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

12.2 Layout Example

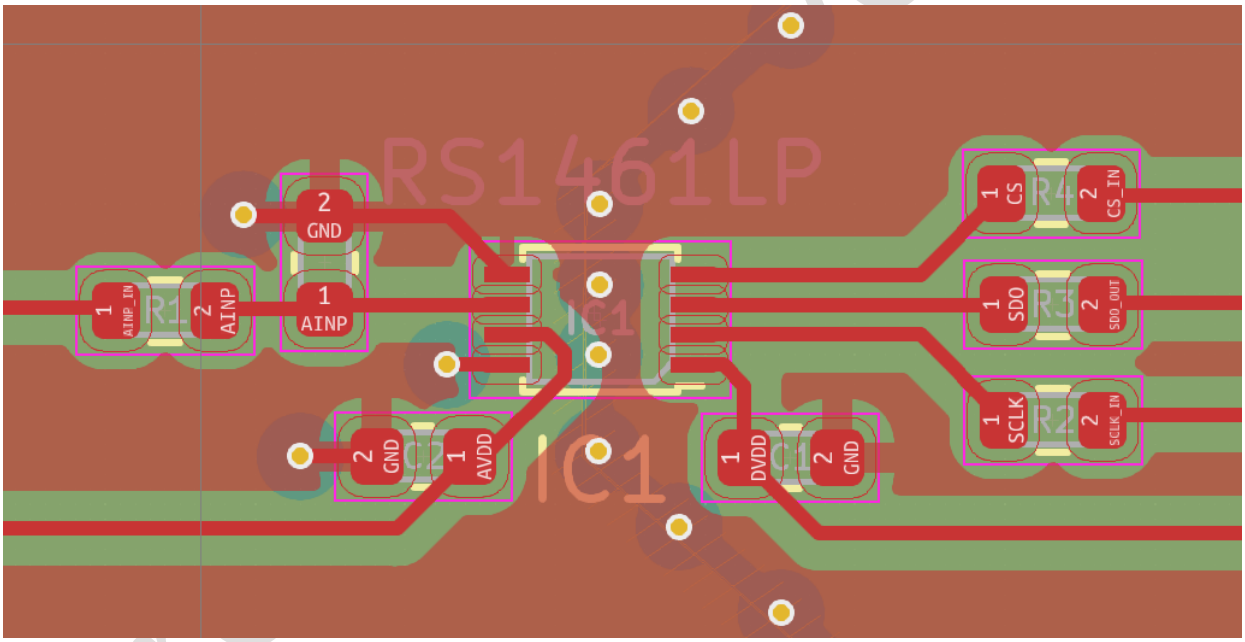
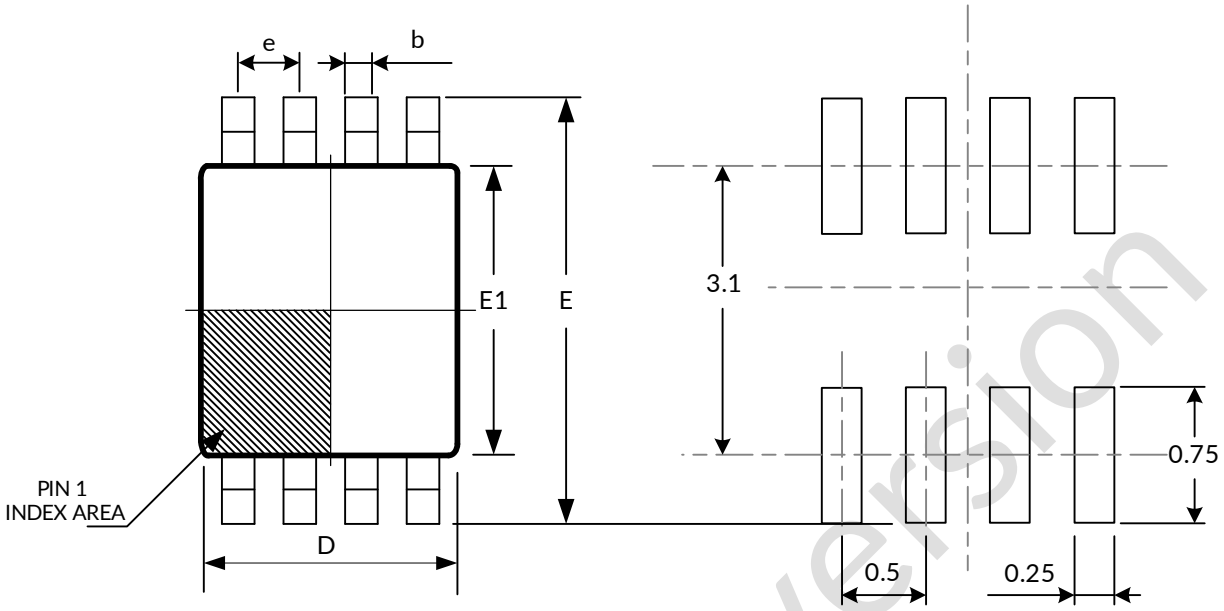


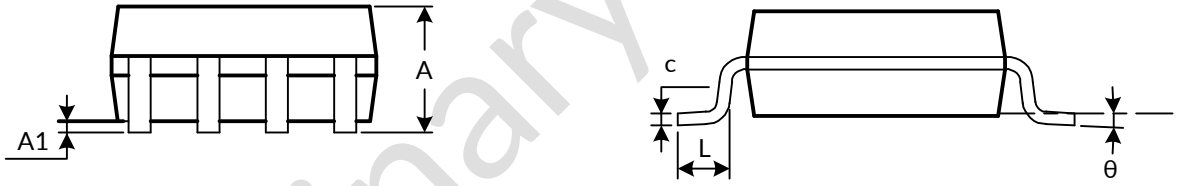
Figure 40. Example Layout

13 PACKAGE OUTLINE DIMENSIONS

VSSOP8 (3)



RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.600	0.900	0.024	0.085
A1	0.000	0.100	0.000	0.004
b	0.170	0.250	0.007	0.010
c	0.100	0.200	0.004	0.008
D (1)	1.900	2.100	0.075	0.083
e	0.500 (BSC) (2)		0.020 (BSC) (2)	
E	3.000	3.200	0.118	0.126
E1 (1)	2.200	2.400	0.087	0.095
L	0.200	0.350	0.008	0.014
θ	0°	6°	0°	6°

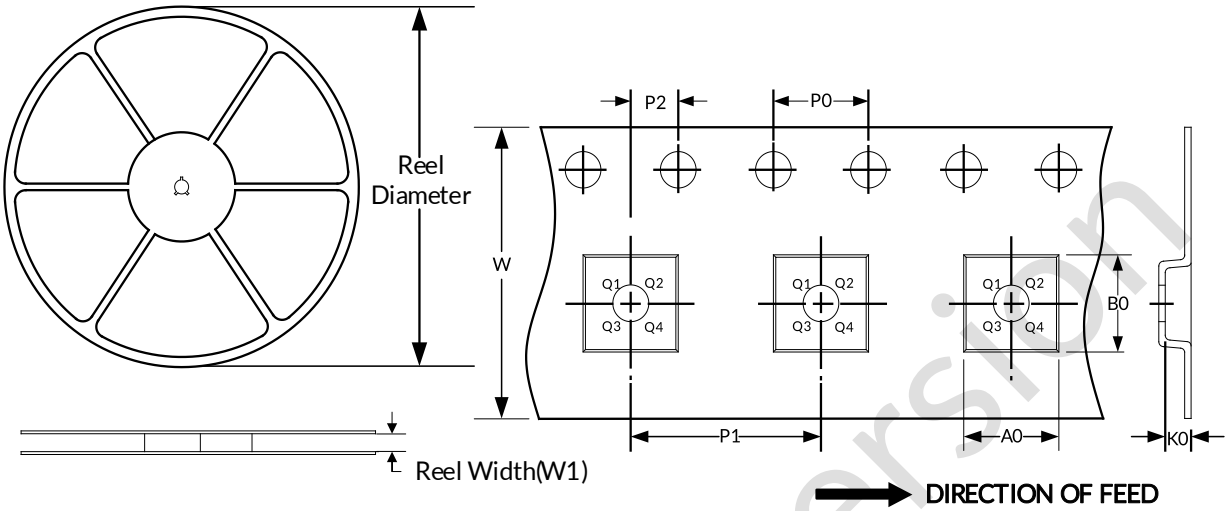
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

14 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
VSSOP8	7”	9.5	2.25	3.35	1.40	4.0	4.0	2.0	8.0	Q3

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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