

4-Bit Bidirectional Voltage-Level Translator with Automatic Direction Sensing

1 FEATURES

- **RS0204A-Q1 AEC-Q100 Qualification is Ongoing**
- **No Direction-Control**
- **Data Rates 100Mbps**
- **1.2V to 3.6V on A ports and 1.65V to 5.5V on B Ports ($V_{CCA} \leq V_{CCB}$)**
- **V_{CC} Isolation Feature: If Either V_{CC} Input is at GND, Both Ports are in the High-Impedance State**
- **Output Enable (OE) Input Circuit Referenced to V_{CCA}**
- **Low Power Consumption, 10 μ A Maximum I_{CC}**
- **No Power-Supply Sequencing Required: Either V_{CCA} or V_{CCB} can be Ramped First**
- **IOFF: Supports Partial-Power-Down Mode Operation**
- **Extended Temperature: -40°C to 125°C**

2 APPLICATIONS

- **Automotive Infotainment**
- **Advance Driver Assistance Systems (ADAS)**

3 DESCRIPTIONS

This 4-bit non-inverting translator is a bidirectional voltage-level translator and can be used to establish digital switching compatibility between mixed-voltage systems. It uses two separate configurable power-supply rails, with the A ports supporting operating voltages from 1.2V to 3.6V while it tracks the V_{CCA} supply, and the B ports supporting operating voltages from 1.65V to 5.5V while it tracks the V_{CCB} supply. This allows the support of both lower and higher logic signal levels while providing bidirectional translation capabilities between any of the 1.2V, 1.5V, 1.8V, 2.5V, 3.3V and 5V voltage nodes.

V_{CCA} must not exceed V_{CCB} .

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state, which significantly reduces the power-supply quiescent current consumption. OE has an internal pull-down current source, as long as V_{CCA} is powered.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The RS0204A-Q1 is available in Green UQFN1.7X2-12 and TSSOP14 packages. It operates over an ambient temperature range of -40°C to 125°C.

Device Information ⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS0204A-Q1	TSSOP14	5.00mm×4.40mm
	UQFN1.7X2-12	2.00mm×1.70mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 FUNCTIONAL BLOCK DIAGRAM

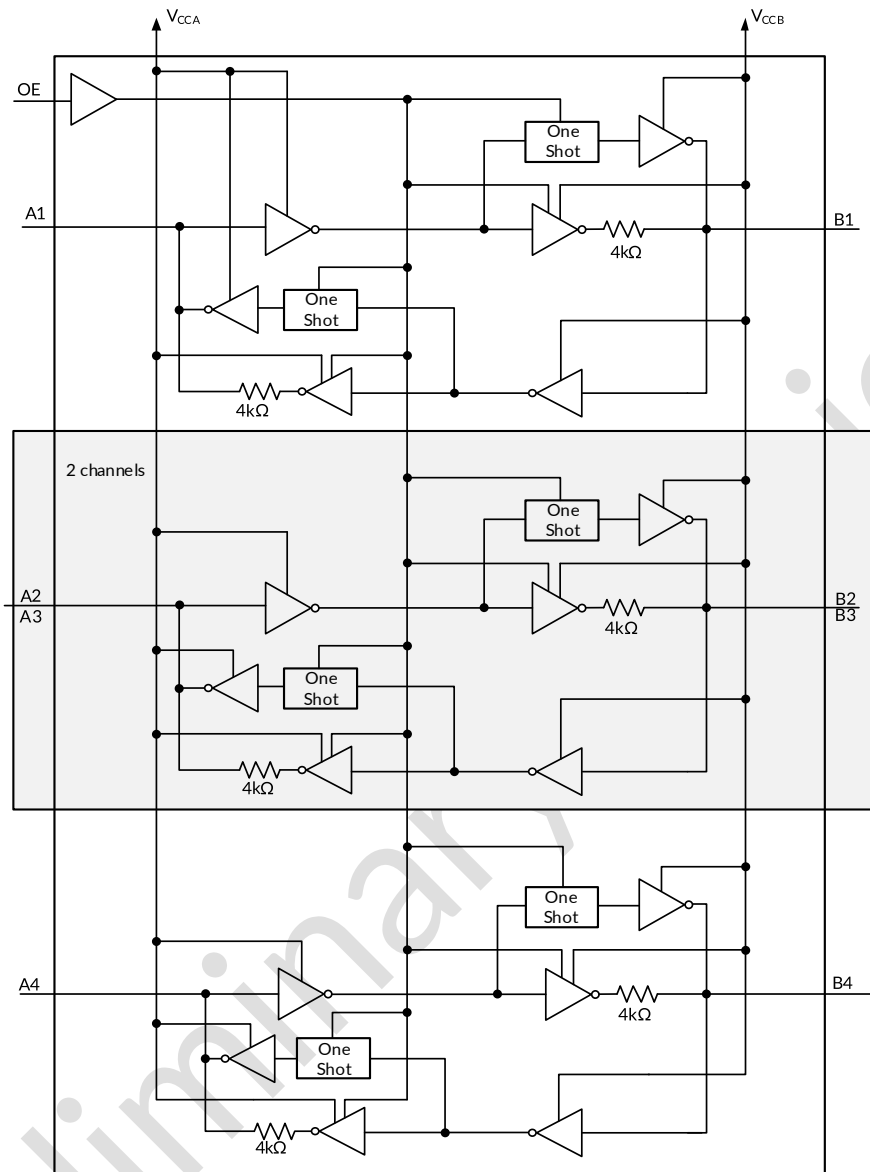


Table of Contents

1 FEATURES	1
2 APPLICATIONS	1
3 DESCRIPTIONS	1
4 FUNCTIONAL BLOCK DIAGRAM	2
5 REVISION HISTORY	4
6 PACKAGE/ORDERING INFORMATION ⁽¹⁾	5
7 PIN CONFIGURATIONS	6
8 SPECIFICATIONS	8
8.1 Absolute Maximum Ratings	8
8.2 ESD Ratings	8
8.3 Recommended Operating Conditions	9
8.4 Electrical Characteristics	10
8.5 Timing Requirements:	11
8.5.1 $V_{CCA}=1.2V$	11
8.5.2 $V_{CCA}=1.5V \pm 0.1 V$	11
8.5.3 $V_{CCA}=1.8V \pm 0.15 V$	11
8.5.4 $V_{CCA}=2.5V \pm 0.2 V$	11
8.5.5 $V_{CCA}=3.3V \pm 0.3 V$	11
8.6 Switching Characteristics: $V_{CCA}=1.2V$	12
8.7 Switching Characteristics: $V_{CCA}=1.5V \pm 0.1V$	12
8.8 Switching Characteristics: $V_{CCA}=1.8V \pm 0.15V$	13
8.9 Switching Characteristics: $V_{CCA}=2.5V \pm 0.2V$	13
8.10 Switching Characteristics: $V_{CCA}=3.3V \pm 0.3V$	14
9 OPERATING CHARACTERISTICS	14
10 PARAMETER MEASUREMENT INFORMATION	15
11 DETAILED DESCRIPTION	17
11.1 Overview	17
11.2 Architecture	17
11.3 Input Driver Requirements	18
11.4 Output Load Considerations	18
11.5 Enable and Disable	18
11.6 Pullup or Pulldown Resistors on I/O Lines	18
11.7 Device Functional Modes	18
12 APPLICATION AND IMPLEMENTATION	19
12.1 Application Information	19
12.2 Typical Application	19
13 PACKAGE OUTLINE DIMENSIONS	20
14 TAPE AND REEL INFORMATION	22

5 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2024/07/30	Preliminary version completed
A.0.1	2025/01/07	Update PACKAGE/ORDERING INFORMATION
A.0.2	2025/08/20	1. Update ESD Ratings 2. Update Recommended Operating Conditions 3. Update Switching Characteristics 4. Update TSSOP14 PACKAGE OUTLINE DIMENSIONS

Preliminary version

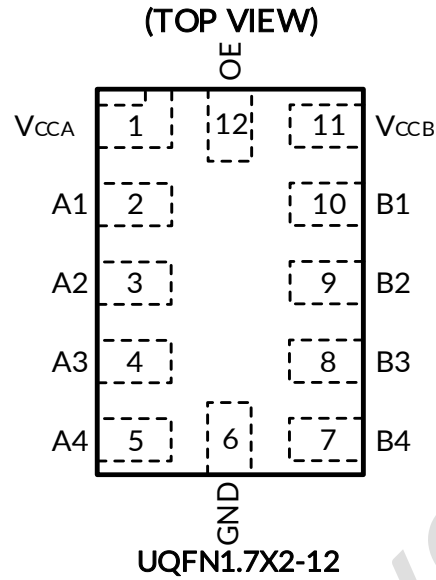
6 PACKAGE/ORDERING INFORMATION ⁽¹⁾

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	Lead finish/Ball material ⁽²⁾	MSL Peak Temp ⁽³⁾	PACKAGE MARKING ⁽⁴⁾	PACKAGE OPTION
RS0204A-Q1	RS0204AXUTQH12-Q1	-40°C ~125°C	UQFN1.7X2-12	NIPDAU	MSL1-260°-Unlimited	0204A	Tape and Reel, 4000
	RS0204AXQ-Q1	-40°C ~125°C	TSSOP14	SN	MSL1-260°-Unlimited	RS0204A	Tape and Reel, 4000

NOTE:

- (1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.
- (2) Lead finish/Ball material. Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F, Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.
- (4) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

7 PIN CONFIGURATIONS

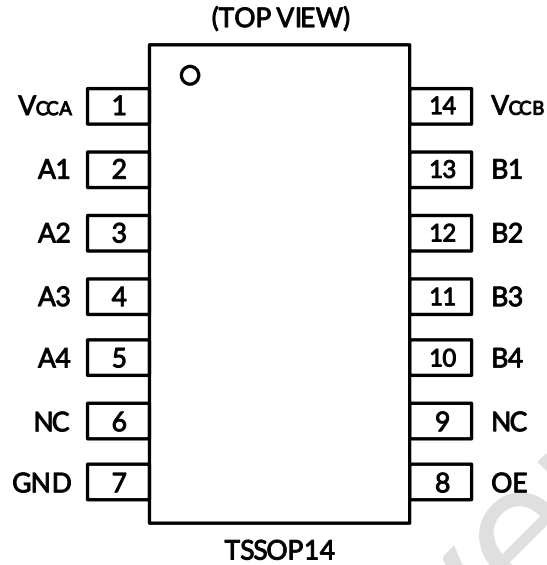


PIN DESCRIPTION

PIN	NAME	TYPE ⁽¹⁾	FUNCTION
UQFN1.7X2-12			
1	V _{CCA}	P	A Port Supply Voltage. $1.2V \leq V_{CCA} \leq 3.6V$ and $V_{CCA} \leq V_{CCB}$.
2	A1	I/O	Input/output A1. Reference to V _{CCA} .
3	A2	I/O	Input/output A2. Reference to V _{CCA} .
4	A3	I/O	Input/output A3. Reference to V _{CCA} .
5	A4	I/O	Input/output A4. Reference to V _{CCA} .
6	GND	-	Ground.
7	B4	I/O	Input/output B4. Reference to V _{CCB} .
8	B3	I/O	Input/output B3. Reference to V _{CCB} .
9	B2	I/O	Input/output B2. Reference to V _{CCB} .
10	B1	I/O	Input/output B1. Reference to V _{CCB} .
11	V _{CCB}	P	B Ports Supply Voltage. $1.65V \leq V_{CCB} \leq 5.5V$.
12	OE	I	Output Enable (Active High). Pull OE low to place all outputs in 3-state mode. Referenced to V _{CCA} .

(1) I=input, O=output, I/O=input and output, P=power

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN TSSOP14	NAME	TYPE ⁽¹⁾	FUNCTION
1	V _{CCA}	P	A Port Supply Voltage. $1.2V \leq V_{CCA} \leq 3.6V$ and $V_{CCA} \leq V_{CCB}$
2	A1	I/O	Input/output A1. Reference to V _{CCA} .
3	A2	I/O	Input/output A2. Reference to V _{CCA} .
4	A3	I/O	Input/output A3. Reference to V _{CCA} .
5	A4	I/O	Input/output A4. Reference to V _{CCA} .
6	NC	-	No internal connection.
7	GND	-	Ground.
8	OE	I	Output Enable (Active High). Pull OE low to place all outputs in 3-state mode. Referenced to V _{CCA} .
9	NC	-	No internal connection.
10	B4	I/O	Input/output B4. Reference to V _{CCB} .
11	B3	I/O	Input/output B3. Reference to V _{CCB} .
12	B2	I/O	Input/output B2. Reference to V _{CCB} .
13	B1	I/O	Input/output B1. Reference to V _{CCB} .
14	V _{CCB}	P	B Ports Supply Voltage. $1.65V \leq V_{CCB} \leq 5.5V$.

(1) I=input, O=output, I/O=input and output, P=power

8 SPECIFICATIONS

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

SYMBOL	PARAMETER		MIN	MAX	UNIT
V _{CCA}	Supply Voltage Range		-0.3	4.6	V
V _{CCB}	Supply Voltage Range		-0.3	6.5	V
V _I ⁽²⁾	Input Voltage Range	A port	-0.3	4.6	V
		B port	-0.3	6.5	
		OE	-0.3	4.6	
V _O ⁽²⁾	Voltage range applied to any output in the high-impedance or power-off state	A port	-0.3	4.6	V
		B port	-0.3	6.5	
V _O ⁽²⁾⁽³⁾	Voltage range applied to any output in the high or low state	A port	-0.3	V _{CCA} +0.3	V
		B port	-0.3	V _{CCB} +0.3	
I _{IK}	Input clamp current	V _I <0		-50	mA
I _{OK}	Output clamp current	V _O <0		-50	mA
I _O	Continuous output current			±50	mA
	Continuous current through V _{CCA} , V _{CCB} or GND			±100	mA
θ _{JA}	Package thermal impedance ⁽⁴⁾	TSSOP14		121	°C/W
		UQFN1.7X2-12		120	
T _J	Junction Temperature ⁽⁵⁾		-40	150	°C
T _{stg}	Storage temperature		-65	150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

(4) The package thermal impedance is calculated in accordance with JEDEC-51.

(5) The maximum power dissipation is a function of T_{J(MAX)}, R_{θJA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} - T_A) / R_{θJA}. All numbers apply for packages soldered directly onto a PCB.

8.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-Body Model (HBM), per AEC Q100-002 ⁽¹⁾	±2500	V
		Charged-Device Model (CDM), per AEC Q100-011	±1000	
		Latch-Up (LU), per AEC Q100-004	±200	mA

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.



ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.3 Recommended Operating Conditions

V_{CCI} is the supply voltage associated with the input port. V_{CCO} is the supply voltage associated with the output port. ⁽¹⁾⁽²⁾

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
Supply voltage	V _{CCA}		1.2		3.6	V
	V _{CCB}		1.65		5.5	
High-level input voltage (V _{IH})	A-port inputs	V _{CCA} = 1.2 V to 3.6 V V _{CCB} = 1.65 V to 5.5 V	V _{CCI} x 0.75 ⁽³⁾		V _{CCI}	V
	B-port inputs	V _{CCA} = 1.2 V to 3.6 V V _{CCB} = 1.65 V to 5.5 V	V _{CCI} x 0.75		V _{CCI}	
	OE input	V _{CCA} = 1.2 V to 3.6 V V _{CCB} = 1.65 V to 5.5 V	V _{CCA} x 0.75		5.5	
Low-level input voltage (V _{IL})	A-port inputs	V _{CCA} = 1.2 V to 3.6 V V _{CCB} = 1.65 V to 5.5 V	0		V _{CCI} x 0.35 ⁽³⁾	V
	B-port inputs	V _{CCA} = 1.2 V to 3.6 V V _{CCB} = 1.65 V to 5.5 V	0		V _{CCI} x 0.35	
	OE input	V _{CCA} = 1.2 V to 3.6 V V _{CCB} = 1.65 V to 5.5 V	0		V _{CCA} x 0.35	
Voltage applied to any output in the high-impedance or power-off state (V _O)	A-port	V _{CCA} = 1.2 V to 3.6 V V _{CCB} = 1.65 V to 5.5 V	0		3.6	V
	B-port	V _{CCA} = 1.2 V to 3.6 V V _{CCB} = 1.65 V to 5.5 V	0		5.5	
Input transition rise or fall rate(Δt/Δv)	A-port inputs	V _{CCA} = 1.2 V to 3.6 V V _{CCB} = 1.65 V to 5.5 V			40	ns/V
	B-port inputs	V _{CCA} = 1.2 V to 3.6 V	V _{CCB} = 1.65 V to 3.6 V		40	
			V _{CCB} = 4.5 V to 5.5 V		30	
T _A Operating free-air temperature			-40		125	°C

(1) The A and B sides of an unused data I/O pair must be held in the same state, that is, both at V_{CCI} or both at GND.

(2) V_{CCA} must be less than or equal to V_{CCB} and must not exceed 3.6 V.

(3) V_{CCI} is the supply voltage associated with the input port.

8.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted) ^{(1) (2) (3)}

PARAMETER	CONDITIONS	V _{CCA}	V _{CCB}	TEMP	MIN ⁽⁴⁾	TYP ⁽⁵⁾	MAX ⁽⁴⁾	UNIT
V _{OHA} Port A output high voltage	I _{OH} = -20μA	1.2V		+25°C		1.1		V
		1.4V to 3.6V		Full	V _{CCA} - 0.4			
V _{OLA} Port A output low voltage	I _{OL} = 20μA	1.2V		+25°C		0.3		
		1.4V to 3.6V		Full			0.4	
V _{OHB} Port B output high voltage	I _{OH} = -20μA		1.65V to 5.5V	Full	V _{CCB} - 0.4			V
V _{OLB} Port B output low voltage	I _{OL} = 20μA		1.65V to 5.5V	Full			0.4	
I _I Input leakage current	OE V _I =V _{CCI} or GND	1.2V to 3.6V	1.65V to 5.5V	+25°C			±1	μA
				Full			±2	
I _{off} Partial power down current	A Ports V _I or V _O =0 to 3.6V	0V	0V to 5.5V	+25°C			±1	μA
				Full			±2	
	B Ports V _I or V _O =0 to 5.5V	0V to 3.6V	0V	+25°C			±1	μA
				Full			±2	
I _{oz} ⁽⁶⁾ High-impedance State output current	A or B port OE=GND	1.2V to 3.6V	1.65V to 5.5V	+25°C			±1	μA
				Full			±2	
I _{CCA} V _{CCA} supply current	V _I =V _{CCI} or GND I _O = 0	1.2V	1.65V to 5.5V	+25°C		0.06		μA
		1.4V to 3.6V	1.65V to 5.5V	Full			5	
		3.6V	0V	Full			2	
		0V	5.5V	Full			-2	
I _{CCB} V _{CCB} supply current	V _I =V _{CCI} or GND I _O = 0	1.2V	1.65V to 5.5V	+25°C		3.4		μA
		1.4V to 3.6V	1.65V to 5.5V	Full			5	
		3.6V	0V	Full			-2	
		0V	5.5V	Full			2	
I _{CCA} + I _{CCB} Combined supply current	V _I = V _{CCI} or GND I _O = 0	1.2V	1.65V to 5.5V	+25°C		3.5		μA
		1.4V to 3.6V	1.65V to 5.5V	Full			10	
I _{CCZA} V _{CCA} supply current	V _I = V _{CCI} or GND I _O = 0, OE=GND	1.2V	1.65V to 5.5V	+25°C		0.05		μA
		1.4V to 3.6V	1.65V to 5.5V	Full			5	
I _{CCZB} V _{CCB} supply current	V _I = V _{CCI} or GND I _O = 0, OE=GND	1.2V	1.65V to 5.5V	+25°C		3.3		μA
		1.4V to 3.6V	1.65V to 5.5V	Full			5	
C _i Input capacitance	OE	1.2V to 3.6V	1.65V to 5.5V	+25°C		4		pF
C _{io} Input-to-output internal capacitance	A port	1.2V to 3.6V	1.65V to 5.5V	+25°C		5		pF
	B port	1.2V to 3.6V	1.65V to 5.5V	+25°C		9		

(1) V_{CCI} is the V_{CC} associated with the input port.

(2) V_{CCO} is the V_{CC} associated with the output port

(3) V_{CCA} must be less than or equal to V_{CCB}.

(4) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(5) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

(6) For I/O ports, the parameter I_{oz} includes the input leakage current.

8.5 Timing Requirements:

8.5.1 $V_{CCA}=1.2V$

$T_A=25^{\circ}C$, $V_{CCA}=1.2V$

		$V_{CCB}=1.8V$	$V_{CCB}=2.5V$	$V_{CCB}=3.3V$	$V_{CCB}=5V$	UNIT
		TYP	TYP	TYP	TYP	
Data rate		20	20	20	20	Mbps
Pulse duration(t_w)	data inputs	50	50	50	50	ns

8.5.2 $V_{CCA}=1.5V\pm0.1V$

$T_A=25^{\circ}C$, $V_{CCA}=1.5V\pm0.1V$ (unless otherwise noted)

		$V_{CCB}=1.8V\pm0.15V$	$V_{CCB}=2.5V\pm0.2V$	$V_{CCB}=3.3V\pm0.3V$	$V_{CCB}=5V\pm0.5V$	UNIT
		TYP	TYP	TYP	TYP	
Data rate		40	40	40	40	Mbps
Pulse duration(t_w)	data inputs	25	25	25	25	ns

8.5.3 $V_{CCA}=1.8V\pm0.15V$

$T_A=25^{\circ}C$, $V_{CCA}=1.8V\pm0.15V$ (unless otherwise noted)

		$V_{CCB}=1.8V\pm0.15V$	$V_{CCB}=2.5V\pm0.2V$	$V_{CCB}=3.3V\pm0.3V$	$V_{CCB}=5V\pm0.5V$	UNIT
		TYP	TYP	TYP	TYP	
Data rate		50	50	50	50	Mbps
Pulse duration(t_w)	data inputs	25	25	25	25	ns

8.5.4 $V_{CCA}=2.5V\pm0.2V$

$T_A=25^{\circ}C$, $V_{CCA}=2.5V\pm0.2V$ (unless otherwise noted)

		$V_{CCB}=2.5V\pm0.2V$	$V_{CCB}=3.3V\pm0.3V$	$V_{CCB}=5V\pm0.5V$	UNIT
		TYP	TYP	TYP	
Data rate		70	80	80	Mbps
Pulse duration(t_w)	data inputs	14	12	12	ns

8.5.5 $V_{CCA}=3.3V\pm0.3V$

$T_A=25^{\circ}C$, $V_{CCA}=3.3V\pm0.3V$ (unless otherwise noted)

		$V_{CCB}=3.3V\pm0.3V$	$V_{CCB}=5V\pm0.5V$	UNIT
		TYP	TYP	
Data rate		80	100	Mbps
Pulse duration(t_w)	data inputs	12	10	ns

8.6 Switching Characteristics: $V_{CCA}=1.2V$

 $T_A=25^{\circ}C$, $V_{CCA}=1.2V$

PARAMETER	CONDITIONS	$V_{CCB}=1.8V$			$V_{CCB}=2.5V$			$V_{CCB}=3.3V$			$V_{CCB}=5V$			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL} Propagation delay time high-to-low output	A-to-B	15		45.5	13		39.2	12.1		36.5	10.6		32	ns
t_{PLH} Propagation delay time low-to-high output	A-to-B	15.9		47.7	12.5		37.5	11.6		35	11.3		34.1	ns
t_{PHL} Propagation delay time high-to-low output	B-to-A	19.5		58.5	17.4		52.2	10.4		31.5	10		30.2	ns
t_{PLH} Propagation delay time low-to-high output	B-to-A	15		45.5	13		39.2	12.3		36.9	11.1		33.3	ns
t_{en} Enable time	OE-to-A or B	184		552	156		470	145		435	144		432	ns
t_{dis} Disable time	OE-to-A or B	358		1074	343		1031	329		989	289		867	ns
t_{rA} , t_{fA} Input rise time	A port rise and fall time	6.2		18.6	6.1		18.5	6.3		19.1	6.2		18.6	ns
t_{rB} , t_{fB} Input rise time	B port rise and fall time	1.6		4.8	0.75		2.3	0.5		1.5	0.4		1.4	ns
Maximum data rate			20			20			20			20		Mbps

8.7 Switching Characteristics: $V_{CCA}=1.5V \pm 0.1V$

over recommended operating free-air temperature range, $V_{CCA}=1.5V \pm 0.1V$ (unless otherwise noted)

PARAMETER	CONDITIONS	$V_{CCB}=1.8V \pm 0.15V$			$V_{CCB}=2.5V \pm 0.2V$			$V_{CCB}=3.3V \pm 0.3V$			$V_{CCB}=5V \pm 0.5V$			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL} Propagation delay time high-to-low output	A-to-B	9.8		29.7	6.6		19.8	6		18	5.7		17.3	ns
t_{PLH} Propagation delay time low-to-high output	A-to-B	11.2		33.8	7.6		23	7		21	6.4		19.2	ns
t_{PHL} Propagation delay time high-to-low output	B-to-A	10.9		32.9	9.1		27.5	8.8		26.6	8.5		25.7	ns
t_{PLH} Propagation delay time low-to-high output	B-to-A	10.5		31.5	8.4		25.2	7.9		23.7	7.5		22.7	ns
t_{en} Enable time	OE-to-A or B	162		488	155		467	142		428	134		402	ns
t_{dis} Disable time	OE-to-A or B	344		1032	339		1019	326		978	286		858	ns
t_{rA} , t_{fA} Input rise time	A port rise and fall time	2.1		6.3	2.1		6.3	2.1		6.3	2		6.2	ns
t_{rB} , t_{fB} Input rise time	B port rise and fall time	1.5		4.7	0.7		2.3	0.5		1.5	0.45		1.4	ns
Maximum data rate			40			40			40			40		Mbps

8.8 Switching Characteristics: $V_{CCA}=1.8V \pm 0.15V$

over recommended operating free-air temperature range, $V_{CCA}=1.8V \pm 0.15V$ (unless otherwise noted)

PARAMETER	CONDITIONS	$V_{CCB}=1.8V \pm 0.15V$			$V_{CCB}=2.5V \pm 0.2V$			$V_{CCB}=3.3V \pm 0.3V$			$V_{CCB}=5V \pm 0.5V$			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL} Propagation delay time high-to-low output	A-to-B	8.5		25.5	5.6		17	5		15	4.6		14	ns
t_{PLH} Propagation delay time low-to-high output	A-to-B	9.2		27.8	6		18	5.2		15.8	4.7		14.3	ns
t_{PHL} Propagation delay time high-to-low output	B-to-A	8.2		24.8	5.8		17.6	5.2		15.8	5		15	ns
t_{PLH} Propagation delay time low-to-high output	B-to-A	8.2		24.8	6.3		18.9	5.5		16.7	4.3		13.1	ns
t_{en} Enable time	OE-to-A or B	157		473	153		461	139		417	129		389	ns
t_{dis} Disable time	OE-to-A or B	330		992	324		972	320		962	270		810	ns
t_{rA}, t_{fA} Input rise time	A port rise and fall time	1.5		4.5	1.5		4.7	1.6		4.8	1.5		4.5	ns
t_{rB}, t_{fB} Input rise time	B port rise and fall time	1.5		4.7	0.5		1.7	0.45		1.4	0.45		1.4	ns
Maximum data rate			50			50			50			50		Mbps

8.9 Switching Characteristics: $V_{CCA}=2.5V \pm 0.2V$

over recommended operating free-air temperature range, $V_{CCA}=2.5V \pm 0.2V$ (unless otherwise noted)

PARAMETER	CONDITIONS	$V_{CCB}=2.5V \pm 0.2V$			$V_{CCB}=3.3V \pm 0.3V$			$V_{CCB}=5V \pm 0.5V$			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL} Propagation delay time high-to-low output	A-to-B	5		15	4.5		13.5	4.2		12.8	ns
t_{PLH} Propagation delay time low-to-high output	A-to-B	5.2		15.8	4.5		13.5	4.1		12.5	ns
t_{PHL} Propagation delay time high-to-low output	B-to-A	4.6		14	4.2		12.6	3.9		11.7	ns
t_{PLH} Propagation delay time low-to-high output	B-to-A	4.6		14	3.9		11.7	3.7		11.3	ns
t_{en} Enable time	OE-to-A or B	144		432	128		389	121		365	ns
t_{dis} Disable time	OE-to-A or B	318		956	310		932	265		795	ns
t_{rA}, t_{fA} Input rise time	A port rise and fall time	0.5		1.5	0.4		1.4	0.4		1.4	ns
t_{rB}, t_{fB} Input rise time	B port rise and fall time	0.5		1.7	0.4		1.4	0.4		1.4	ns
Maximum data rate			70			80			80		Mbps

8.10 Switching Characteristics: $V_{CCA}=3.3V \pm 0.3V$

over recommended operating free-air temperature range, $V_{CCA}=3.3V \pm 0.3V$ (unless otherwise noted)

PARAMETER		CONDITIONS	V _{CCB} =3.3V ±0.3V			V _{CCB} =5V ±0.5V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t _{PHL}	Propagation delay time high-to-low output	A-to-B	4.2		12.8	3.7		11.3	ns
t _{PLH}	Propagation delay time low-to-high output	A-to-B	4.2		12.6	3.6		11	ns
t _{PHL}	Propagation delay time high-to-low output	B-to-A	3.7		11.3	3.4		10.4	ns
t _{PLH}	Propagation delay time low-to-high output	B-to-A	4		12.2	3.7		11.3	ns
t _{en}	Enable time	OE-to-A or B	124		372	116		350	ns
t _{dis}	Disable time	OE-to-A or B	305		915	251		755	ns
t _{rA}	Input rise time	A port rise time	0.4		1.2	0.45		1.4	ns
t _{rB}	Input rise time	B port rise time	0.45		1.4	0.45		1.4	ns
t _{fA}	Input fall time	A port fall time	0.4		1.2	0.45		1.4	ns
t _{fB}	Input fall time	B port fall time	0.45		1.4	0.45		1.4	ns
Maximum data rate				80			100		Mbps

9 OPERATING CHARACTERISTICS

$T_A=25^\circ C$

PARAMETER		CONDITIONS		V _{CCA}							UNIT
				1.2V	1.2V	1.5V	1.8V	2.5V	2.5V	3.3V	
				V _{CCB}							
				5V	1.8V	1.8V	1.8V	2.5V	5V	3.3V to 5V	
				TYP	TYP	TYP	TYP	TYP	TYP	TYP	
C _{pdA}	Power dissipation capacitance	C _L =0 f=10MHz t _r =t _f =1ns OE=V _{CCA} (outputs enabled)	A-port input B-port output	0.53	28	16	17	4	5	15	pF
			B-port input A-port output	11	11	11	11	11	11	11	
C _{pdB}	Power dissipation capacitance		A-port input B-port output	23	18	18	17	19	23	7	
			B-port input A-port output	41	24	20	20	19	35	23	
C _{pdA}	Power dissipation capacitance	C _L =0 f=10MHz t _r =t _f =1ns OE=GND (outputs enabled)	A-port input B-port output	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF
			B-port input A-port output	0.01	0.01	0.01	0.01	0.01	0.01	0.01	
C _{pdB}	Power dissipation capacitance		A-port input B-port output	0.01	0.01	0.01	0.01	0.01	0.01	0.01	
			B-port input A-port output	0.01	0.01	0.01	0.01	0.01	0.01	0.01	

10 PARAMETER MEASUREMENT INFORMATION

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- PRR 10 MHz
- $Z_o = 50 \Omega$
- $dv/dt \geq 1 \text{ V/ns}$

Note: All input pulses are measured one at a time, with one transition per measurement.

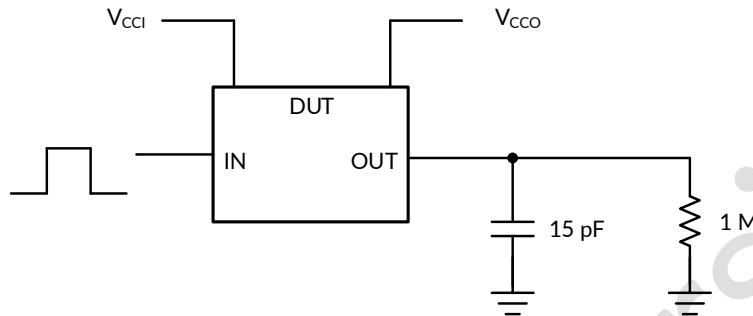


Figure 1. Data Rate, Pulse Duration, Propagation Delay, Output Rise And Fall Time Measurement Using A Push-Pull Driver

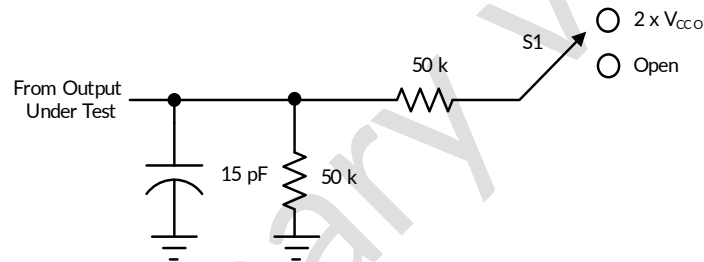


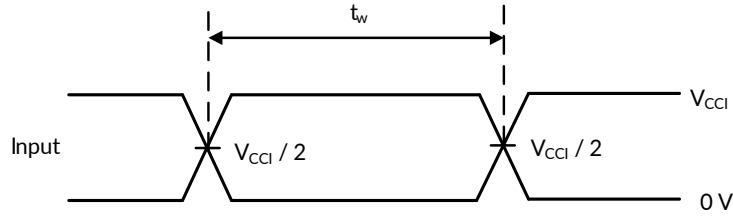
Figure 2. Load Circuit for Enable/Disable Time Measurement

Table 1. Switch Configuration for Enable/Disable Timing

TEST	S1
$t_{PZL}^{(1)}, t_{PLZ}^{(2)}$	$2 \times V_{CCO}$
$t_{PHZ}^{(1)}, t_{PZH}^{(2)}$	Open

(1) t_{PZL} and t_{PZH} are the same as t_{en} .

(2) t_{PLZ} and t_{PHZ} are the same as t_{dis} .



(1) All input pulses are measured one at a time, with one transition per measurement.

Figure 3. Voltage Waveforms Pulse Duration

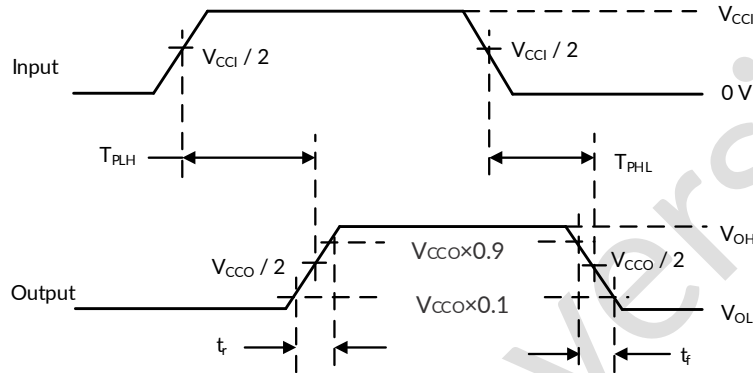
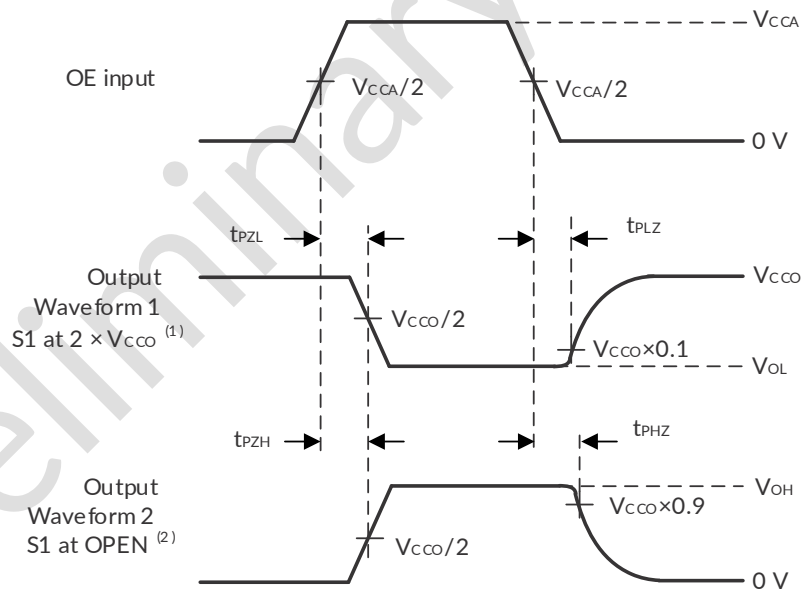


Figure 4. Voltage Waveforms Propagation Delay Times



A. Waveform 1 is for an output with internal such that the output is high, except when OE is high.
 B. Waveform 2 is for an output with conditions such that the output is low, except when OE is high.

Figure 5. Voltage Waveforms Enable and Disable

11 DETAILED DESCRIPTION

11.1 Overview

The RS0204A-Q1 device is a 4-bit, directionless voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.2 V to 3.6 V, while the B port can accept I/O voltages from 1.65 V to 5.5 V. The device is a buffered architecture with edge-rate accelerators (one-shots) to improve the overall data rate. This device can only translate push-pull CMOS logic outputs. If for open-drain signal translation, please refer to RS010X products.

11.2 Architecture

The RS0204A-Q1 device architecture (see Figure 6) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a DC state, the output drivers of the device maintain a high or low, but are designed to be weak, so the output drivers can be overdriven by an external driver when data on the bus flows the opposite direction.

The output one-shots detect rising or falling edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one-shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 70 Ω at $V_{CCO} = 1.2$ V to 1.8 V, 50 Ω at $V_{CCO} = 1.8$ V to 3.3 V, and 40 Ω at $V_{CCO} = 3.3$ V to 5 V.

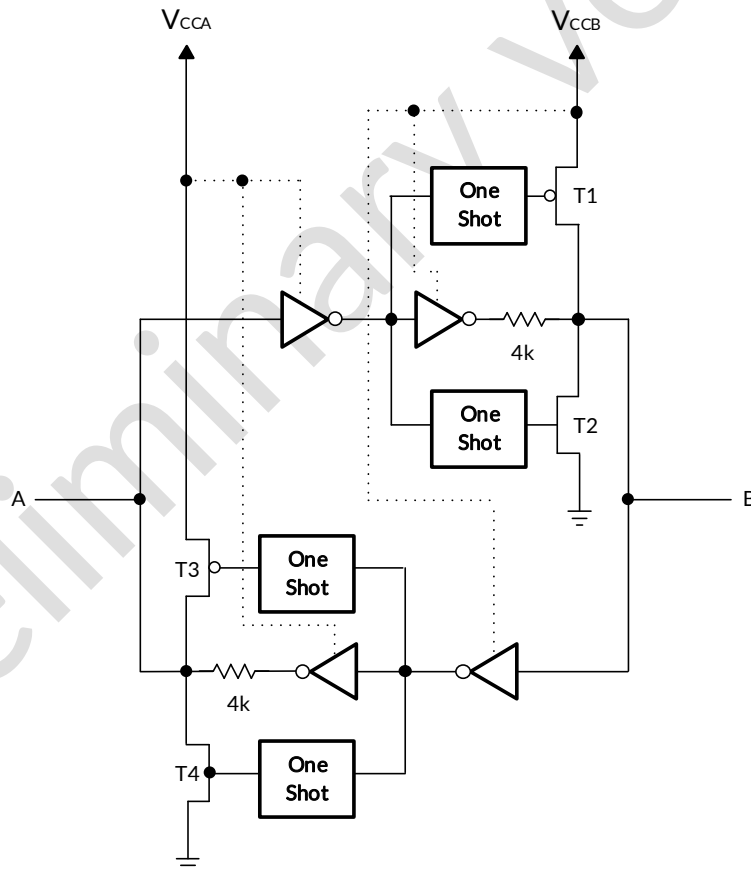


Figure 6. Architecture of RS0204A-Q1 Device I/O Cell

11.3 Input Driver Requirements

Typical I_{IN} vs V_{IN} characteristics of the device are shown in Figure 7. For proper operation, the device driving the data I/Os of the RS0204A-Q1 device must have driven strength of at least ± 2 mA.

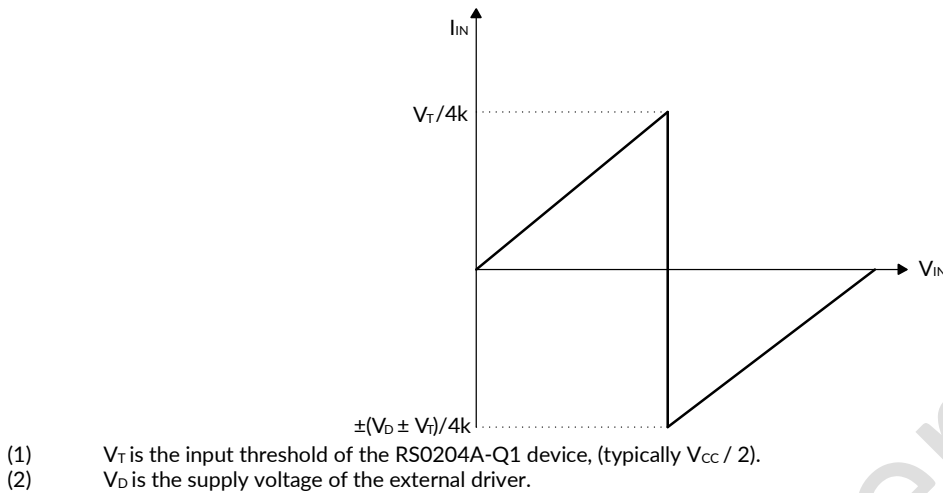


Figure 7. Typical I_{IN} vs V_{IN} Curve

11.4 Output Load Considerations

We recommend careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper O.S. triggering takes place. PCB signal trace-lengths must be kept short enough such that the round-trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The O.S. circuits have been designed to stay on for approximately 10 ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic I_{CC} , load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the device output sees, so it is recommended that this lumped-load capacitance be considered to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

11.5 Enable and Disable

The RS0204A-Q1 device has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

11.6 Pullup or Pulldown Resistors on I/O Lines

The device is designed to drive capacitive loads of up to 70 pF. The output drivers of the RS0204A-Q1 device have low dc drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 50 k Ω to ensure that they do not contend with the output drivers of the RS0204A-Q1 device.

For the same reason, the RS0204A-Q1 device must not be used in applications such as I²C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the RS010X series of level translators.

11.7 Device Functional Modes

The device has two functional modes, enabled and disabled. To disable the device, set the OE input to low, which places all I/Os in a high impedance state. Setting the OE input to high will enable the device.

12 APPLICATION AND IMPLEMENTATION

Information in the following applications sections is not part of the RUNIC component specification, and RUNIC does not warrant its accuracy or completeness. RUNIC's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

12.1 Application Information

The RS0204A-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. It can only translate push-pull CMOS logic outputs. Any external pulldown or pullup resistors are recommended larger than 50kΩ.

12.2 Typical Application

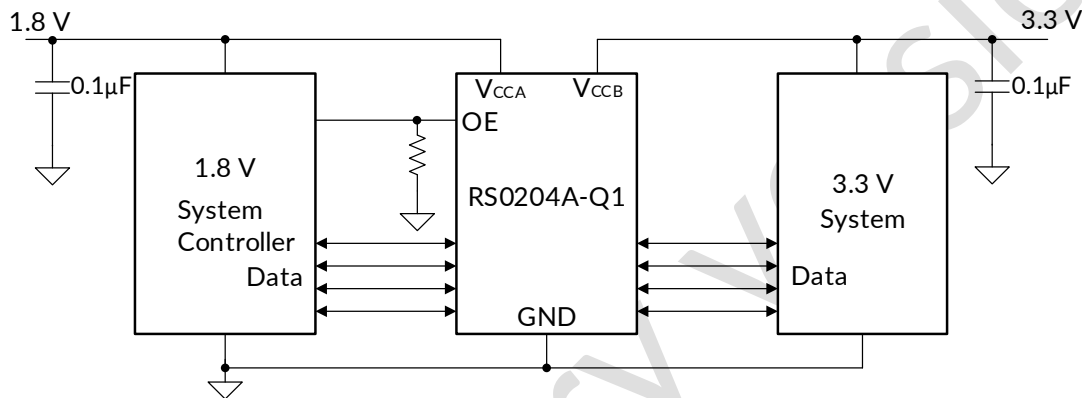
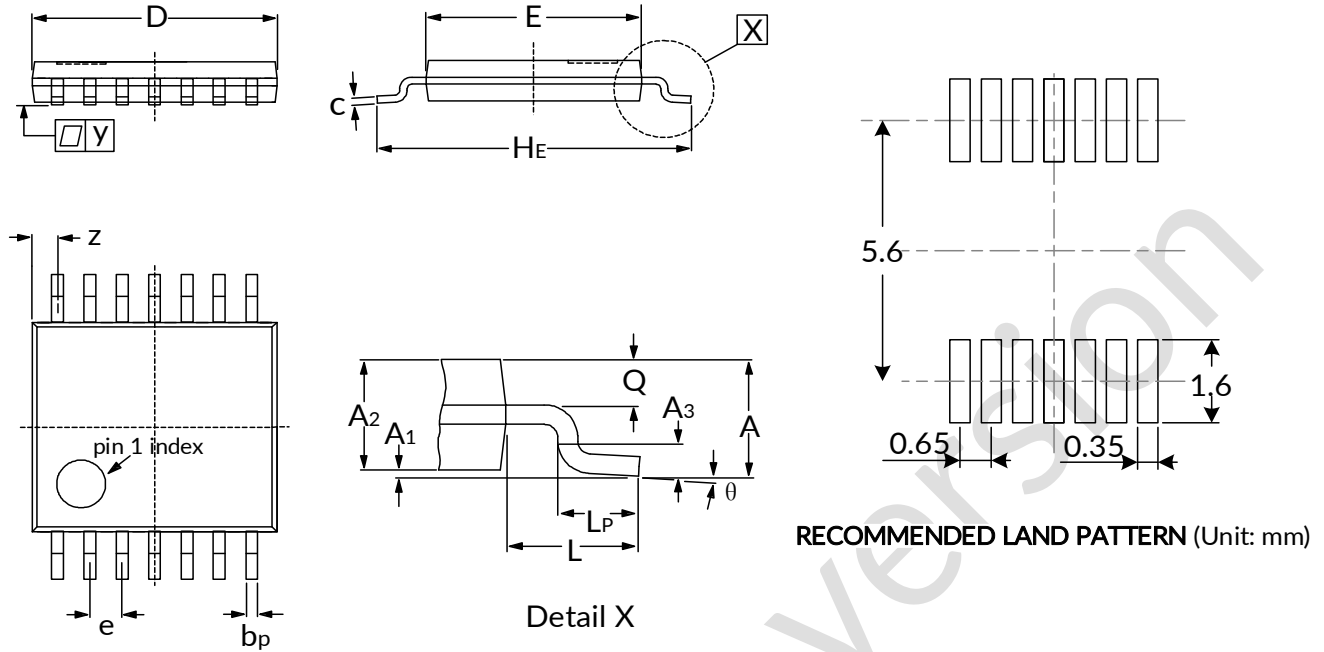


Figure 8. Typical Application Circuit

13 PACKAGE OUTLINE DIMENSIONS

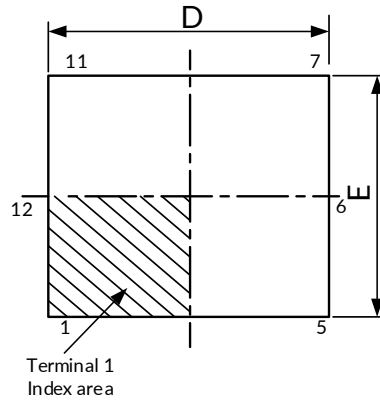
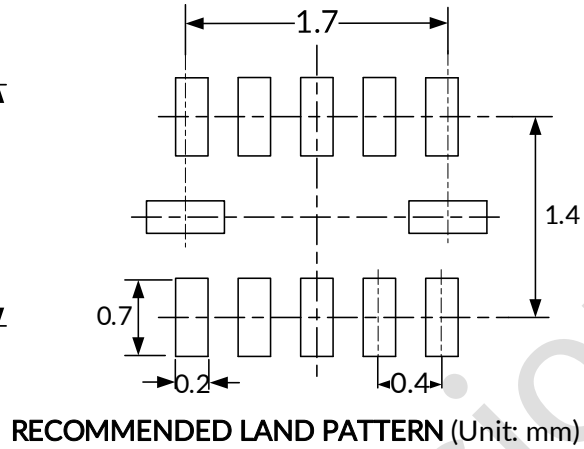
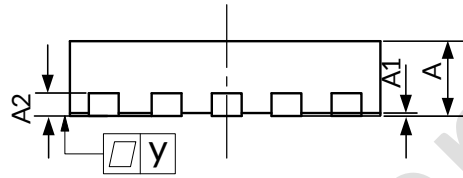
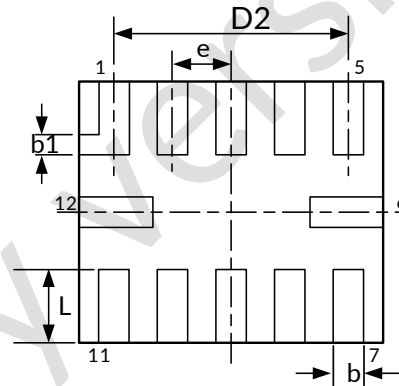
TSSOP14⁽²⁾



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A ⁽¹⁾		1.200		0.047
A ₁	0.050	0.150	0.002	0.006
A ₂	0.800	1.050	0.031	0.041
A ₃	0.250		0.010	
b _p	0.190	0.300	0.007	0.012
c	0.100	0.200	0.004	0.008
D ⁽¹⁾	4.900	5.100	0.193	0.201
E ⁽¹⁾	4.300	4.500	0.169	0.177
H _E	6.200	6.600	0.244	0.260
e	0.650		0.026	
L	1		0.039	
L _P	0.450	0.750	0.017	0.030
Q	0.300	0.490	0.012	0.019
Z	0.380	0.720	0.015	0.028
y	0.1		0.004	
θ	0°	8°	0°	8°

NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. This drawing is subject to change without notice.

UQFN1.7X2-12⁽²⁾

TOP VIEW

RECOMMENDED LAND PATTERN (Unit: mm)

SIDE VIEW

BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A ⁽¹⁾		0.500		0.020
A1	0.000	0.050	0.000	0.002
A2	0.127		0.005	
D ⁽¹⁾	1.900	2.100	0.075	0.083
E ⁽¹⁾	1.600	1.800	0.063	0.071
D2	1.500	1.700	0.059	0.067
b	0.150	0.250	0.006	0.010
b1	0.150		0.006	
e	0.400		0.016	
y	0.050		0.002	
L	0.450	0.550	0.017	0.022

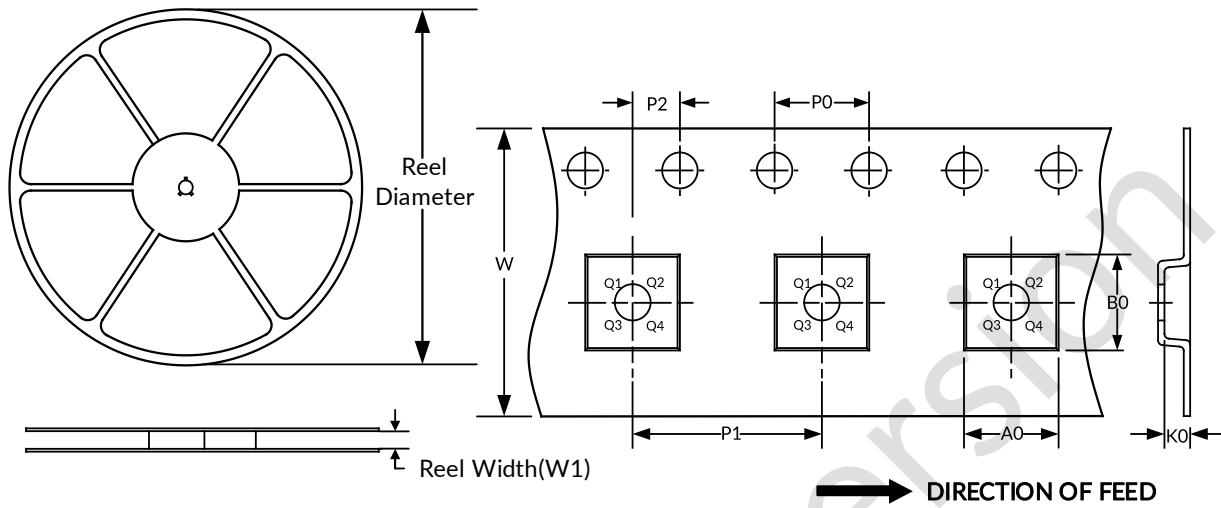
NOTE:

1. Plastic or metal protrusions of 0.075mm maximum per side are not included.
2. This drawing is subject to change without notice.

14 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP14	13"	12.4	6.95	5.60	1.20	4.0	8.0	2.0	12.0	Q1
UQFN1.7X2-12	7"	9.0	1.90	2.30	0.75	4.0	4.0	2.0	8.0	Q1

NOTE:

1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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Preliminary version