2-Bit Dual-Supply Bidirectional I^3C/I^2C-Bus and SPI Voltage-Level Translator

1 FEATURES

- **Wide Supply Voltage Range:**
  - **V_{CCA}: 0.72 V to 1.98 V and V_{CCB}: 0.72 V to 1.98 V; $V_{CCA} \leq V_{CCB}$**
- **I_{OFF} Circuitry Provides Partial Power-Down Mode Operation**
- **Inputs Accept Voltages Up to 1.98 V and are Overvoltage Tolerant to 1.98 V**
- **Provided Voltage Level Translation for I^3C, I^2C-bus, SMBus, and SPI Devices**
- **ESD Protection:**
  - **HBM JESD22-A114E Class 2 Exceeds 4000 V**
  - **CDM JESD22-C101E Exceeds 1000 V**
- **Latch-Up Performance Exceeds 100 mA per JESD 78B Class II**
- **Available in XDFN1.4X1-8 package**
- **Specified from -40 °C to +125 °C**

2 APPLICATIONS

- **Servers**
- **Wearables**
- **Personal Electronics**

3 DESCRIPTIONS

The RS0322 is a 2-bit, dual-supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation for traditional I^2C-bus/SMBus applications, 12.5 MHz I^3C-bus applications and also higher speed SPI applications (with two devices). It features two 1-bit input-output ports (An and Bn), one output enable input (OE) and two supply pins (V_{CCA} and V_{CCB}). V_{CCA} can be supplied at any voltage between 0.72 V and 1.98 V and V_{CCB} can be supplied at any voltage between 0.72 V and 1.98 V, making the device suitable for translating between any of the low voltage nodes (0.8 V, 1.2 V, and 1.8 V). V_{CCA} must be ≤V_{CCB} to ensure proper operation.

RS0322 can be used for both open drain as well as push-pull application which allows for level translation applications using I^3C, I^2C, and SPI protocols.

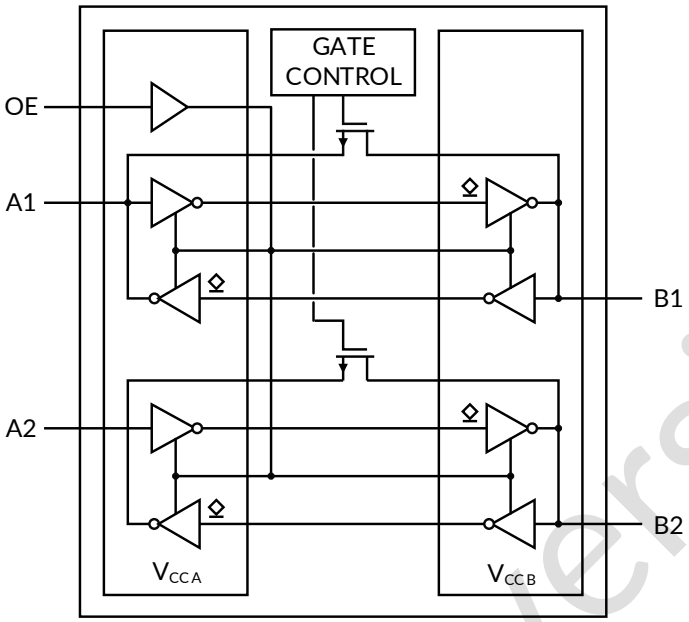
Pins An are referenced to V_{CCA} and pins Bn are referenced to V_{CCB}. The active HIGH OE pin is referenced to V_{CCA} and controllable by a signal in either V_{CCA} or V_{CCB} domain. A LOW level at pin OE causes the outputs to be in a high-impedance OFF-state. This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it ispowered down.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS0322	XDFN1.4X1-8	1.00mm×1.40mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 FUNCTIONAL BLOCK DIAGRAM



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5 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2026/03/24	Preliminary version completed

6 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING (2)	MSL (3)	PACKAGE OPTION
RS0322	RS0322XUTDS8	-40°C ~125°C	XDFN1.4X1-8	0322	MSL3	Tape and Reel, 5000

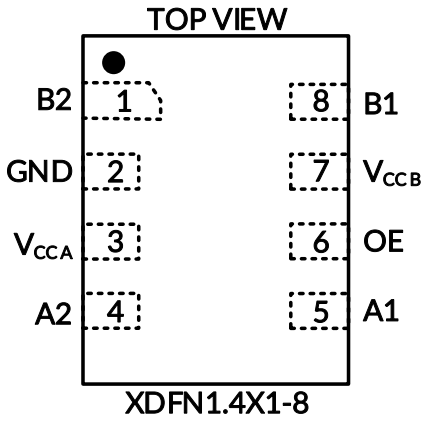
NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

7 PIN CONFIGURATION AND FUNCTIONS



7.1 Pin Description

NAME	PIN	FUNCTION
	XDFN1.4X1-8	
B1, B2	1, 8	B port - data input or output (referenced to V_{CCB})
GND	2	Ground (0 V)
V_{CCA}	3	Supply voltage A
A2, A1	4, 5	A port - data input or output (referenced to V_{CCA})
OE	6	Output enable input (active HIGH, referenced to V_{CCA}); signal can be from V_{CCA} or V_{CCB} domain
V_{CCB}	7	Supply voltage B

7.2 Function Table (1)

Supply voltage		Input	Input/output
V_{CCA}	V_{CCB}	OE (2)	
0.72 V to 1.98 V	0.72 V to 1.98 V	L	Disconnected
0.72 V to 1.98 V	0.72 V to 1.98 V	H	A1 = B1; A2 = B2
GND (3)	GND (3)	X	Disconnected

(1) H = HIGH voltage level; L = LOW voltage level; X = don't care.
(2) V_{IL} and V_{IH} are referenced to V_{CCA}. The OE can be controlled by an external device that is powered by either V_{CCA} or V_{CCB}. As V_{CCB} is required to begreater than V_{CCA}, the OE pin has been designed to withstand a voltage equal to V_{CCB} (up to 1.98 V per recommended functional voltage range).
(3) When either V_{CCA} or V_{CCB} is at GND level, the device goes into power-down mode.

8 SPECIFICATIONS

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage A	$V_{CCA} \le V_{CCB}$	-0.5	2.5	V
V_{CCB}	Supply voltage B	$V_{CCA} \le V_{CCB}$	-0.5	2.5	
V_I	Input voltage	A port, B port, and OE (2)	-0.5	2.5	
V_O	Output voltage	Active mode (2) (3) (4)	-0.5	V_{CCO}+0.25	
		Power-down or 3-state mode (2)	-0.5	2.5	
I_{IK}	Input clamping current	V_I< 0 V	-50		mA
I_{OK}	Output clamping current	V_O < 0 V	-50		
I_O	Output current	V_O = 0 V to V_{CCO} (3)		±50	
I_{CC}	Supply current	$I_{CC(A)}$ or $I_{CC(B)}$		100	
I_{GND}	Ground current		-100		
θ_{JA}	Package thermal impedance (5)	XDFN1.4X1-8		265	°C/W
T_{stg}	Storage Temperature Range		-65	150	°C
P_{tot}	Total power dissipation	T_{amb} = -40°C to 125°C		125	mW

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The minimum input and minimum output voltage ratings can be exceeded if the input and output current ratings are observed.
(3) V_{CCO} is the supply voltage associated with the output.
(4) V_{CCO} + 0.25 V should not exceed 2.5 V.
(5) The package thermal impedance is calculated in accordance with JESD-51.

8.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-Body Model (HBM)	±4000	V
	Charged Device Model (CDM)	±1000	

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.3 Recommended operating conditions (1)

Over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V_{CCA}	Supply voltage A	$V_{CCA} \le V_{CCB}$		0.72	1.98	V
V_{CCB}	Supply voltage B	$V_{CCA} \le V_{CCB}$		0.72	1.98	V
V_I	Input voltage	A port, B port, and OE		0	1.98	V
V_O	Output voltage	Power-down or 3-state mode; V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 0.72 V to 1.98 V	A port	0	1.98	V
			B port	0	1.98	V
T_{amb}	Ambient temperature			-40	125	°C
T_J	Junction temperature (2)			-40	125	°C
$\Delta t/\Delta V$	Input transition rise and fall rate	V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 0.72 V to 1.98 V			<5.3	ns/V

(1) The A and B sides of an unused I/O pair must be held in the same state, both at V_{CCI} or both at GND.

(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

8.4 Typical Static Characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
C_I	Input Capacitance	OE input; V_{CCA} = 0.72 V to 1.98 V; V_{CCB} =0.72 V to 1.98 V		1.6		pF
$C_{I/O}$	Input/Output Capacitance	A port; V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 0.72 V to 1.98 V		3.4		pF
		B port; V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 0.72 V to 1.98 V		3.4		pF

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

8.5 Static Characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	-40 °C to +85 °C		-40 °C to +125 °C		UNIT
			MIN(3)	MAX(3)	MIN(3)	MAX(3)	
V_{IH}	HIGH-Level Input Voltage	A port or B port					
		V_{CCA} = 0.72 V to 0.9 V; V_{CCB} = 0.72 V to 0.9 V (1)	0.75V_{CCI}		0.75V_{CCI}		V
		V_{CCA} = 0.9 V to 1.98 V; V_{CCB} = 0.9 V to 1.98 V (1)	0.7V_{CCI}		0.7V_{CCI}		V
		OE input					
		V_{CCA} = 0.72 V to 1.98 V; V_{CCB} =0.72 V to 1.98 V	0.65V_{CCA}		0.65V_{CCA}		V
V_{IL}	LOW-Level Input Voltage	A or B port					
		V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 0.72 V to 1.98 V		0.3V_{CCA}		0.3V_{CCA}	V
		OE input					
		V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 0.72 V to 1.98 V		0.3V_{CCA}		0.3V_{CCA}	V
V_{OH}	HIGH-Level Output Voltage	I_O = -20 μA (2)					
		A port; V_{CCA} = 0.72 V to 1.98 V	V_{CCO} - 0.285		V_{CCO} - 0.285		V
		B port; V_{CCB} = 0.72 V to 1.98 V	V_{CCO} - 0.285		V_{CCO} - 0.285		V
V_{OL}	LOW-Level Output Voltage	V_I = 0.05 V, I_O = 20 μA (2)					
		A port; V_{CCA} = 0.72 V to 1.98 V		0.3		0.3	V
		B port; V_{CCB} = 0.72 V to 1.98 V		0.3		0.3	V
I_I	Input Leakage Current	OE input; V_I = 0 V to 1.98 V; V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 0.72 V to 1.98 V		±1		±2	μA
I_{OZ}	OFF-State Output Current	A or B port; V_O = 0 V or V_{CCO}; V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 0.72 V to 1.98 V (2)		±1		±2	μA
I_{OFF}	Power Off Leakage Current	A port; V_I or V_O = 0 V to 1.98 V; V_{CCA} =0.72 V to 1.98 V; V_{CCB} = 0.72 V to 1.98 V		±1		±5	μA
		B port; V_I or V_O = 0 V to 1.98 V; V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 0.72 V to 1.98 V		±1		±5	μA
I_{CC}	Supply Current	V_I = 0 V or V_{CCI}; I_O = 0 A (1)					
		$I_{CC(A)}$					
		OE = LOW; V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 0.72 V to 1.98 V		4		10	μA
		OE = HIGH; V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 0.72 V to 1.98 V		4		10	μA
		V_{CCA} = 1.98 V; V_{CCB} = 0 V		4		10	μA
		V_{CCA} = 0 V; V_{CCB} = 1.98 V		-1.5		-10	μA
		$I_{CC(B)}$					
		OE = LOW; V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 0.72 V to 1.98 V		8		15	μA
		OE = HIGH; V_{CCA} = 0.72 V to 1.98 V; V_{CCB} = 0.72 V to 1.98 V		8		15	μA

		V_{CCA} = 1.98 V; V_{CCB} = 0 V		-2		-10	µA
		V_{CCA} = 0 V; V_{CCB} = 1.98 V		5		15	µA

(1) V_{CCI} is the supply voltage associated with the input.
(2) V_{CCO} is the supply voltage associated with the output.
(3) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

8.6 Dynamic Characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C. (1)

SYMBOL	PARAMETER	CONDITIONS	V_{CCB} 1.2 V ± 10 %			V_{CCB} 1.8 V ± 10 %			UNIT
			MIN(2)	TYP(3)	MAX(2)	MIN(2)	TYP(3)	MAX(2)	
V_{CCA} = 0.8 V ± 10 %									
t_{pd}	Propagation Delay	A to B; C_L = 15 pF		4.5			4.4		ns
		B to A; C_L = 15 pF		2.1			1.8		ns
t_{pzl}	Enable Time	OE to A; C_L = 15 pF		7.1			3		ns
	Enable Time	OE to B; C_L = 15 pF		8.6			6.5		ns
t_{pzh}	Enable Time	OE to A; C_L = 15 pF		4.3			3		ns
	Enable Time	OE to B; C_L = 15 pF		145			218		ns
t_{plz}	Disable Time	OE to A; C_L = 15 pF		103			90		ns
		OE to B; C_L = 15 pF		117.5			114.5		ns
t_{phz}	Disable Time	OE to A; C_L = 15 pF		235.1			195.3		ns
		OE to B; C_L = 15 pF		239.7			255.7		ns
t_t	Transition Time	A port; C_L = 15 pF		2.4			0.9		ns
		B port; C_L = 15 pF		2.8			2.5		ns
$t_{sk(o)}$	Output Skew Time	Delta between channels (4)		0.12			0.04		ns
t_W	Pulse Width	Data inputs	37			37			ns
f_{data}	Data Rate		0.064		26	0.064		26	Mbps
V_{CCA} = 1.2 V ± 10 %									
t_{pd}	Propagation Delay	A to B; C_L = 15 pF		1.7			2.4		ns
		B to A; C_L = 15 pF		1.7			1.3		ns
t_{pdc}	Propagation Delay	A to B; C_L = 80 pF	NA	NA	NA		3.8		ns
		B to A; C_L = 30 pF	NA	NA	NA		1.8		ns
t_{pzl}	Enable Time	OE to A; C_L = 15 pF		5.7			5.1		ns
	Enable Time	OE to B; C_L = 15 pF		6.4			5.2		ns
t_{pzh}	Enable Time	OE to A,; C_L = 15 pF		4.3			2.6		ns
	Enable Time	OE to B; C_L = 15 pF		3.7			50.1		ns
t_{plz}	Disable Time	OE to A; C_L = 15 pF		116.9			122.9		ns
		OE to B; C_L = 15 pF		130.4			126.3		ns
t_{phz}	Disable Time	OE to A; C_L = 15 pF		235.2			210.4		ns
		OE to B; C_L = 15 pF		232.9			249.8		ns
t_t	Transition Time	A port; C_L = 15 pF		2.1			0.8		ns
		B port; C_L = 15 pF		2.1			1.9		ns
t_{tc}	Transition Time	A port; C_L = 30 pF	NA	NA	NA		1.2		ns
		B port; C_L = 80 pF	NA	NA	NA		3.2		ns
$t_{sk(o)}$	Output Skew Time	Delta between channels (4)		0.14			0.06		ns
t_W	Pulse Width	Data inputs	15			13.5			ns
f_{data}	Data Rate		0.064		52	0.064		52	Mbps

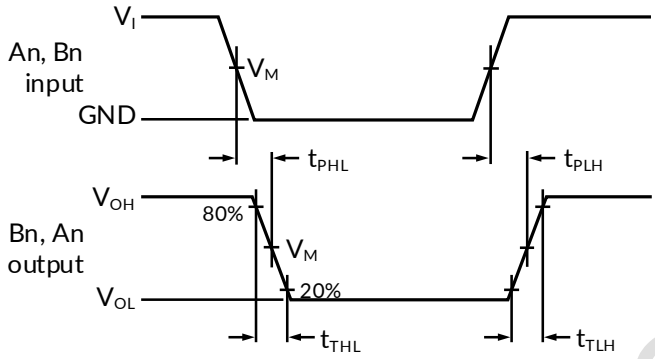
Dynamic Characteristics (Continue)

SYMBOL	PARAMETER	CONDITIONS	V_{CCB}			UNIT
			1.8 V ± 10 %			
			MIN(2)	TYP(3)	MAX(2)	
V_{CCA} = 1.8 V ± 10 %						
t_{pd}	Propagation Delay	A to B; C_L = 15 pF		1.3		ns
		B to A; C_L = 15 pF		1.3		ns
t_{pzl}	Enable Time	OE to A; C_L = 15 pF		2.7		ns
	Enable Time	OE to B; C_L = 15 pF		5.2		ns
t_{pzh}	Enable Time	OE to A; C_L = 15 pF		2.9		ns
	Enable Time	OE to B; C_L = 15 pF		2.5		ns
t_{plz}	Disable Time	OE to A; C_L = 15 pF		123.6		ns
		OE to B; C_L = 15 pF		124.8		ns
t_{phz}	Disable Time	OE to A; C_L = 15 pF		222.8		ns
		OE to B; C_L = 15 pF		242.6		ns
t_t	Transition Time	A port; C_L = 15 pF		1.7		ns
		B port; C_L = 15 pF		1.7		ns
$t_{sk(o)}$	Output Skew Time	Delta between channels (4)		0.07		ns
t_W	Pulse Width	Data inputs	13.5			ns
f_{data}	Data Rate		0.064		52	Mbps

(1) t_{pd} is the same as t_{PLH} and t_{PHL}; t_t is the same as t_{THL} and t_{TLH}.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(4) Skew between any two outputs of the same package switching in the same direction. One channel is not always faster than the other.

9 PARAMETER MEASUREMENT INFORMATION

Figure 1 illustrates the propagation delay times from data input (An, Bn) to data output (Bn, An), while Figure 2 shows the test circuit used for measuring switching times. Table 1 describes the measurement points, and Table 2 provides the test data.



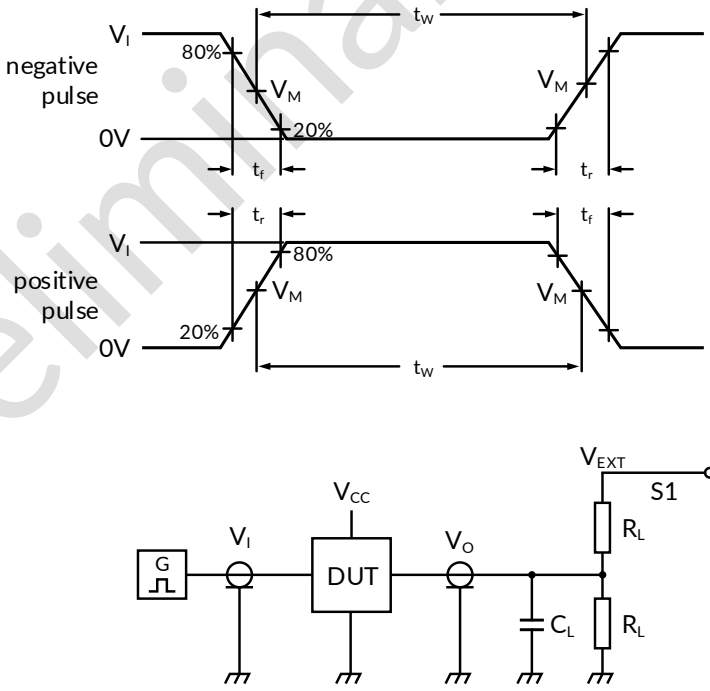
Measurement points are given in Table 1.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 1. Data input (An, Bn) to data output (Bn, An) propagation delay times

Table 1. Measurement Points

V_{CCI} is the supply voltage associated with the input and V_{CCO} is the supply voltage associated with the output.

Supply Voltage	Input	Output		
V_{CCO}	V_M	V_M	V_X	V_Y
0.8 V ± 10 %	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.08 V	V_{OH} - 0.08 V
1.2 V ± 10 %	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.12 V	V_{OH} - 0.12 V
1.8 V ± 10 %	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.18 V	V_{OH} - 0.18 V



Test data is given in Table 2.
All input pulses are supplied by generators having the following characteristics: PRR ≤ 26 MHz; Z_O = 50 Ω; dV/dt ≥ 1.0 V/ns.
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
V_{EXT} = External voltage for measuring switching times.

Figure 2. Test circuit for measuring switching times

Table 2. Test data

Supply voltage		Input		Load		V_{EXT}		
V_{CCA}	V_{CCB}	V_I (1)	Δt/ΔV	C_L	R_L (2)	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ} (3)
0.72 V to 1.98 V	0.72 V to 1.98 V	V_{CCI}	≤ 1.0 ns/V	15 pF	50 kΩ, 1 MΩ	open	open	$2V_{CCO}$

(1) V_{CCI} is the supply voltage associated with the input.
(2) For measuring data rate, pulse width, propagation delay, and output rise and fall measurements, R_L = 1MΩ; for measuring enable and disable times, R_L =50 kΩ.
(3) V_{CCO} is the supply voltage associated with the output.

10 APPLICATION AND IMPLEMENTATION

Information in the following applications sections is not part of the RUNIC component specification, and RUNIC does not warrant its accuracy or completeness. RUNIC's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Voltage level-translation applications. The RS0322 can be used to interface between devices or systems operating at different supply voltages. See Figure 3, Figure 4, Figure 5, and Figure 6 for a typical operating circuit using the RS0322.

10.2 Application Block Diagram

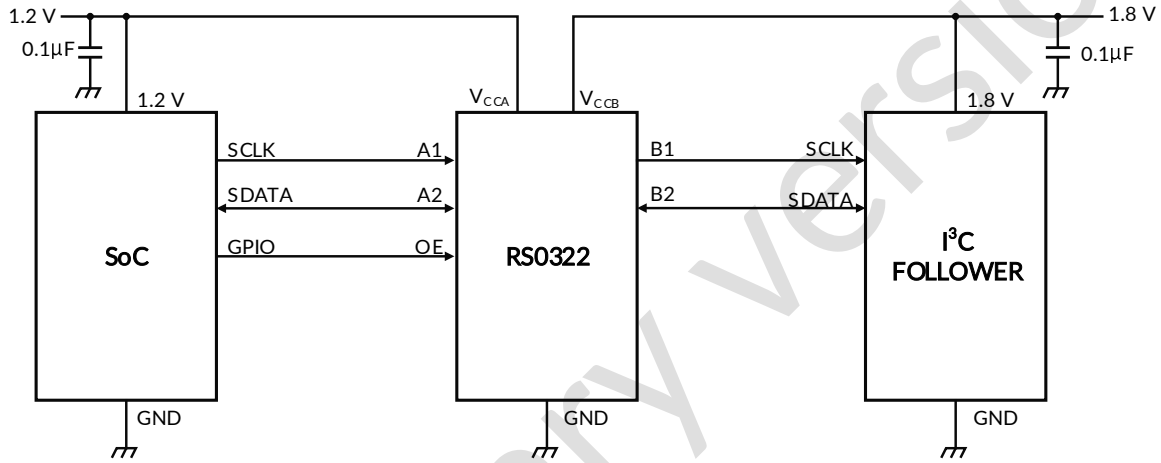


Figure 3. I³C Application Block Diagram

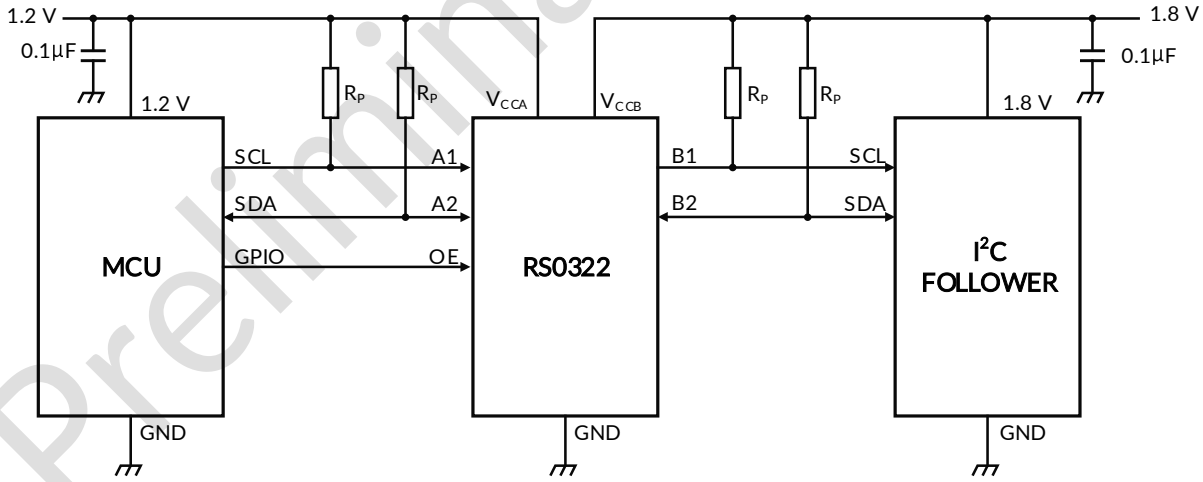


Figure 4. I²C Application Block Diagram

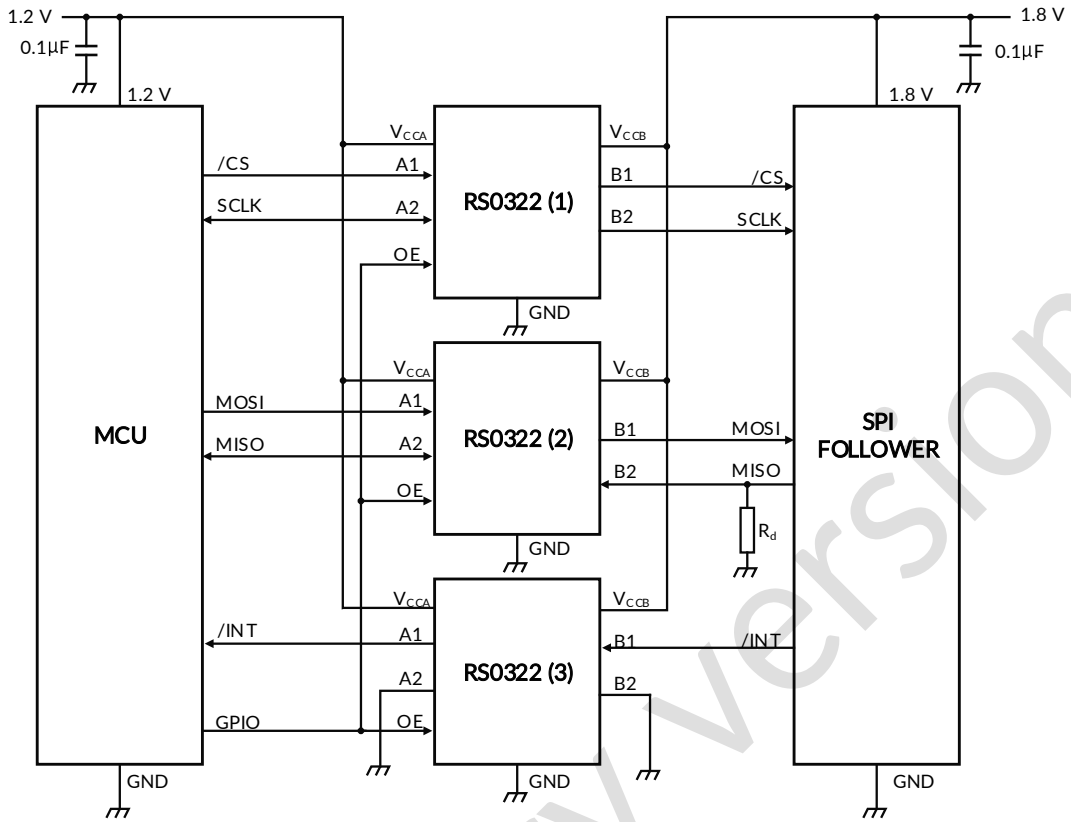


Figure 5. SPI Application Block Diagram

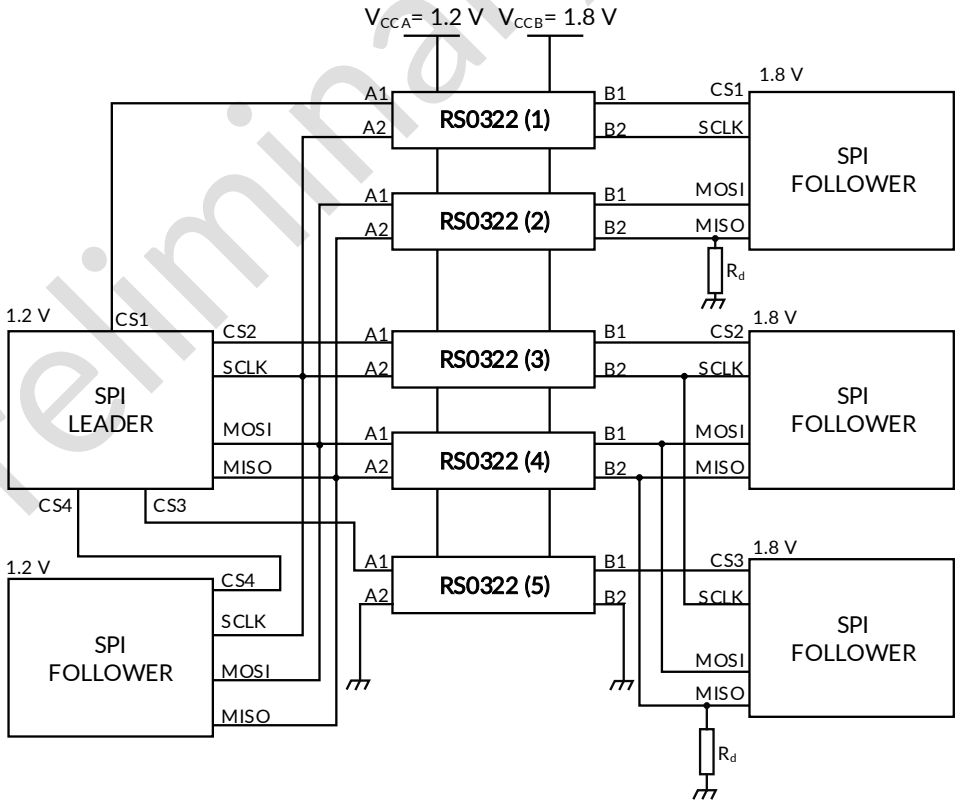


Figure 6. Complex SPI Block Diagram

10.3 Architecture

The architecture uses edge-rate accelerator circuitry (for both the high-to-low and low-to-high), N-channel pass gate transistor and a pullup resistor (to provide DC-bias and drive capabilities) to meet these requirements. The design is directionless and does not need a direction control signal. The implementation supports both low-speed open-drain operation as well as high-speed push-pull operation. The N-channel pass gate transistor is on only during the low input cycle and is off during the high input cycle.

10.4 Input Driver Requirements

The continuous DC-current sinking or sourcing capability is determined by the external system-level; open-drain or push-pull drivers that are interfaced to the RS0322 IO pins.

The high bandwidth of these IO circuits used to facilitate this fast change from an input to an output and an output to an input, they have a modest sourcing capability of hundreds of micro-amperes, as determined by the pullup resistor.

The fall time of a signal depends on the edge-rate and output impedance of the external driving the RS0322 data IOs, and the capacitive loading at the data lines.

10.5 Power Up And Power-Down

This section outlines the power up and power-down sequence of RS0322.

10.5.1 Power Up Sequence

Turn on V_{CCB} first to the recommended operating voltage range, then turn on V_{CCA}.

10.5.2 Power-Down Sequence

Turn off V_{CCB} first, and after it is completely off, then turn off V_{CCA}. The different sequencing of each power supply does not damage the device during the power up operation.

The RS0322 includes circuitry that disables all output ports and puts the device into a power-down mode when either V_{CCA} or V_{CCB} is switched off.

10.6 Enable and Disable

An output enable input (OE) is used to enable/disable the device when both V_{CCA} and V_{CCB} are in recommended operating conditions. Setting OE = LOW causes all I/Os to assume the high-impedance OFF-state. The disable time (t_{dis} with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time (t_{en}) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power up or power down, pin OE should be tied to GND, OE pin should not be left floating in any condition.

OE V_{IL} and V_{IH} are referenced to V_{CCA}. The OE can be controlled by an external device that is powered by either V_{CCA} or V_{CCB}. As V_{CCB} is required to be greater than V_{CCA}, the OE pin has been designed to withstand a voltage equal to V_{CCB} (up to 1.98 V per recommended functional voltage range).

11 LAYOUT

11.1 Layout Guidelines

To ensure reliability of the device, the following common printed-circuit board (PCB) layout guidelines are recommended:

- Bypass capacitors must be used on power supplies and must be placed as close as possible to V_{CCA}, V_{CCB}, and GND pins.
- Short trace lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration, approximately 8 ns, ensuring that any reflection encounters low impedance at the source driver.

11.2 Layout Example

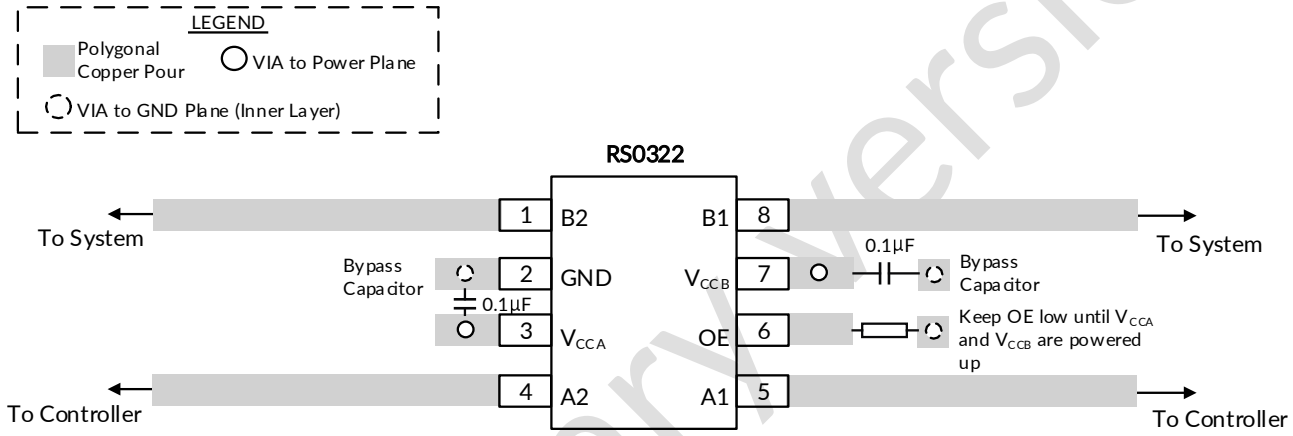
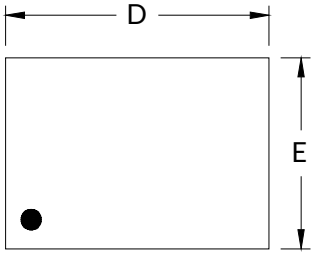


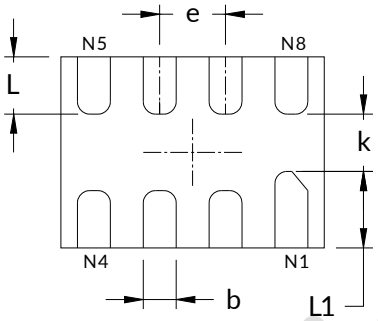
Figure 7. Layout Example

12 PACKAGE OUTLINE DIMENSIONS

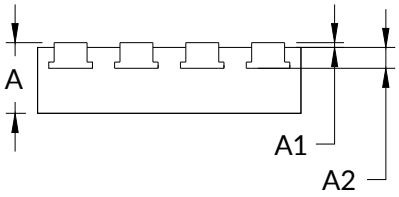
XDFN1.4X1-8 (3)



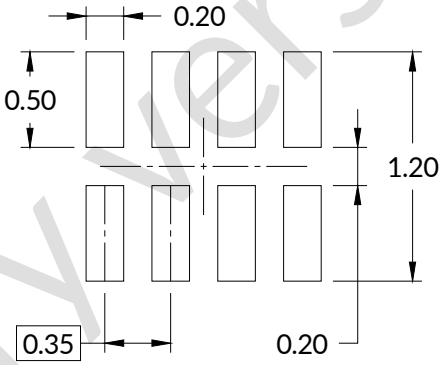
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.340	0.400	0.013	0.016
A1	0.000	0.050	0.000	0.002
A2	0.110 REF (2)		0.004 REF (2)	
D (1)	1.350	1.450	0.053	0.057
E (1)	0.950	1.050	0.037	0.041
k	0.200 MIN		0.008 MIN	
b	0.150	0.200	0.006	0.008
e	0.350 TYP		0.014 TYP	
L	0.250	0.350	0.010	0.014
L1	0.350	0.450	0.014	0.018

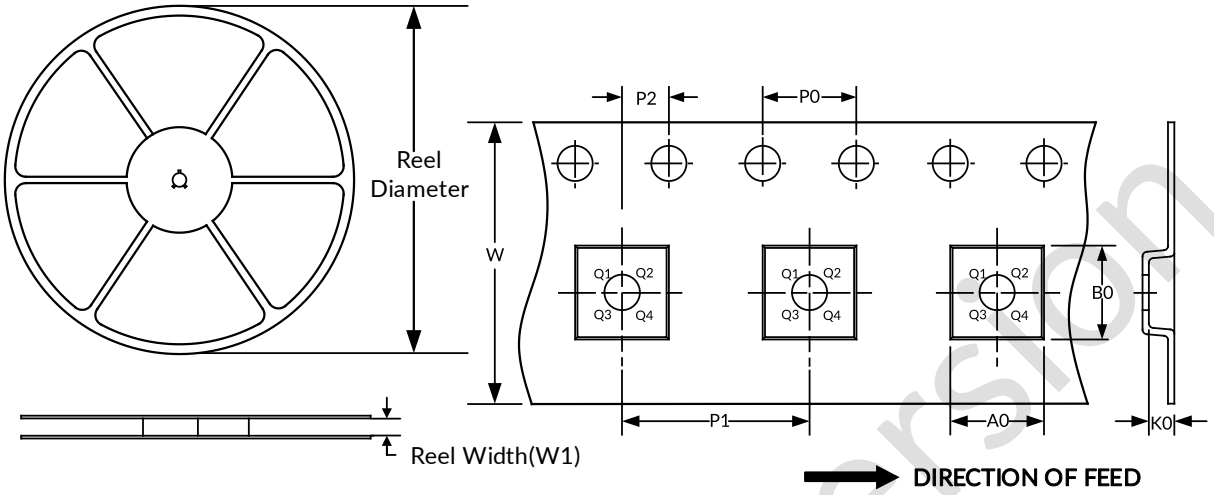
NOTE:

1. Plastic or metal protrusions of 0.075mm maximum per side are not included.
2. REF is the abbreviation for Reference.
3. This drawing is subject to change without notice.

13 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
XDFN1.4X1-8	7”	9.5	1.2	1.6	0.5	4.0	4.0	2.0	8.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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