16-Bit, Ultralow-Glitch, Voltage-Output Digital-to-Analog Converter

1 FEATURES

- **Relative Accuracy: ±6 LSB**
- **Glitch Energy: 1 nV-s**
- **MicroPower Operation: 160 µA at 2.7 V**
- **Power-On Reset to Zero**
- **Power Supply: 2.7 V to 5.5 V**
- **16-Bit Monotonic**
- **Settling Time: 4 µs to ± 0.003% FSR**
- **Low-Power Serial Interface with Schmitt-Triggered Inputs**
- **On-Chip Output Buffer Amplifier with Rail-to-Rail Operation**
- **Power-Down Capability**
- **Binary Input**
- **$\overline{\text{SYNC}}$ Interrupt Facility**

2 APPLICATIONS

- **Multichannel System Monitoring**
- **Battery-Powered Equipment**
- **Process Control**
- **Data Acquisition Systems**
- **Closed-Loop Servo-Control**
- **PC Peripherals**
- **Portable Instrumentation**
- **Programmable Attenuation**

3 DESCRIPTIONS

The RS1361 is a small, low-power, voltage output, 16-bit digital-to-analog converter (DAC). It is monotonic, provides good linearity, and minimizes undesired code-to-code transient voltages. The RS1361 uses a versatile 3-wire serial interface that operates at clock rates to 30 MHz and is compatible with standard SPI™, QSPI™, Microwire™, and digital signal processor (DSP) interfaces.

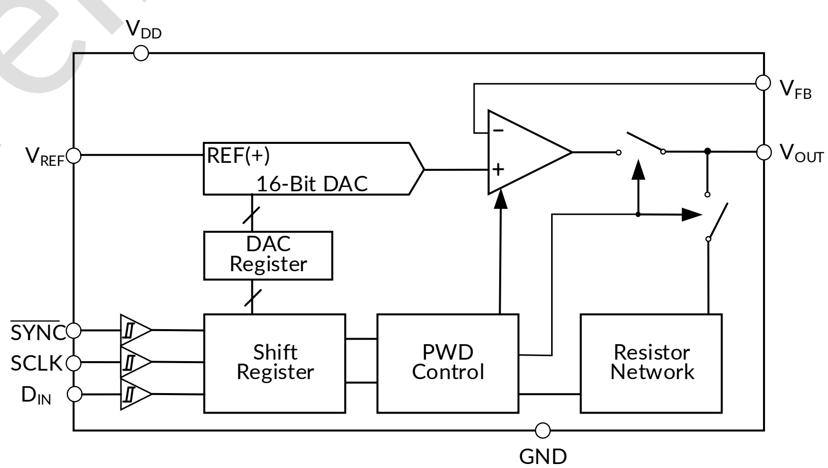
The RS1361 requires an external reference voltage to set its output range. The RS1361 incorporates a power-on-reset circuit that ensures the DAC output powers up at 0 V and remains there until a valid write takes place to the device. The RS1361 contains a power-down feature, accessed over the serial interface, that reduces the current consumption of the device to 10 nA at 5 V.

The low-power consumption of this device in normal operation makes it ideally suited for portable, battery-operated equipment. The power consumption is 0.4 mW at 2.7 V, reducing to less than 0.1 µW in power-down mode.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS1361	MSOP8	3.00mm×3.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram

Table of Contents

4 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

Version	Change Date	Change Item
A.0	2025/07/08	Preliminary version completed
A.0.1	2026/01/23	1. Zero-Code Error (Typical): ±2mV (previously ±3mV). 2. Full-Scale Error (Typical): ±0.06% FSR (previously ±0.1% FSR). 3. PSRR (Typical): 0.15mV/V (previously 0.45mV/V). 4. Added Output Noise test item (significantly reduced from previous version). 5. The static parameter diagram has been modified.
A.0.2	2026/03/25	Add parameter control for upper and lower limits.

5 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING (2)	MSL (3)	PACKAGE OPTION
RS1361	RS1361XM	-40°C ~+125°C	MSOP8	RS1361	MSL1	Tape and Reel, 4000

NOTE:

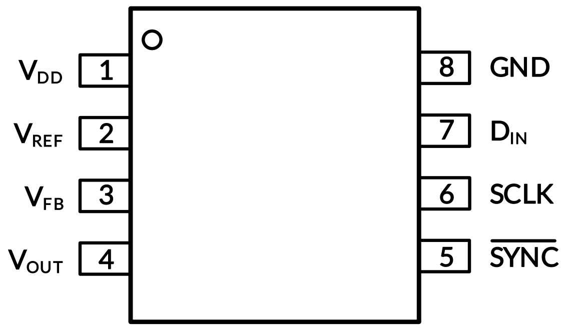
(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

6 PIN CONFIGURATION AND FUNCTIONS

TOP VIEW



MSOP8

PIN FUNCTIONS

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
D_{IN}	7	I	Serial data input. Data is clocked into the 24 bit input shift register on each falling edge of the serial clock input. Schmitt-Trigger logic input.
GND	8	GND	Ground reference point for all circuitry on the part.
SCLK	6	I	Serial clock input. Data can be transferred at rates up to 30 MHz Schmitt-Trigger logic input.
$\overline{SYNC}$	5	I	Level-triggered control input (active LOW). This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes LOW, it enables the input shift register and data is transferred in on the falling edges of the following clocks. The DAC is up dated following the 24th clock (unless $\overline{SYNC}$ is taken HIGH before this edge, in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the RS1361). Schmitt-Trigger logic input.
V_{DD}	1	PWR	Power supply input, 2.7 V to 5.5 V.
V_{FB}	3	I	Feedback connection for the output amplifier. For voltage output operation, tie to V_{OUT} externally.
V_{OUT}	4	O	Analog output voltage from DAC. The output amplifier has rail-to-rail operation.
V_{REF}	2	I	Reference voltage input.

(1) I=Input, O=Output.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [(1)]

		MIN	MAX	UNIT
Input voltage	GND	-0.3	6	V
Digital input voltage	GND	-0.3	V_{DD}+0.3	V
Output voltage	GND	-0.3	V_{DD}+0.3	V
Operating temperature		-40	125	°C
Junction temperature, T_J [(2)]			150	°C
Storage temperature, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{θJA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{θJA}$. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), per ANSI/ESDA/JEDEC JS-001 [(1)]	±2000	V
		Charged-Device Model (CDM), per JEDEC specification JESD22-C101 [(2)]	±500	V

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	Supply voltage (V_{DD} to GND)	2.7		5.5	V
	Digital input voltage (D_{IN}, SCLK, and $\overline{SYNC}$)	0		V_{DD}	V
V_{REF}	Reference input voltage	0		V_{DD}	V
V_{FB}	Output amplifier feedback input		V_{OUT}		V
T_A	Operating ambient temperature	-40		125	°C

7.4 Thermal Information

THERMAL METRIC [(1)]		RS1361	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	206	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	44	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	94.2	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	10.2	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	92.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

V_{DD} = 2.7 V to 5.5 V and −40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
STATIC PERFORMANCE						
Resolution			16			Bits
Relative Accuracy		Measured by line passing through codes 485 and 64741 at V_{REF} = 5 V, codes 970 and 63947 at V_{REF} = 2.5 V		±6	±12	LSB
Differential Nonlinearity				±0.5	±1	LSB
Zero-Code Error		Measured by line passing through codes 485 and 64741		±2	±12	mV
Full-Scale Error				±0.06%	±0.3%	FSR
Gain Error				±0.06%	±0.15%	FSR
Zero-Code Error Drift				±1		µV/°C
Gain Temperature Coefficient				±1		ppm of FSR/°C
PSRR	Power-Supply Rejection Ratio	R_L = 2 kΩ , C_L = 200 pF		0.15		mV/V
OUTPUT CHARACTERISTICS						
Output Voltage Range			0		V_{REF}	V
Output Voltage Settling Time		To ± 0.003% FSR, 0200h to FD00h, R_L = 2 kΩ, 0 pF < C_L < 200 pF		4		µs
		R_L = 2 kΩ , C_L =50pF		4		µs
Slew Rate				1.7		V/µs
Capacitive Load Stability		R_L = ∞		470		pF
		R_L = 2 kΩ		1000		pF
Output Noise		0.1 Hz to 10 Hz		70		µVp-p
Code Change Glitch Impulse		1 LSB change around major carry		1		nV-s
Digital Feedthrough		50 kΩ series resistance on digital lines		0.1		nV-s
DC Output Impedance		At mid-code input		1		Ω
Short-Circuit Current		V_{DD} = 5 V		60		mA
		V_{DD} = 3 V		60		mA

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

Electrical Characteristics (continued)

V_{DD} = 2.7 V to 5.5 V and –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power-up time		Coming out of power-down mode, V_{DD} = 5 V		12		µs
		Coming out of power-down mode, V_{DD} = 3 V		13		µs
AC PERFORMANCE						
SNR	Signal-to-Noise Ratio	BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz, 1st 19 harmonics removed for SNR calculation		93		dB
THD	Total Harmonic Distortion	BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz, 1st 19 harmonics removed for SNR calculation		-74		dB
SFDR	Spurious-Free Dynamic Range	BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz, 1st 19 harmonics removed for SNR calculation		74		dB
SINAD	Signal to Noise and Distortion	BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz, 1st 19 harmonics removed for SNR calculation		74		dB
REFERENCE INPUT						
Reference Current		V_{REF} = V_{DD} = 5 V		40		µA
		V_{REF} = V_{DD} = 3.6 V		30		µA
Reference Input Range			0		V_{DD}	V
Reference Input Impedance				125		kΩ
LOGIC INPUTS						
Input Current				±1		µA
V_{IL}	Input LOW Voltage	3 V ≤ V_{DD} ≤ 5.5 V			0.3×V_{DD}	V
		2.7 V ≤ V_{DD} < 3 V			0.1×V_{DD}	V
V_{IH}	Input HIGH Voltage	3 V ≤ V_{DD} ≤ 5.5 V	0.7×V_{DD}			V
		2.7 V ≤ V_{DD} < 3 V	0.9×V_{DD}			V
Pin Capacitance				3		pF
POWER REQUIREMENTS						
V_{DD}	Supply Voltage		2.7		5.5	V
I_{DD}	Supply Current	Normal mode, input code = 32768, no load, does not include reference current: V_{DD} = 3.6 V to 5.5 V, V_{IH} = V_{DD} and V_{IL} = GND		180	250	µA
		Normal mode, input code = 32768, no load, does not include reference current: V_{DD} = 2.7 V to 3.6 V, V_{IH} = V_{DD} and V_{IL} = GND		160		µA
		All power-down mode, input code = 32768, no load, does not include reference current: V_{DD} = 3.6 V to 5.5 V		0.1		µA
		All power-down mode, input code = 32768, no load, does not include reference current: V_{DD} = 2.7 V to 3.6 V		0.01		µA
I_{OUT}/I_{DD}	Power Efficiency	I_{LOAD} = 2 mA, V_{DD} = 5 V		90%		
Specified Performance Temperature			-40		125	°C

7.6 Timing Characteristics

V_{DD} = 2.7 V to 5.5 V, all specifications –40°C to 125°C (unless otherwise noted) (1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1 (3)	SCLK cycle time	V_{DD} = 2.7 V to 3.6 V	50			ns
		V_{DD} = 3.6 V to 5.5 V	33			
t_2	SCLK HIGH time	V_{DD} = 2.7 V to 3.6 V	13			ns
		V_{DD} = 3.6 V to 5.5 V	13			
t_3	SCLK LOW time	V_{DD} = 2.7 V to 3.6 V	22.5			ns
		V_{DD} = 3.6 V to 5.5 V	13			
t_4	$\overline{SYNC}$ to SCLK rising edge setup time	V_{DD} = 2.7 V to 3.6 V	0			ns
		V_{DD} = 3.6 V to 5.5 V	0			
t_5	Data setup time	V_{DD} = 2.7 V to 3.6 V	5			ns
		V_{DD} = 3.6 V to 5.5 V	5			
t_6	Data hold time	V_{DD} = 2.7 V to 3.6 V	4.5			ns
		V_{DD} = 3.6 V to 5.5 V	4.5			
t_7	24th SCLK falling edge to $\overline{SYNC}$ rising edge	V_{DD} = 2.7 V to 3.6 V	0			ns
		V_{DD} = 3.6 V to 5.5 V	0			
t_8	Minimum $\overline{SYNC}$ HIGH time	V_{DD} = 2.7 V to 3.6 V	50			ns
		V_{DD} = 3.6 V to 5.5 V	33			
t_9	24th SCLK falling edge to $\overline{SYNC}$ falling edge	V_{DD} = 2.7 V to 5.5 V	100			ns

(1) All input signals are specified with t_R = t_F = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH}) / 2.
(2) See Figure 1.
(3) Maximum SCLK frequency is 30 MHz at V_{DD} = 3.6 V to 5.5 V and 20 MHz at V_{DD} = 2.7 V to 3.6 V.

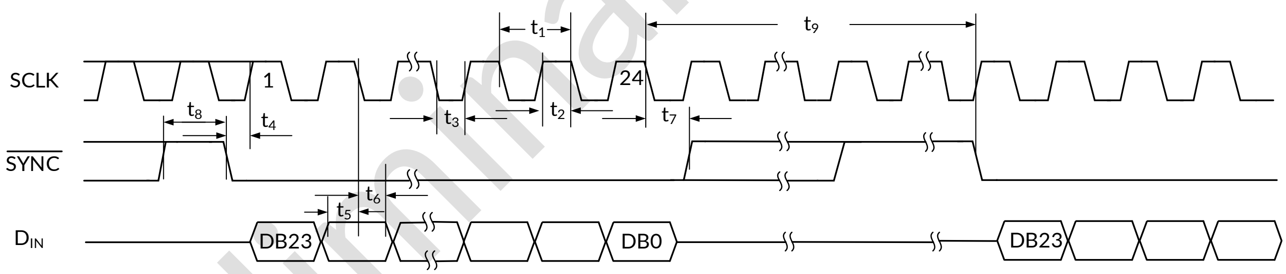


Figure 1. Serial Write Operation

7.7 Typical Characteristics

7.7.1 V_{DD}=5.5V

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A=25°C (unless otherwise noted)

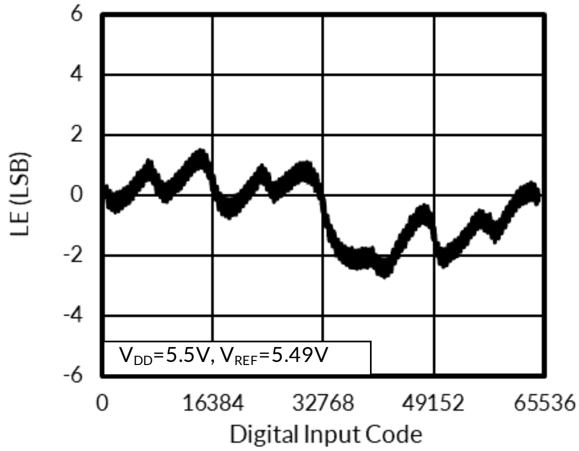


Figure 2. Linearity Error vs Digital Input Code

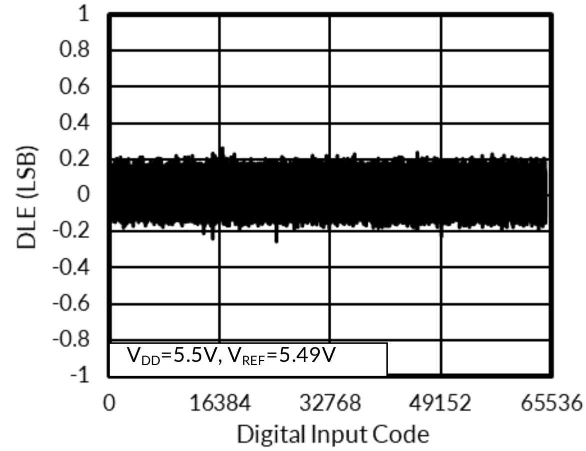


Figure 3. Differential Linearity Error vs Digital Input Code

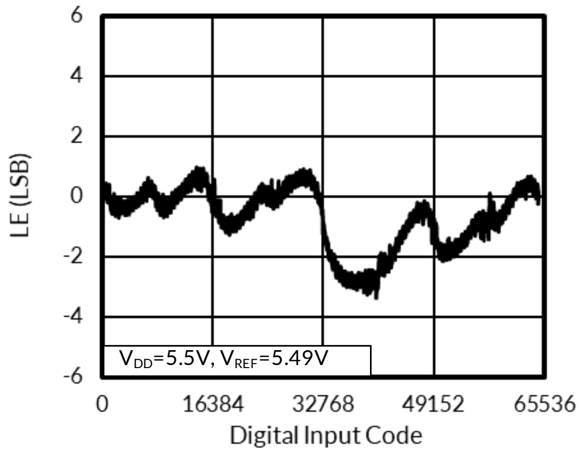


Figure 4. Linearity Error vs Digital Input Code (125°C)

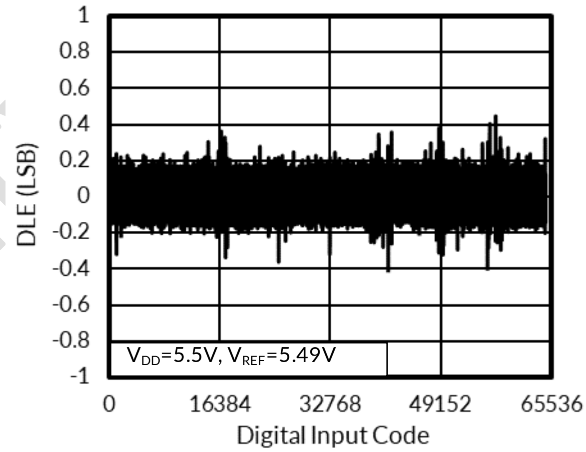


Figure 5. Differential Linearity Error vs Digital Input Code (125°C)

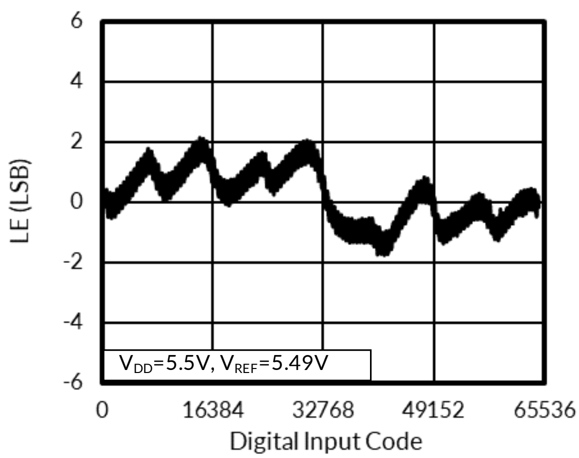


Figure 6. Linearity Error vs Digital Input Code (-40°C)

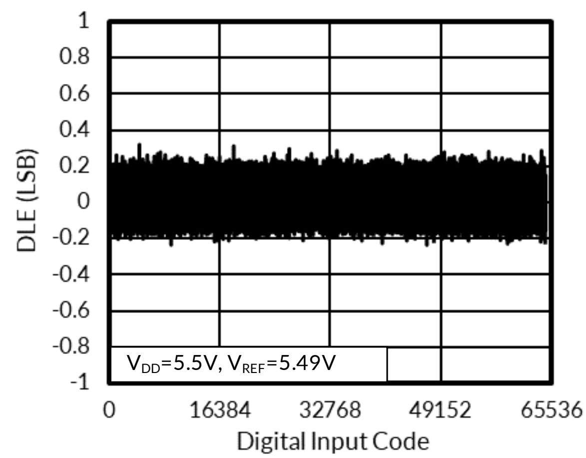


Figure 7. Differential Linearity Error vs Digital Input Code (-40°C)

V_{DD} = 5.5 V (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A=25°C (unless otherwise noted)

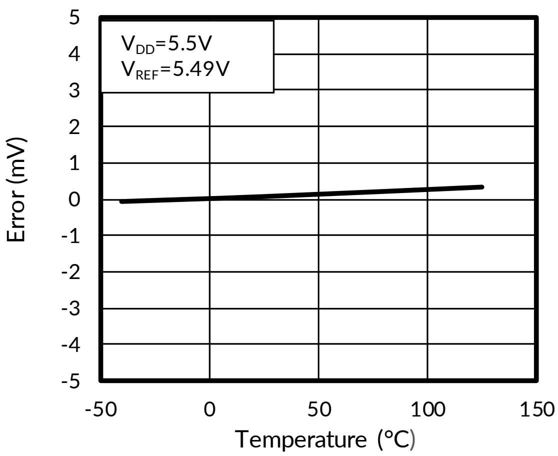


Figure 8. Zero-Scale Error vs Temperature

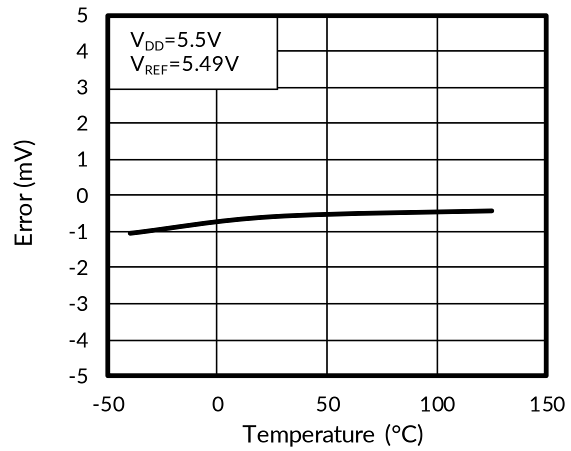


Figure 9. Full-Scale Error vs Temperature

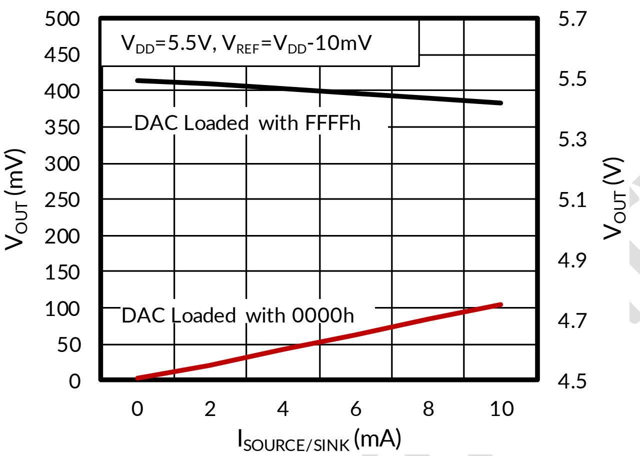


Figure 10. Source and Sink Current Capability

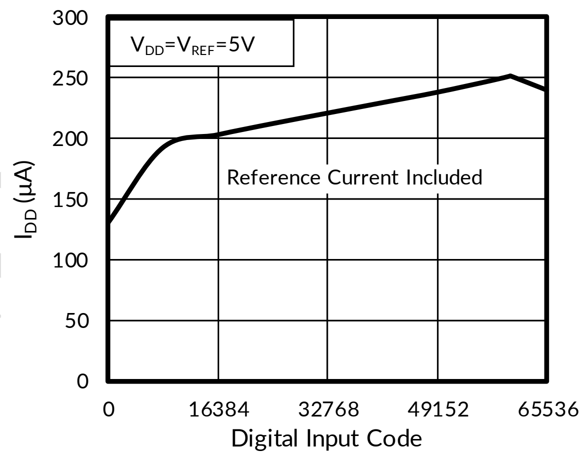


Figure 11. Supply Current vs Digital Input Code

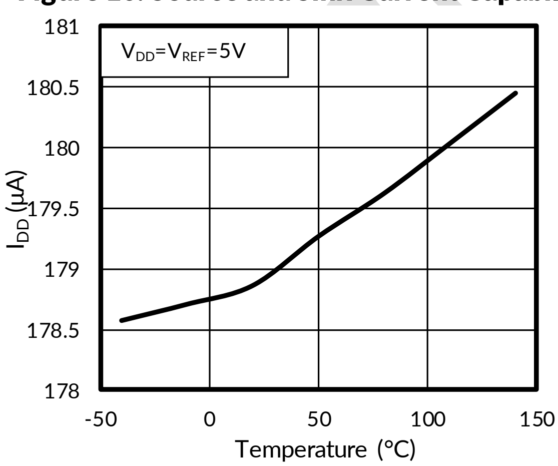


Figure 12. Power-Supply Current vs Temperature

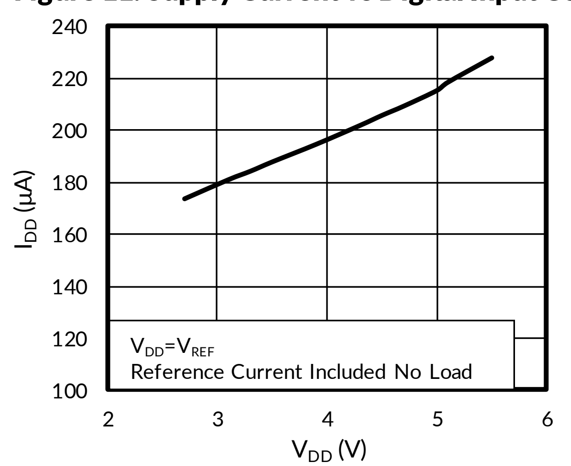


Figure 13. Supply Current vs Supply Voltage

V_{DD} = 5.5 V (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A=25°C (unless otherwise noted)

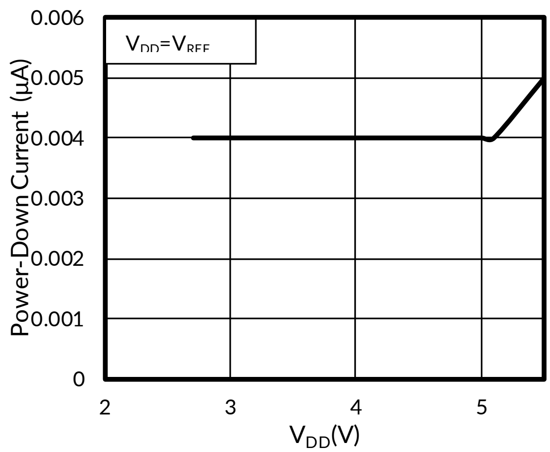


Figure 14. Power-Down Current vs Supply Voltage

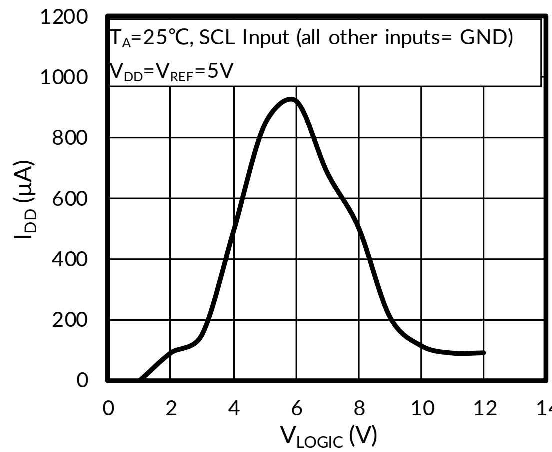


Figure 15. Supply Current vs Logic Input Voltage

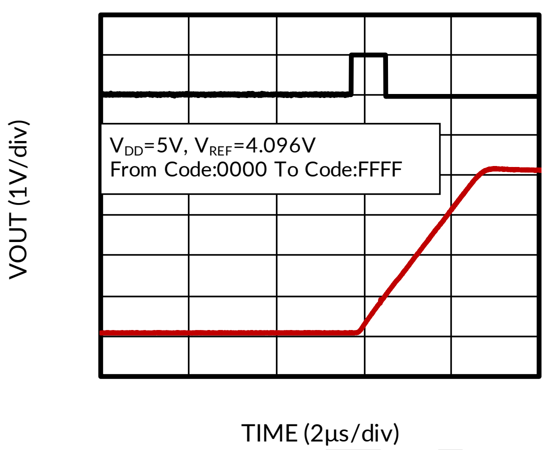


Figure 16. Full-Scale Settling Time, 5-V Rising Edge

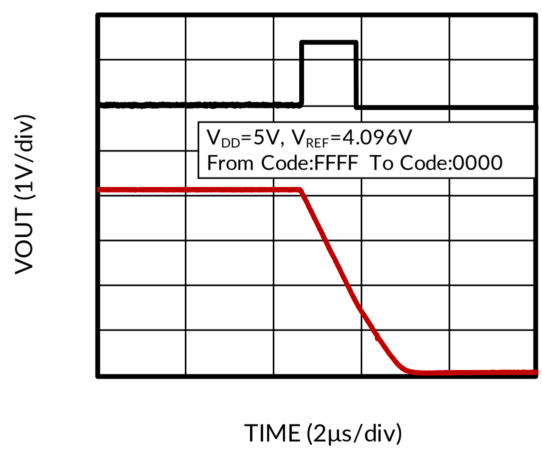


Figure 17. Full-Scale Settling Time, 5-V Falling Edge

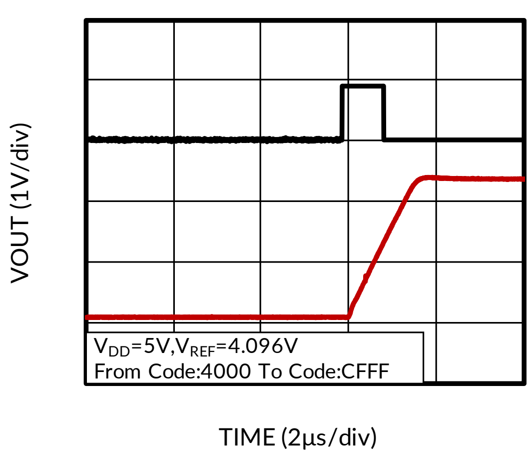


Figure 18. Half-Scale Settling Time, 5-V Rising Edge

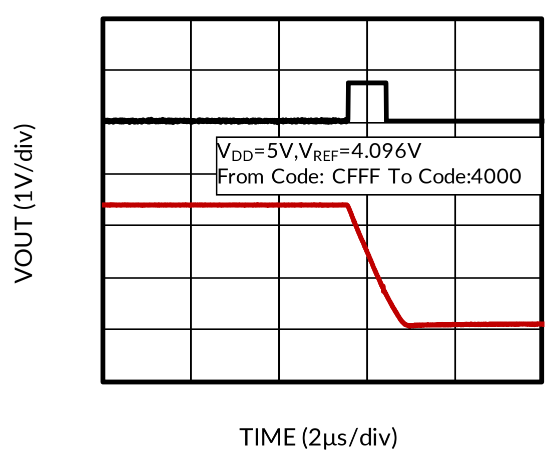


Figure 19. Half-Scale Settling Time, 5-V Falling Edge

V_{DD} = 5.5 V (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A=25°C (unless otherwise noted)

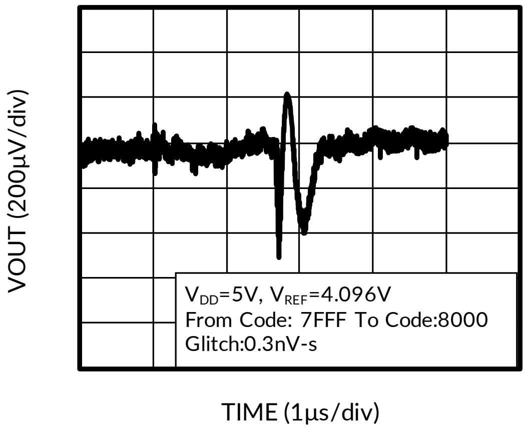


Figure 20. Glitch Energy: 5-V, 1-LSB Step, Rising Edge

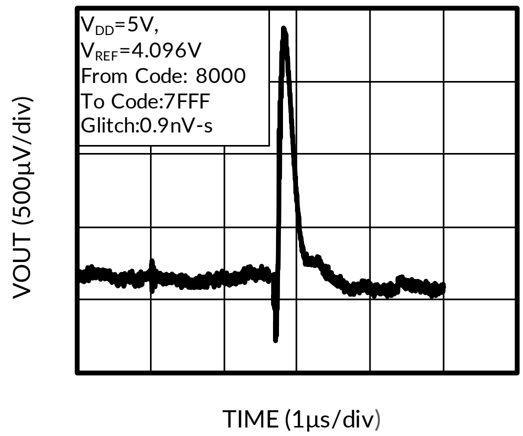


Figure 21. Glitch Energy: 5-V, 1-LSB Step, Falling Edge

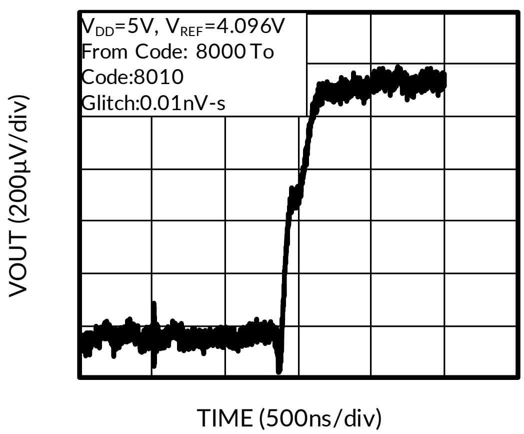


Figure 22. Glitch Energy: 5-V, 16-LSB Step, Rising Edge

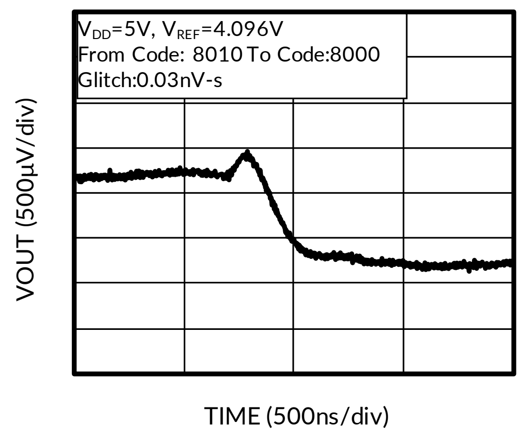


Figure 23. Glitch Energy: 5-V, 16-LSB Step, Falling Edge

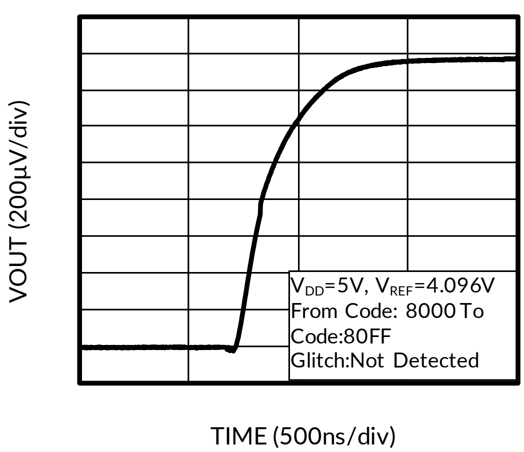


Figure 24. Glitch Energy: 5-V, 256-LSB Step, Rising Edge

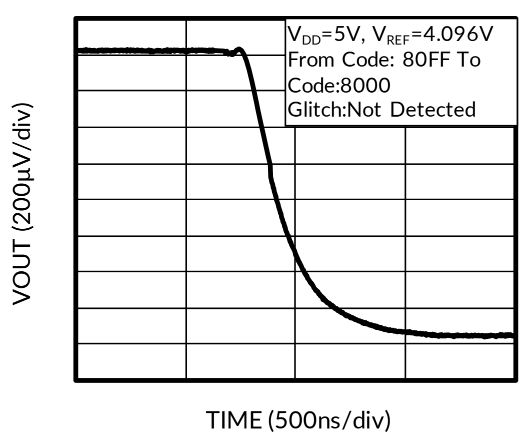


Figure 25. Glitch Energy: 5-V, 256-LSB Step, Falling Edge

V_{DD} = 5.5 V (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A=25°C (unless otherwise noted)

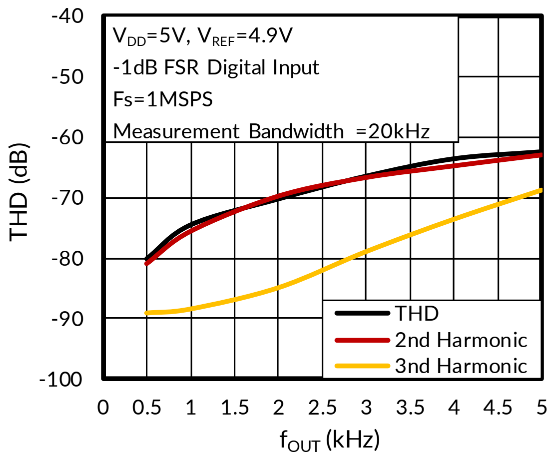


Figure 26. Total Harmonic Distortion vs Output Frequency

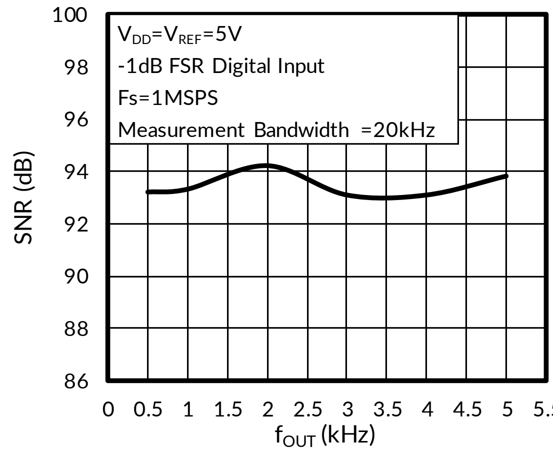


Figure 27. Signal-to-Noise Ratio vs Output Frequency

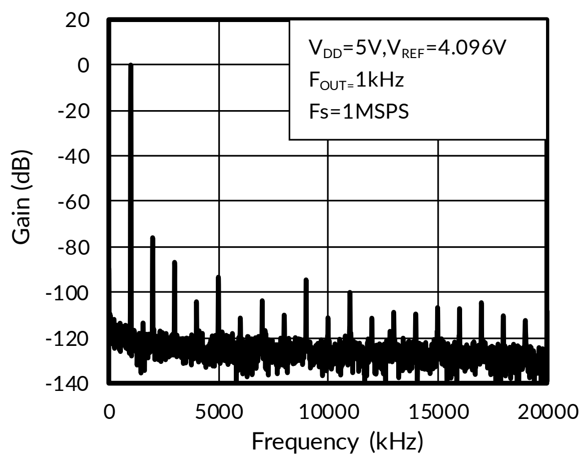


Figure 28. Power Spectral Density

7.7.2 V_{DD} =2.7V

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A=25°C (unless otherwise noted)

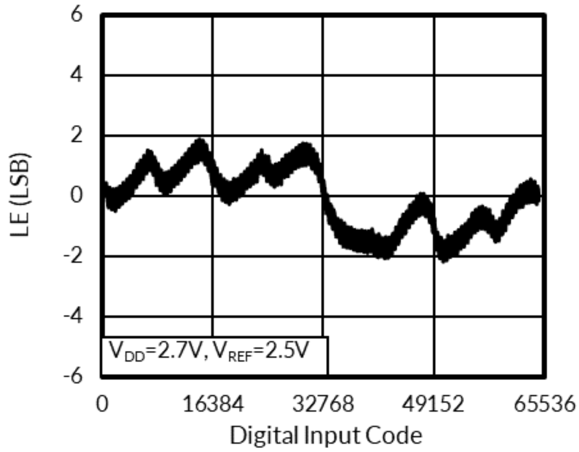


Figure 29. Linearity Error vs Digital Input Code

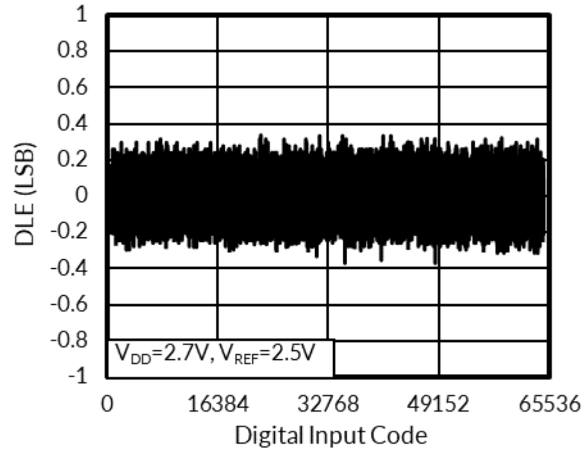


Figure 30. Differential Linearity Error vs Digital Input Code

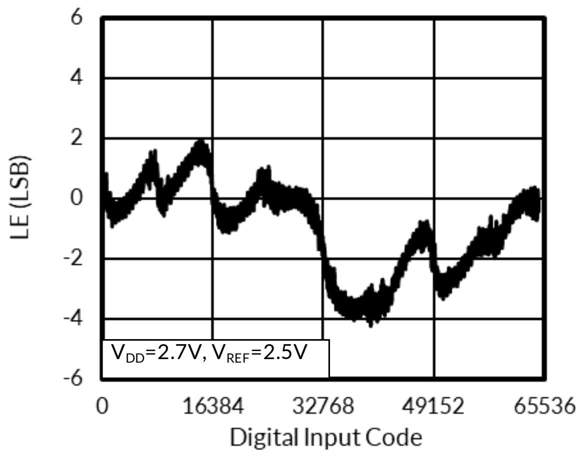


Figure 31. Linearity Error vs Digital Input Code (125°C)

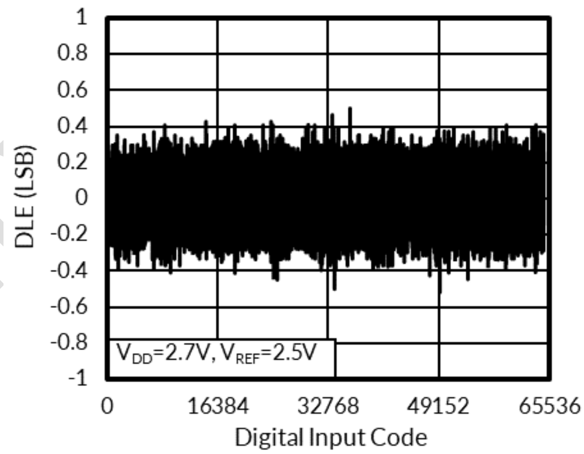


Figure 32. Differential Linearity Error vs Digital Input Code (125°C)

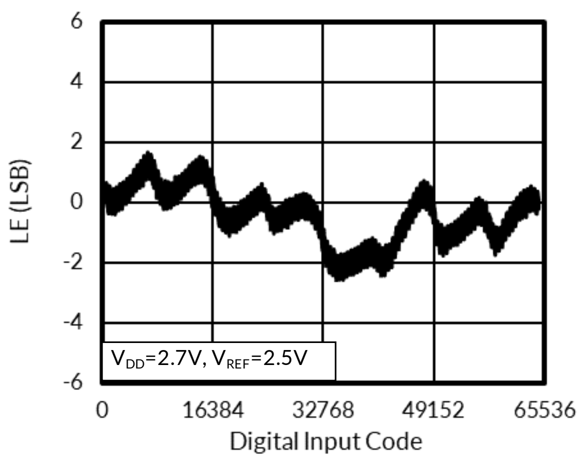


Figure 33. Linearity Error vs Digital Input Code (-40°C)

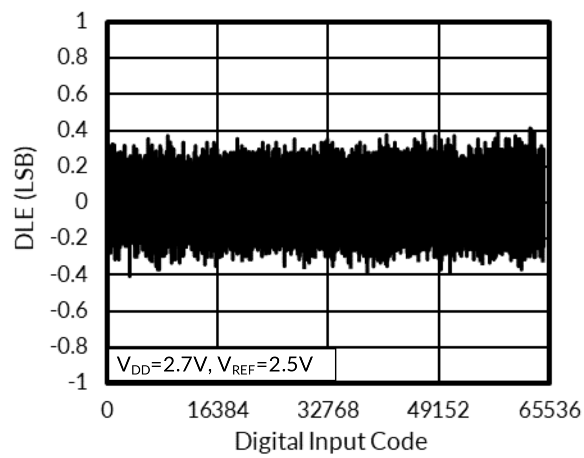


Figure 34. Differential Linearity Error vs Digital Input Code (-40°C)

V_{DD} =2.7V (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A=25°C (unless otherwise noted)

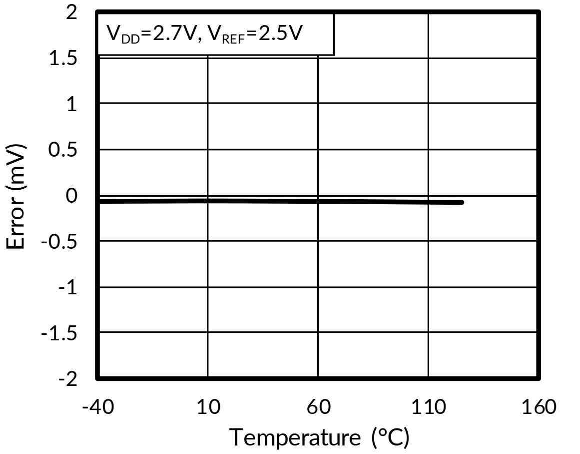


Figure 35. Zero-Scale Error vs Temperature

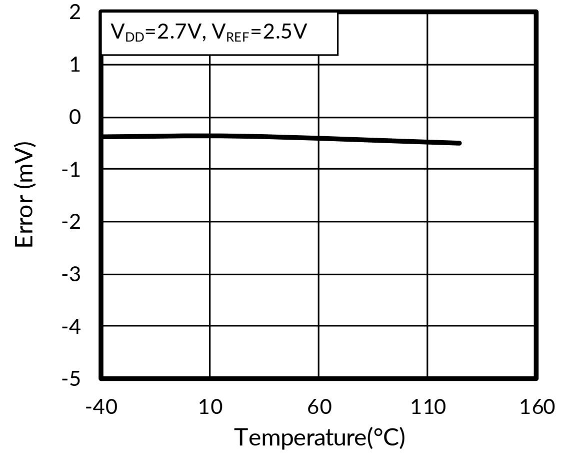


Figure 36. Full-Scale Error vs Temperature

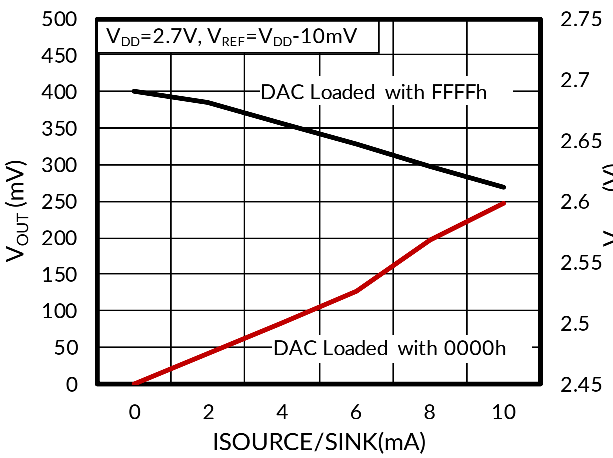


Figure 37. Source and Sink Current Capability

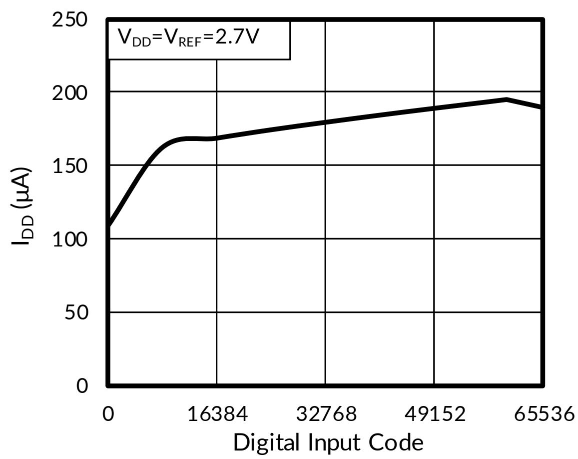


Figure 38. Supply Current vs Digital Input Code

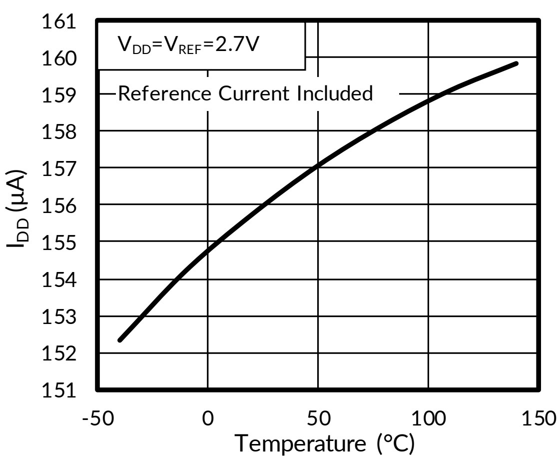


Figure 39. Power-Supply Current vs Temperature

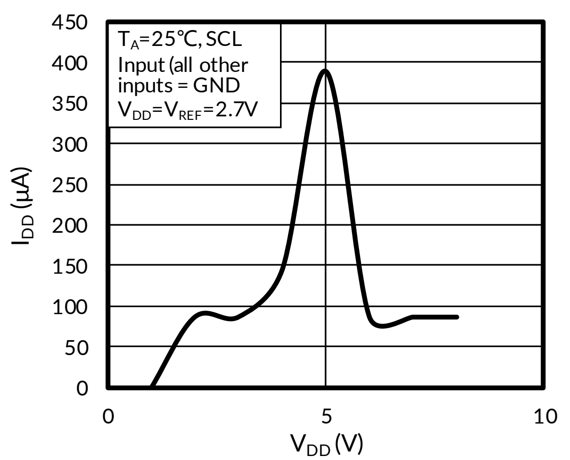


Figure 40. Supply Current vs Logic Input Voltage

V_{DD} =2.7V (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.
At T_A=25°C (unless otherwise noted)

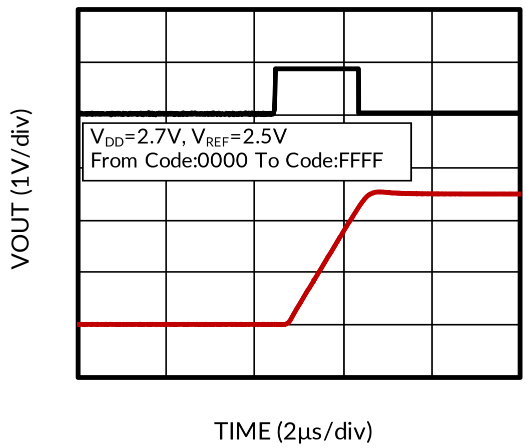


Figure 41. Full-Scale Settling Time, 2.7-V Rising Edge

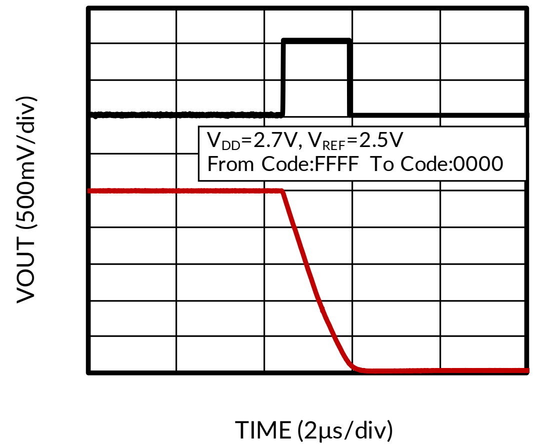


Figure 42. Full-Scale Settling Time, 2.7-V Falling Edge

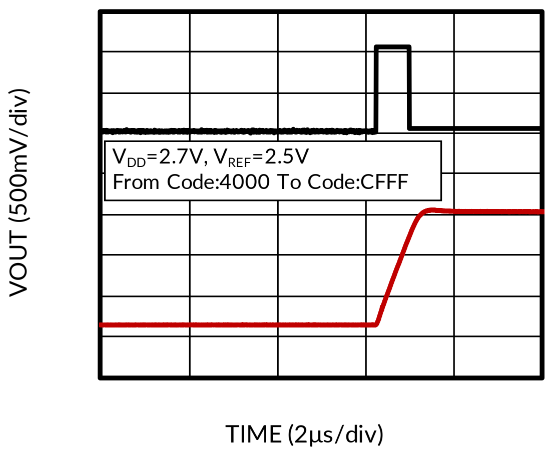


Figure 43. Half-Scale Settling Time, 2.7-V Rising Edge

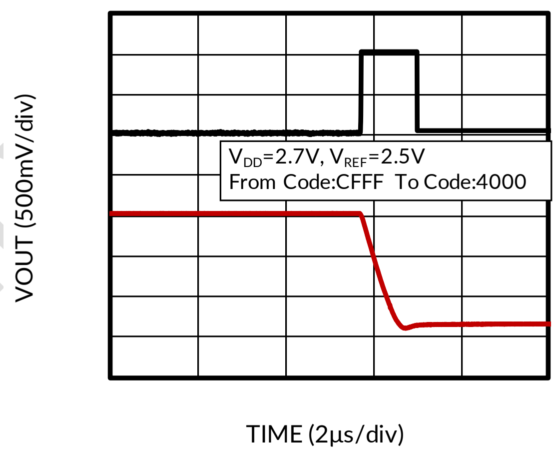


Figure 44. Half-Scale Settling Time, 2.7-V Falling Edge

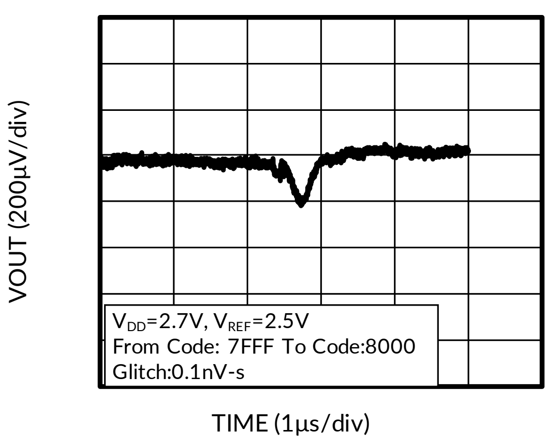


Figure 45. Glitch Energy: 2.7-V, 1-LSB Step, Rising Edge

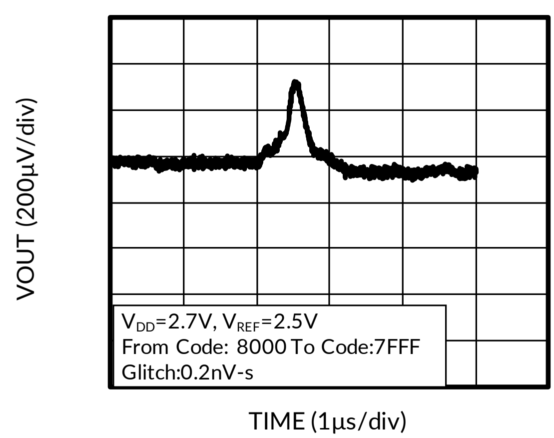


Figure 46. Glitch Energy: 2.7-V, 1-LSB Step, Falling Edge

V_{DD} =2.7V (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A=25°C (unless otherwise noted)

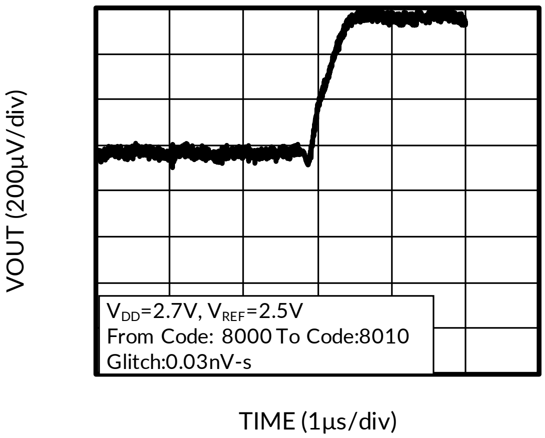


Figure 47. Glitch Energy: 2.7-V, 16-LSB Step, Rising Edge

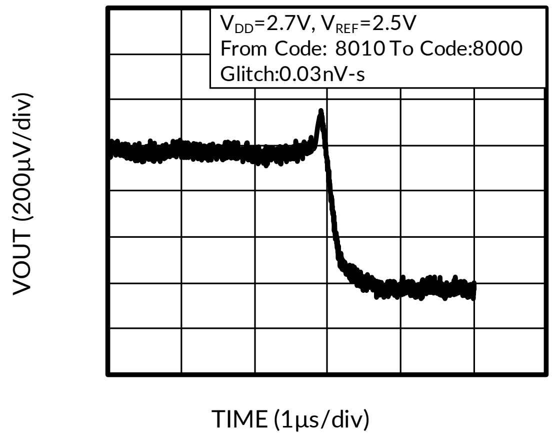


Figure 48. Glitch Energy: 2.7-V, 16-LSB Step, Falling Edge

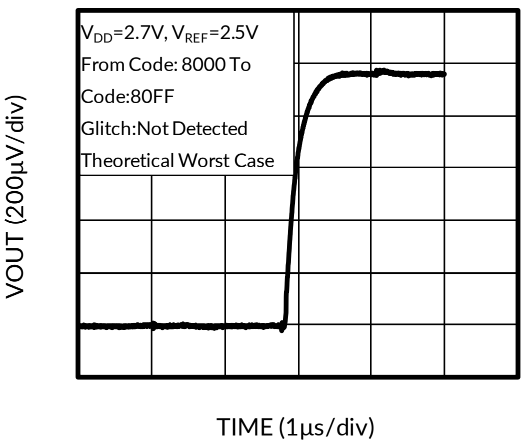


Figure 49. Glitch Energy: 2.7-V, 256-LSB Step, Rising Edge

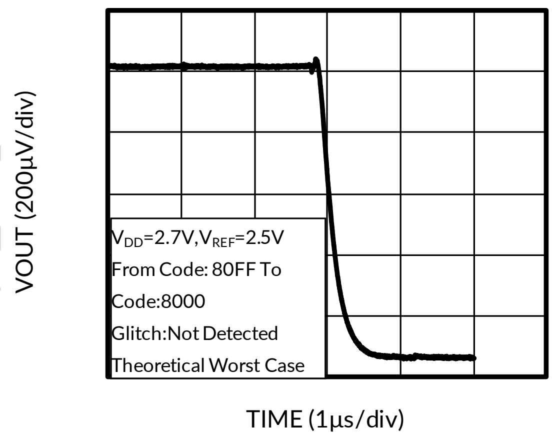


Figure 50. Glitch Energy: 2.7-V, 256-LSB Step, Falling Edge

8 DETAILED DESCRIPTION

8.1 Overview

The RS1361 is a small, low-power, voltage output, single-channel, 16-bit, DAC. The device is monotonic by design, provides excellent linearity, and minimizes undesired code-to-code transient voltages. The RS1361 uses a versatile, three-wire serial interface that operates at clock rates of up to 30 MHz and is compatible with standard SPI, QSPI, Microwire, and digital signal processor (DSP) interfaces.

8.2 Functional Block Diagram

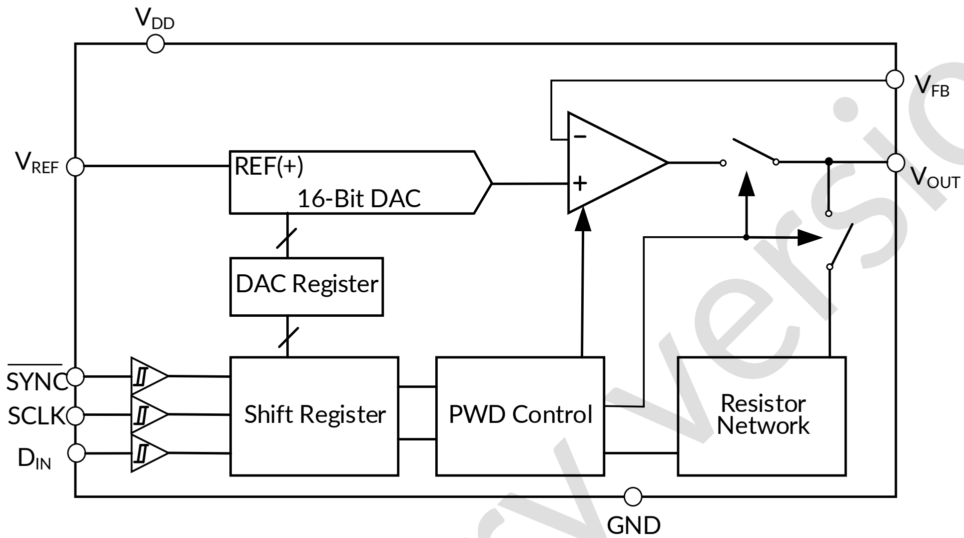


Figure 51. Functional Block Diagram

8.3 Feature Description

8.3.1 DAC Section

The RS1361 architecture consists of a string DAC followed by an output buffer amplifier. Figure 52 shows a block diagram of the DAC architecture.

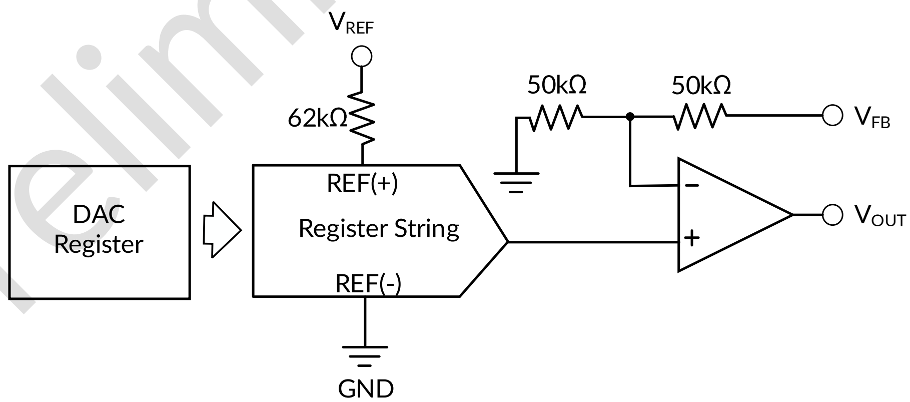


Figure 52. RS1361 Architecture

The input coding to the RS1361 is straight binary, so the ideal output voltage is given by:

$$V_O = D_{IN} / 65536 \times V_{REF} \quad (1)$$

Where

- D_{IN} = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 65535.

8.3.1.1 Resistor String

The resistor string section is shown in Figure 53. It is simply a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. Monotonicity is ensured because of the string resistor architecture.

8.3.1.2 Output Amplifier

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving an output range of 0 V to V_{DD}. It is capable of driving a load of 2kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in the Typical Characteristics section V_{DD} = 5 V. The slew rate is 1.7 V/µs with a full-scale setting time of 4 µs with the output unloaded.

The inverting input of the output amplifier is brought out to the V_{FB} pin. This configuration allows for better accuracy in critical applications by tying the V_{FB} point and the amplifier output together directly at the load. Other signal conditioning circuitry may also be connected between these points for specific applications.

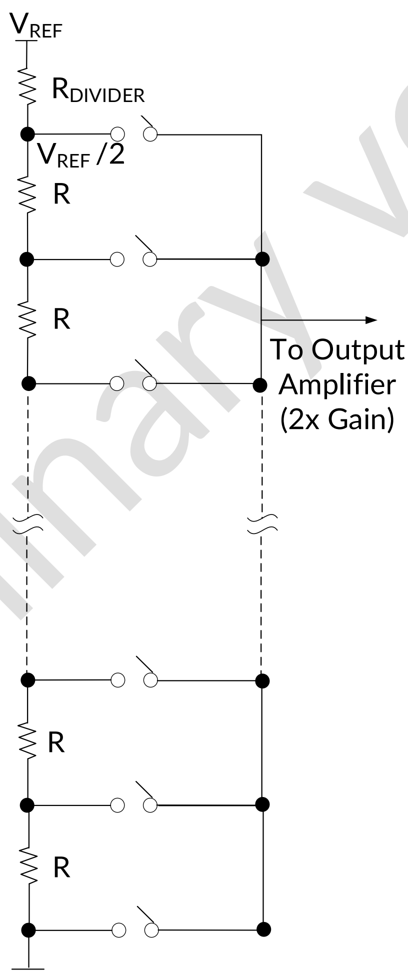


Figure 53. Resistor String

8.3.2 Power-On Reset

The RS1361 contains a power-on-reset circuit that controls the output voltage during power up. On power up, the DAC registers are filled with zeros and the output voltages are 0 V; they remain that way until a valid write sequence is made to the DAC. The power-on reset is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

8.4 Device Functional Modes

8.4.1 Power-Down Modes

The RS1361 supports four separate modes of operation. These modes are programmable by setting two bits (PD1 and PD0) in the control register. Table 1 shows how the state of the bits corresponds to the mode of operation of the device.

Table 1. Operating Modes

PD1 (DB17)	PD0 (DB16)	OPERATING MODE
0	0	Normal operation
Power-down modes		
0	1	Output typically 1 kΩ to GND
1	0	Output typically 100 kΩ to GND
1	1	High-Z

When both bits are set to '0', the device works normally with its typical current consumption of 180 µA at 5 V. However, for the three power-down modes, the supply current falls to 10 nA at 5 V (10 nA at 3 V). Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This configuration has the advantage that the output impedance of the device is known while it is in power-down mode. There are three different options. The output is connected internally to GND through a 1-kΩ resistor, a 100-kΩ resistor, or it is left open-circuited (High-Z). The output stage is illustrated in Figure 54.

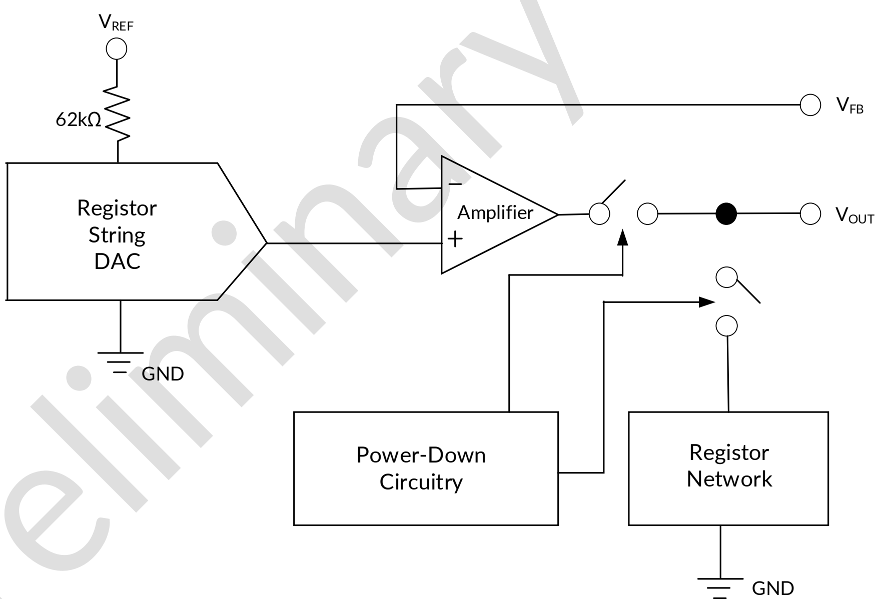


Figure 54. Output Stage During Power-Down

All analog circuitry is shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. Power up time is typically 12 µs for V_{DD} = 5 V, and 13 µs for V_{DD} = 3 V. See Typical Characteristics for more information.

8.5 Programming

8.5.1 Serial Interface

The RS1361 has a 3-wire serial interface ($\overline{SYNC}$, and D_{IN}), which is compatible with SPI, QSPI, and Microwire interface standards, as well as most DSPs. See Figure 1 for an example of a typical write sequence. The write sequence begins by bringing the $\overline{SYNC}$ line LOW. Data from the D_{IN} line are clocked into the 24-bit shift register on each falling edge of SCLK. The serial clock frequency can be as high as 30 MHz, making the RS1361 compatible with high-speed DSPs. On the 24th falling edge of the serial clock, the last data bit is clocked in and the programmed function is executed (that is, a change in DAC register contents and/or a change in the mode of operation).

At this point, the $\overline{SYNC}$ line may be kept LOW or brought HIGH. In either case, it must be brought HIGH for a minimum of 33 ns before the next write sequence so that a falling edge of $\overline{SYNC}$ can initiate the next write sequence. As previously mentioned, it must be brought HIGH again just before the next write sequence.

8.5.2 Input Shift Register

The input shift register is 24 bits wide, as shown in Figure 55. The first six bits are unused bits. The next two bits (PD1 and PD0) are control bits that control which mode of operation the part is in (normal mode or any one of three power-down modes). A more complete description of the various modes is located in Power-Down Modes. The next 16 bits are the data bits. These bits are transferred to the DAC register on the 24th falling edge of SCLK.

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Unused						PD1	PD0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Figure 55. RS1361 Data Input Register Format

8.5.3 $\overline{SYNC}$ Interrupt

In a normal write sequence, the $\overline{SYNC}$ line is kept LOW for at least 24 falling edges of SCLK and the DAC is updated on the 24th falling edge. However, if $\overline{SYNC}$ is brought HIGH before the 24th falling edge, it acts as an interrupt to the write sequence. The shift register is reset, and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs, as shown in Figure 56.

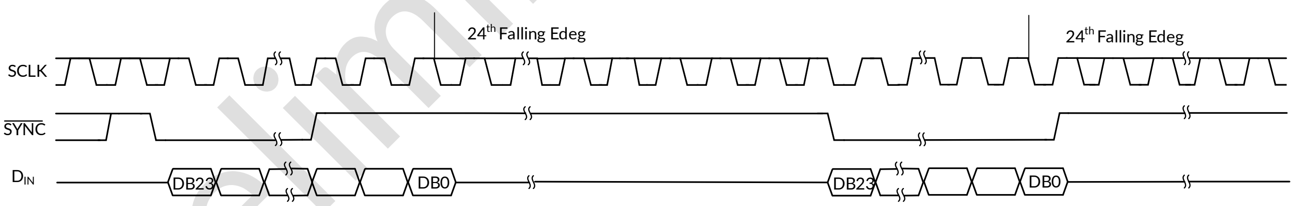


Figure 56. $\overline{SYNC}$ Interrupt Facility

9 APPLICATION AND IMPLEMENTATION

Information in the following applications sections is not part of the RUNIC component specification, and RUNIC does not warrant its accuracy or completeness. RUNIC's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The low-power consumption of the RS1361 lends itself to applications such as loop-powered control where the current dissipation of each device is critical. The low power consumption also allows the RS1361 to be powered using only a precision reference for increased accuracy. The low-power operation coupled with the ultra-low power power-down modes also make the RS1361 a great choice for battery and portable applications.

9.1.1 Bipolar Operation Using the RS1361

The RS1361 has been designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 57. The circuit shown gives an output voltage range of $\pm V_{REF}$. Rail-to-rail operation at the amplifier output is achievable using an operational amplifier. See CMOS, Rail-to-Rail, I/O Operational Amplifiers for more information.

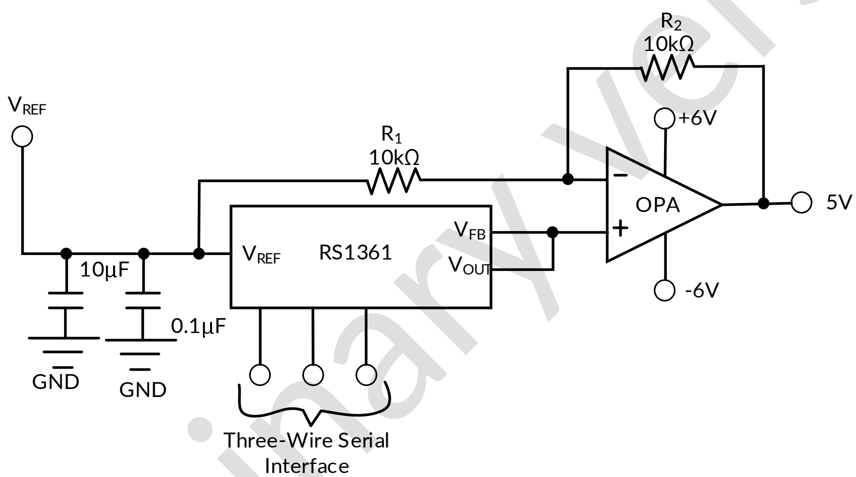


Figure 57. Bipolar Output Range

The output voltage for any input code can be calculated as follows:

$$V_0 = \left[V_{REF} \times \left(\frac{D}{65536}\right) \times \left(\frac{R_1 + R_2}{R_1}\right) - V_{REF} \times \left(\frac{R_2}{R_1}\right)\right] \quad (2)$$

Where

- D is the input code in decimal (0-65535).

With V_{REF}=5V, R_1=R_2=10kΩ.

$$V_0 = \left(\frac{10 \times D}{65536}\right) - 5V \quad (3)$$

Using this example, an output voltage range of ±5 V with 0000h corresponding to a 5 V output and FFFFh corresponding to a 5 V output can be achieved. Similarly, using V_{REF} = 2.5 V, a ±2.5 V output voltage range can be achieved.

9.2 Typical Application

9.2.1 Loop-Powered, 2-Wire, 4-mA to 20-mA Transmitter With XTR116

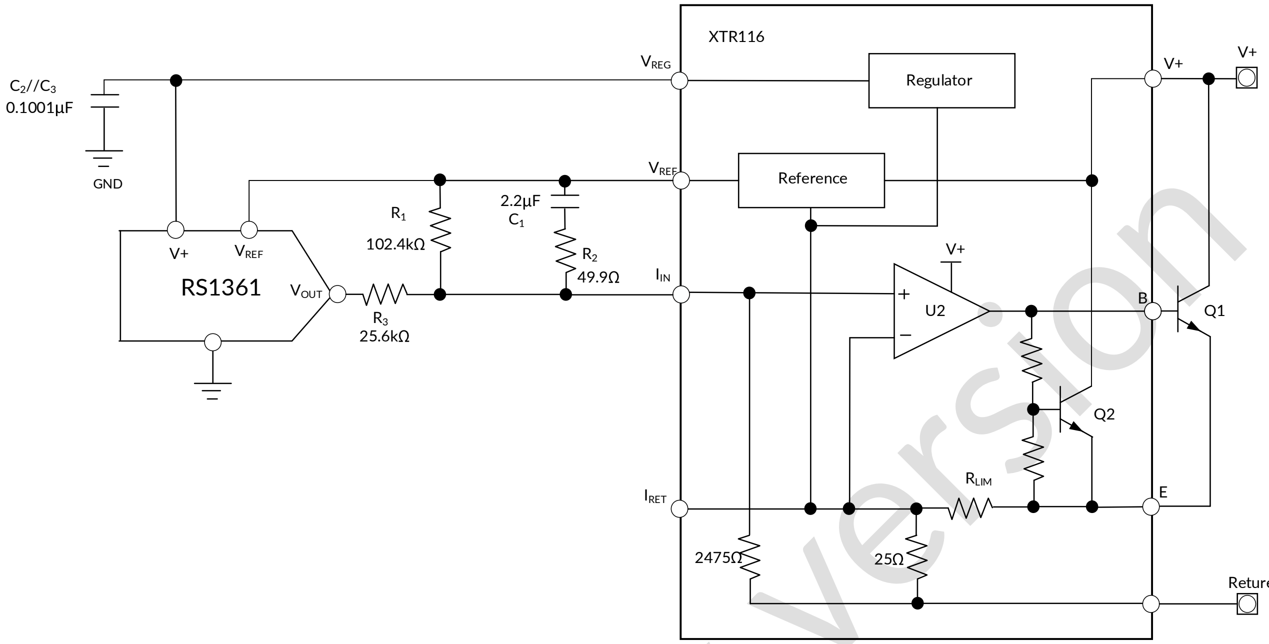


Figure 58. Loop-Powered Transmitter

9.2.1.1 Design Requirements

This design is commonly referred to as a loop-powered, or 2-wire, 4-mA to 20-mA transmitter. The transmitter has only two external input terminals: a supply connection and an output, or return, connection. The transmitter communicates back to its host, typically a PLC analog input module, by precisely controlling the magnitude of its return current. In order to conform to the 4-mA to 20-mA communication standard, the complete transmitter must consume less than 4 mA of current. The RS1361 enables the accurate control of the loop current from 4 mA to 20 mA in 16-bit steps.

9.2.1.2 Detailed Design Procedure

Although it is possible to recreate the loop-powered circuit using discrete components, the XTR116 provides simplicity and improved performance due to the matched internal resistors. The output current can be modified if necessary by looking using Equation 4.

$$I_{OUT}(\text{Code}) = \left(\frac{V_{REF} \times \text{Code}}{2^N \times R_3} + \frac{V_{REG}}{R_1}\right) \times \left(1 + \frac{2475\,\Omega}{25\,\Omega}\right) \quad (4)$$

See 2-wire, 4-mA to 20-mA Transmitter, EMC/EMI Tested Reference Design (TIDUAO7) for more information. It covers in detail the design of this circuit as well as how to protect it from EMC/EMI tests.

9.2.1.3 Application Curves

Total unadjusted error (TUE) is a good estimate for the performance of the output as shown in Figure 59. The linearity of the output or INL is in Figure 60.

Typical Application (continued)

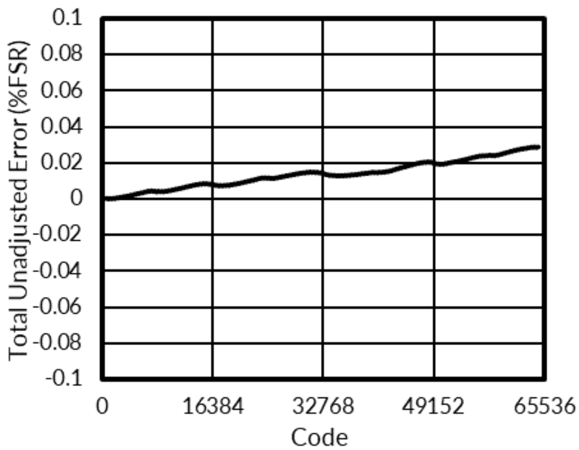


Figure 59. Total Unadjusted Error

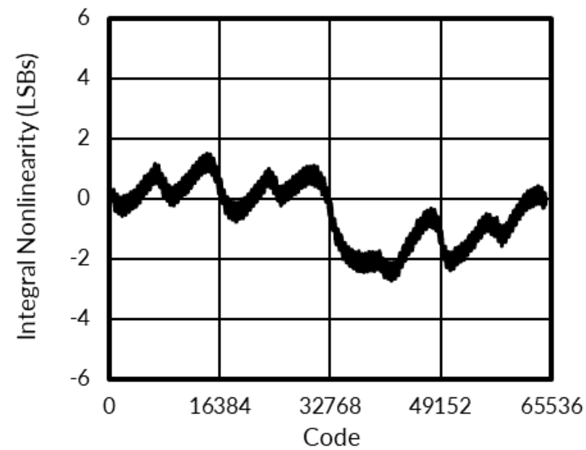


Figure 60. Integral Nonlinearity

9.2.2 Using the RS3450-Q1 as a Power Supply for the RS1361

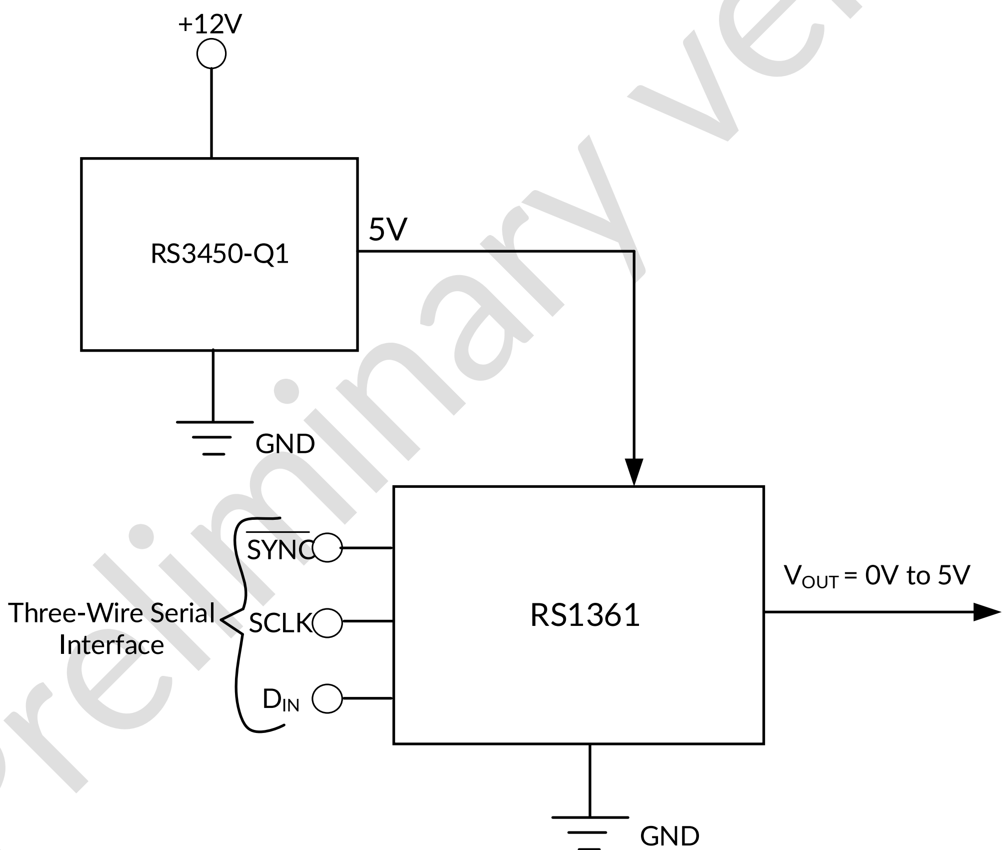


Figure 61. RS3450-Q1 as a Power Supply to the RS1361

9.2.2.1 Design Requirements

Due to the extremely low supply current required by the RS1361, an alternative option is to use the RS3450-Q1 to supply the required voltage to the device, as illustrated in Figure 61. See +5 V Precision Voltage Reference (SBVS003) for more information.

9.2.2.2 Detailed Design Procedure

This configuration is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5 V. The RS3450-Q1 outputs a steady supply voltage for the RS1361. If the RS3450-Q1 is used, the current it needs to supply to the RS1361 is 200 µA. This configuration is with no load on the output of the DAC. When a DAC output is loaded, the RS3450-Q1 also needs to supply the current to the load.
The total typical current required (with a 5-kΩ load on the DAC output) is:

$$200\,\mu\text{A} + \frac{5\text{V}}{5\text{k}\Omega} = 1.2\text{mA} \tag{5}$$

The load regulation of the RS3450-Q1 is typically 0.005%/mA, resulting in an error of 299 µV for the 1.2-mA current drawn from it. This value corresponds to a 3.9-LSB error.

9.3 System Examples

9.3.1 Microprocessor Interfacing

9.3.1.1 RS1361 to 8051 Interface

Figure 62 shows a serial interface between the RS1361 and a typical 8051-type microcontroller.
The interface is setup with the TXD of the 8051 drives SCLK of the RS1361, while RXD drives the serial data line of the device. The $\overline{SYNC}$ signal is derived from a bit-programmable pin on the port of the 8051. In this case, port line P3.3 is used. When data are to be transmitted to the RS1361, P3.3 is taken LOW. The 8051 transmits data in 8-bit bytes; thus, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left LOW after the first eight bits are transmitted, then a second write cycle is initiated to transmit the second byte of data. P3.3 is taken HIGH following the completion of the third write cycle. The 8051 outputs the serial data in a format that has the LSB first. The RS1361 requires data with the MSB as the first bit received. The 8051 transmit routine must therefore take this into account, and mirror the data as needed.

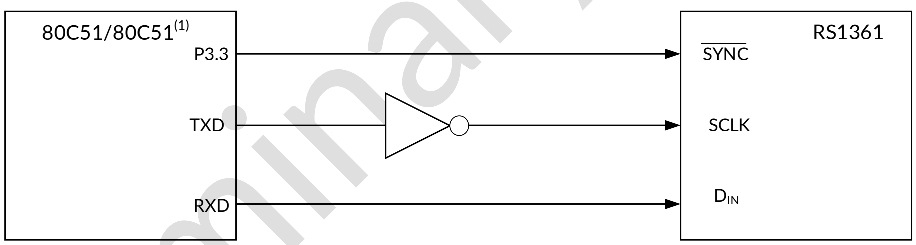


Figure 62. RS1361 to 80C51 or 80C51 Interface

NOTE: (1) Additional pins omitted for clarity.

9.3.1.2 RS1361 to Microwire Interface

Figure 63 shows an interface between the RS1361 and any Microwire-compatible device. Serial data are shifted out on the falling edge of the serial clock and is clocked into the RS1361 on the rising edge of the SK signal.

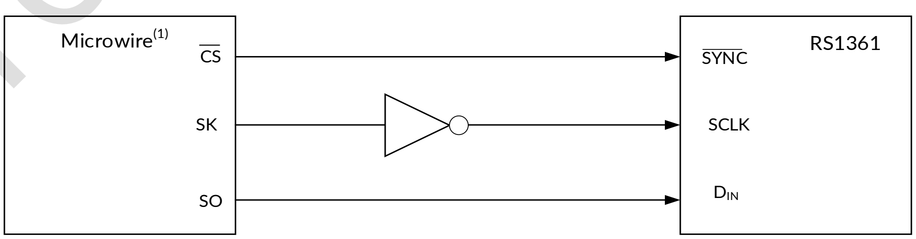


Figure 63. RS1361 to Microwire Interface

NOTE: (1) Additional pins omitted for clarity.

9.3.1.3 RS1361 to 68HC11 Interface

Figure 64 shows a serial interface between the RS1361 and the 68HC11 microcontroller. SCK of he 68HC11 drives the SCLK of the RS1361, while the MOSI output drives the serial data line of the DAC. The $\overline{\text{SYNC}}$ signal is derived from a port line (PC7), similar to the 8051 diagram.

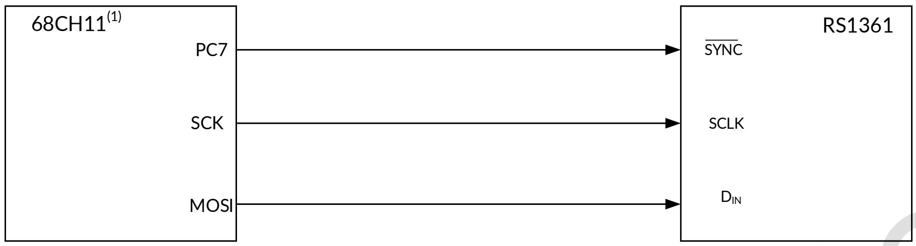


Figure 64. RS1361 to 68HC11 Interface

NOTE: (1) Additional pins omitted for clarity.

The 68HC11 should be configured so that its CPOL bit is '0' and its CPHA bit is '1'. This configuration causes data appearing on the MOSI output to be valid on the falling edge of SCK. When data are being transmitted to the DAC, the $\overline{\text{SYNC}}$ line is held LOW (PC7). Serial data from the 68HC11 are transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. (Data are transmitted MSB first.) In order to load data to the RS1361, PC7 is left LOW after the first eight bits are transferred, then a second and third serial write operation are performed to the DAC. PC7 is taken HIGH at the end of this procedure.

10 POWER SUPPLY RECOMMENDATIONS

The RS1361 can operate within the specified supply voltage range of 2.7 V to 5.5 V. The power applied to V_{DD} should be well-regulated and low-noise. Switching power supplies and DCDC converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high- frequency spikes. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. Runic recommends including a 1 µF to 10 µF capacitor and 0.1 µF bypass capacitor in order to further minimize noise from the power supply. The current consumption on the V_{DD} pin, the short-circuit current limit, and the load current for the device is listed in Electrical Characteristics. The power supply must meet the aforementioned current requirements.

11 LAYOUT

11.1 Layout Guidelines

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

The RS1361 offers single-supply operation, and it often is used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to keep digital noise from appearing at the output.

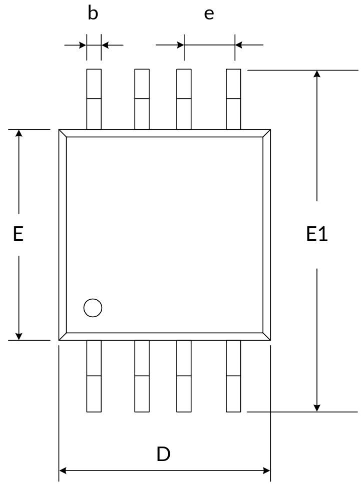
Due to the single ground pin of the RS1361, all return currents, including digital and analog return currents for the DAC, must flow through a single point. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power-entry point of the system.

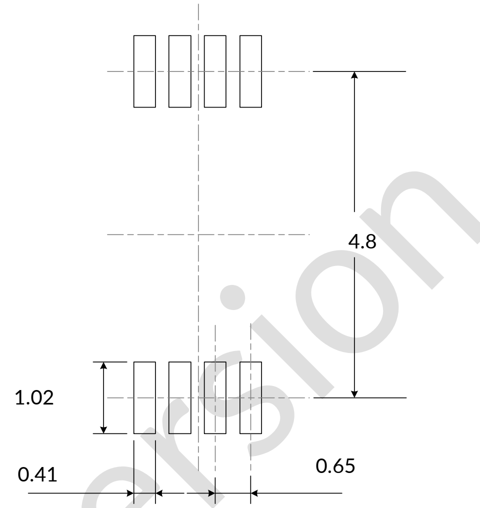
As with the GND connection, V_{DD} should be connected to a 5 V power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power-entry point. Runic recommends an additional 1 µF to 10 µF capacitor and 0.1 µF bypass capacitor. In some situations, additional bypassing may be required, such as a 100 µF electrolytic capacitor or even a Pi filter made up of inductors and capacitors—all designed to essentially low-pass filter the 5-V supply, removing the high-frequency noise.

11.2 Layout Example

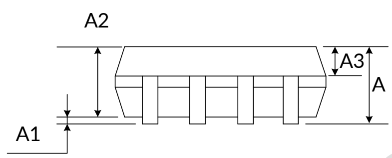
12 PACKAGE OUTLINE DIMENSIONS

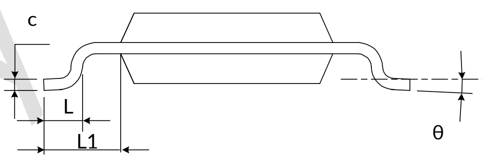
MSOP8 (4)





RECOMMENDED LAND PATTERN (Unit: mm)





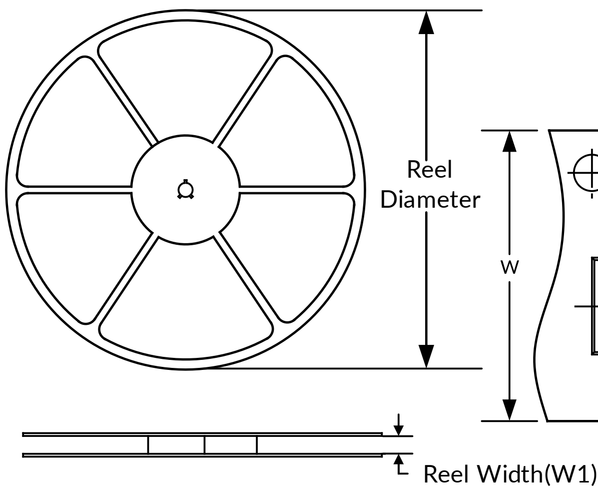
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.100		0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
A3	0.300	0.400	0.012	0.016
b	0.280	0.360	0.011	0.014
c	0.150	0.190	0.006	0.007
D (1)	2.900	3.100	0.114	0.122
e	0.650(BSC) (2)		0.026(BSC) (2)	
E (1)	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.200
L	0.400	0.700	0.016	0.027
L1	0.950(REF) (3)		0.037(REF) (3)	
θ	0°	8°	0°	8°

NOTE:

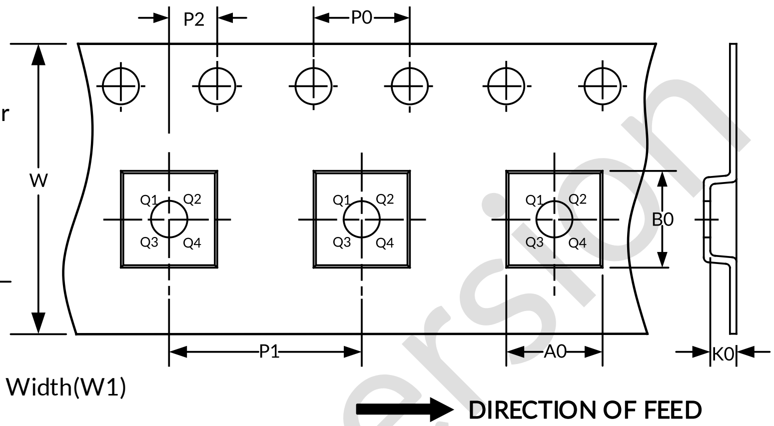
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. REF is the abbreviation for Reference.
4. This drawing is subject to change without notice.

13 TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
MSOP8	13”	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

IMPORTANT NOTICE AND DISCLAIMER

Jiangsu RUNIC Technology Co., Ltd. will accurately and reliably provide technical and reliability data (including data sheets), design resources (including reference designs), application or other design advice, WEB tools, safety information and other resources, without warranty of any defect, and will not make any express or implied warranty, including but not limited to the warranty of merchantability Implied warranty that it is suitable for a specific purpose or does not infringe the intellectual property rights of any third party.

These resources are intended for skilled developers designing with RUNIC products You will be solely responsible for: (1) Selecting the appropriate products for your application; (2) Designing, validating and testing your application; (3) Ensuring your application meets applicable standards and any other safety, security or other requirements; (4) RUNIC and the RUNIC logo are registered trademarks of RUNIC INCORPORATED. All trademarks are the property of their respective owners; (5) For change details, review the revision history included in any revised document. The resources are subject to change without notice. Our company will not be liable for the use of this product and the infringement of patents or third-party intellectual property rights due to its use.