0.7 µA, High-Precision Operational Amplifier

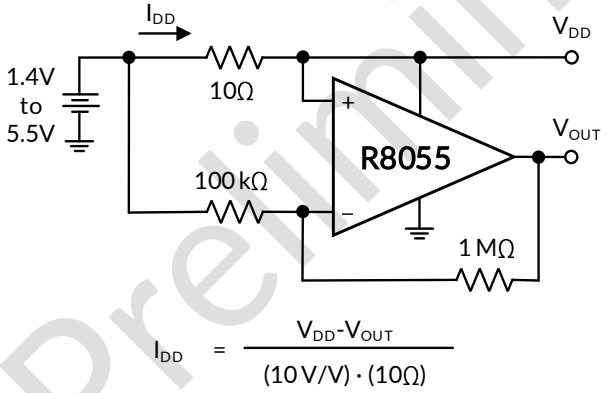
1 FEATURES

- **Rail-to-Rail Input and Output**
- **Low Offset Voltage: ±70 µV (maximum)**
- **Ultra-Low Quiescent Current: 0.7 µA (typical)**
- **Wide Power Supply Voltage: 1.8V to 5.5V**
- **Gain Bandwidth Product: 8 kHz (typical)**
- **Unity Gain Stable**
- **Extended Temperature Range: -40°C to +125°C**
- **No Phase Reversal**

2 APPLICATIONS

- **Toll Booth Tags**
- **Wearable Products**
- **Battery Current Monitoring**
- **Sensor Conditioning**
- **Battery Powered**

Typical Application



High-Side Battery Current Sensor

3 DESCRIPTIONS

RS8055/RS8056 family of operational amplifiers (op amps) operates with a single-supply voltage as low as 1.8V, while drawing ultra-low quiescent current per amplifier (0.7 µA, typical). This device also has low input offset voltage (±70 µV, maximum) and rail-to-rail input and output operation. This combination of features supports battery-powered and portable applications.

The RS8055/RS8056 family is unity gain stable and has a gain bandwidth product of 8 kHz (typical). These specifications make these op amps appropriate for low-frequency applications, such as battery current monitoring and sensor conditioning.

The RS8055/RS8056 family is designed with advanced CMOS process. All devices are available in the extended temperature range, with a power supply range of 1.8V to 5.5V.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE(NOM)
RS8055	SOT23-5	2.90mm×1.60mm
	SC70-5	2.10mm×1.25mm
RS8056	SOP8	4.90mm×3.90mm
	MSOP8	3.00mm×3.00mm
	DFN2X2-8	2.00mm×2.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Table of Contents

4 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

Version	Change Date	Change Item
A.0	2025/08/05	Preliminary version completed
A.0.1	2025/08/27	Update Absolute Maximum Ratings and Electrical Characteristics
A.0.2	2025/10/10	1. Update Electrical Characteristics 2. Add Figure 21. Closed-Loop Output Impedance vs Frequency 3. Delete 8.1.2 Input Voltage and Current Limits in RevA.0.1 4. Update Typical Characteristics Figure 5, 6

5 PACKAGE/ORDERING INFORMATION (1)

Orderable Device	Package Type	Pin	Channel	Op Temp(°C)	Device Marking (2)	MSL (3)	Package Qty
RS8055XF	SOT23-5	5	1	-40°C ~125°C	8055	MSL3	Tape and Reel, 3000
RS8055BXC5	SC70-5 (4)	5	1	-40°C ~125°C	8055B	MSL3	Tape and Reel, 3000
RS8056XK	SOP8	8	2	-40°C ~125°C	RS8056	MSL3	Tape and Reel, 4000
RS8056XM	MSOP8	8	2	-40°C ~125°C	RS8056	MSL3	Tape and Reel, 4000
RS8056XTDE8	DFN2X2-8	8	2	-40°C ~125°C	8056	MSL3	Tape and Reel, 3000

NOTE:

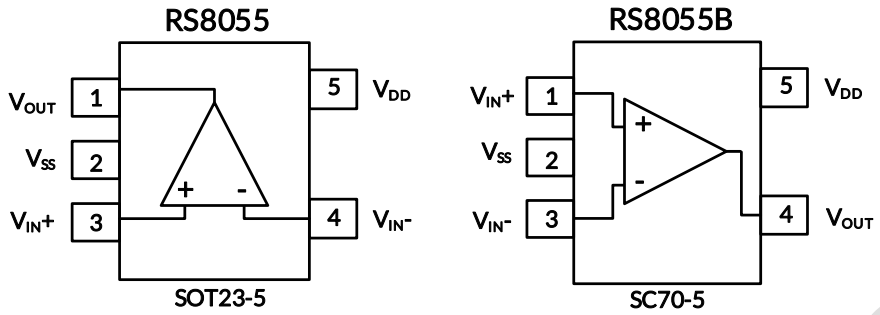
(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

(4) Equivalent to SOT353.

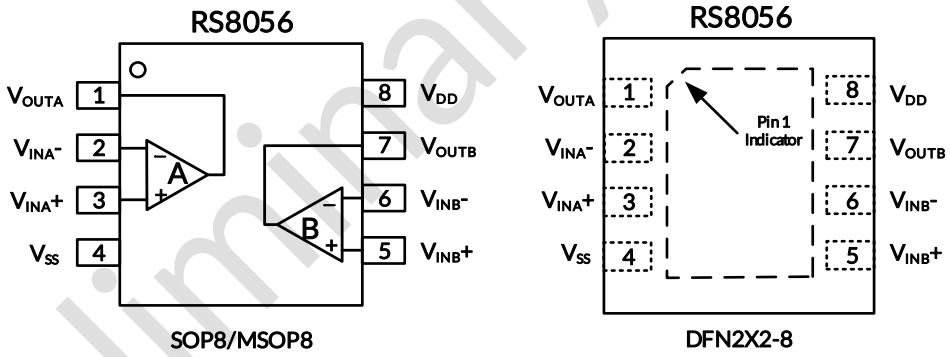
6 PIN CONFIGURATION AND FUNCTIONS



PIN DESCRIPTION

NAME	PIN		I/O (1)	DESCRIPTION
	RS8055	RS8055B		
	SOT23-5	SC70-5		
V_{OUT}	1	4	O	Analog Output
V_{IN}-	4	3	I	Inverting Input
V_{IN}+	3	1	I	Noninverting Input
V_{DD}	5	5	-	Positive Power Supply
V_{SS}	2	2	-	Negative Power Supply

(1) I = Input, O = Output.



PIN DESCRIPTION

NAME	PIN	I/O (1)	DESCRIPTION
	SOP8/MSOP8/DFN2X2-8		
V_{OUTA}	1	O	Analog Output (Op Amp A)
V_{INA}-	2	I	Inverting Input (Op Amp A)
V_{INA}+	3	I	Noninverting Input (Op Amp A)
V_{DD}	8	-	Positive Power Supply
V_{INB}+	5	I	Noninverting Input (Op Amp B)
V_{INB}-	6	I	Inverting Input (Op Amp B)
V_{OUTB}	7	O	Analog Output (Op Amp B)
V_{SS}	4	-	Negative Power Supply

(1) I=Input, O=Output.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Voltage	Supply, V_S=(V+) - (V-)			6	V
	Signal input pin (2)		(V-)-0.3	(V+) +0.3	
	Signal output pin (3)		(V-)-0.3	(V+) +0.3	
	Differential input voltage		(V-)-(V+)	(V+)-(V-)	
Current	Signal input pin (2)		-10	10	mA
	Signal output pin (3)		-10	10	mA
	Output short-circuit (4)		Continuous		
θ_{JA}	Package thermal impedance (5)	SOT23-5		230	°C/W
		SC70-5		380	
		SOP8		110	
		MSOP8		170	
		DFN2X2-8		80	
Temperature	Operating range, T_A		-40	125	°C
	Junction, T_J (6)		-40	150	
	Storage, T_{stg}		-65	150	
	Lead temperature (Soldering, 10 sec)		260		

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current-limited to ±10mA or less.
(3) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.3V beyond the supply rails should be current-limited to ±10mA or less.
(4) Short-circuit to ground, one amplifier per package.
(5) The package thermal impedance is calculated in accordance with JESD-51.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), EIA/JESD22-a114	±4000	V
		Charged-Device Model (CDM), ANSI/ESDA/JEDEC JS-002-2022	±1500	

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, V_S= (V+) - (V-)	Single-supply	1.8		5.5	V
	Dual-supply	±0.9		±2.75	

7.4 Electrical Characteristics

Unless otherwise noted [1]: T_A = +25°C, V_S=1.8 to 5.5V, R_L = 10kΩ, V_{CM} = V_{OUT} = V_S/2, Full [9] = -40°C to +125°C.

PARAMETER		CONDITIONS	T_A	RS8055, RS8056			UNIT
				MIN[2]	TYP[3]	MAX[2]	
INPUT OFFSET							
V_{OS}	Input Offset Voltage	V_S = 5V, V_{CM} = 2.5V	25°C	-35	10	35	μV
			Full	-70		70	
V_{OS} Tc	Input Offset Voltage Drift	V_S = 5V, V_{CM} = 2.5V	Full		±0.1		μV/°C
PSRR	Power-Supply Rejection Ratio	V_S = 1.8V to 5.5V V_{CM}=0.4V	25°C	90	110		dB
			Full	70			
INPUT BIAS CURRENT							
I_B	Input Bias Current [4] [5]	V_S = 5V, V_{CM} = 2.5V	25°C		30		pA
			125°C			500	
I_{OS}	Input Offset Current [4]	V_S = 5V, V_{CM} = 2.5V	25°C		30		pA
COMMON-MODE							
V_{CM}	Common-Mode Voltage Range		Full	(V-)-0.1		(V+)+0.1	V
CMRR	Common-Mode Rejection Ratio	V_{CM}=-0.1 to 5.6V, V_{DD}=5.5V	25°C	90	110		dB
		V_{CM}=-0.1 to 4.3V, V_{DD}=5.5V	25°C	95	115		dB
		V_{CM}=4.3 to 5.6V, V_{DD}=5.5V	25°C	85	105		dB
		V_{CM}=-0.1 to 1.9V, V_{DD}=1.8V	25°C	90	110		dB
Z_{CM}	Common-mode Input Impedance		25°C	/	10^{13}||6	/	Ω||pF
Z_{DIFF}	Differential Input Impedance		25°C	/	10^{13}||6	/	Ω||pF
OPEN-LOOP VOLTAGE GAIN							
A_{OL}	Open-loop Voltage Gain	R_{LOAD} = 10kΩ, (V-)+0.2V<V_O<(V+)-0.2V	25°C	95	110		dB
OUTPUT							
V_{OH}	Output Swing from Positive Rail	R_{LOAD} = 10kΩ to V_S/2	25°C		5	15	mV
V_{OL}	Output Swing from Negative Rail	R_{LOAD} = 10kΩ to V_S/2	25°C		5	15	
I_{SC}	Short-Circuit Current [6] [7]	V_{DD}=1.8V	25°C		±5		mA
		V_{DD}=5V			±30		
C_L	Capacitive Load Driving		25°C		100		pF
POWER SUPPLY							
V_S	Operating Voltage Range		Full	1.8		5.5	V
I_Q	Quiescent Current per Amplifier	V_S = 5V	25°C		0.7	0.95	μA
			Full			1.5	
AC SPECIFICATIONS							
GBW	Gain-Bandwidth Product		25°C		8		KHz
SR	Slew Rate [8]	G=1, 1V Step	25°C		3.5		V/ms
t_{OR}	Overload Recovery Time		25°C		560		μs
PM	Phase Margin	R_L=1M, C_L= 50pF	25°C		65		°
NOISE							
En	Input Voltage Noise	V_S = 5V, f = 0.1Hz to 10Hz	25°C		8.5		μVpp
en	Input Voltage Noise Density [4]	f = 100Hz	25°C		340		nV/$\sqrt{Hz}$

NOTE:

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

(4) This parameter is ensured by design and/or characterization and is not tested in production.

(5) Positive current corresponds to current flowing into the device.

(6) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

(7) Short circuit test is a momentary test.

(8) Number specified is the slower of positive and negative slew rates.

(9) Specified by characterization only.

7.5 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.
Unless otherwise indicated: T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L, C_L = 60 pF.

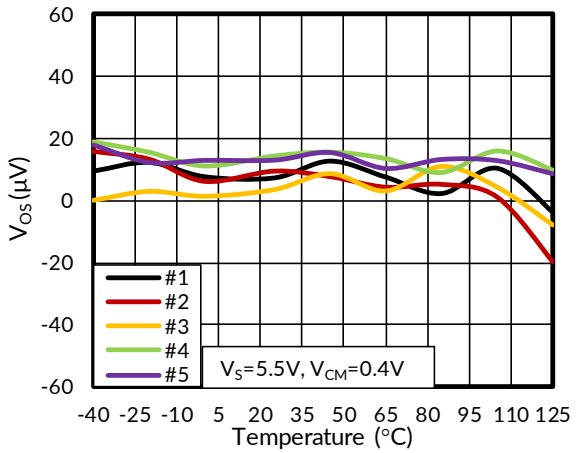


Figure 1. Offset Voltage vs Temperature

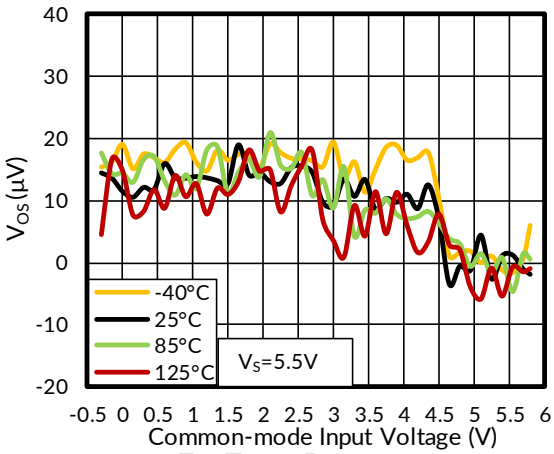


Figure 2. Input Offset Voltage vs Common-mode Input Voltage

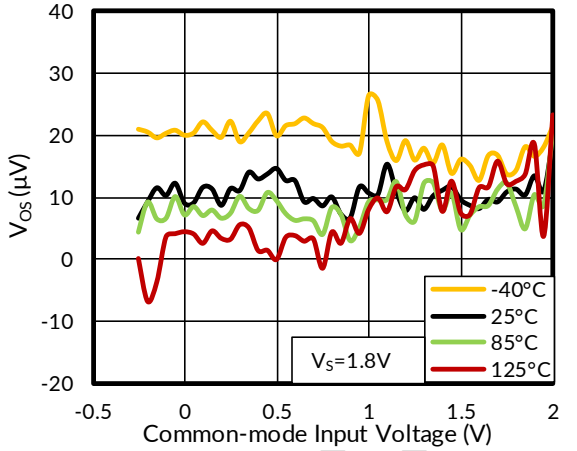


Figure 3. Input Offset Voltage vs Common-mode Input Voltage

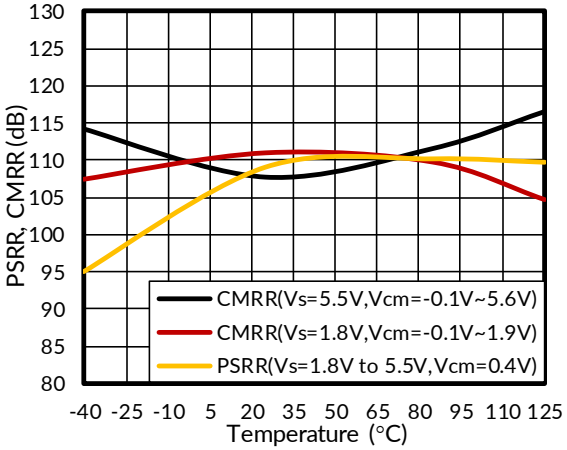


Figure 4. Common-mode Rejection Ratio, Power Supply Rejection Ratio vs Ambient Temperature.

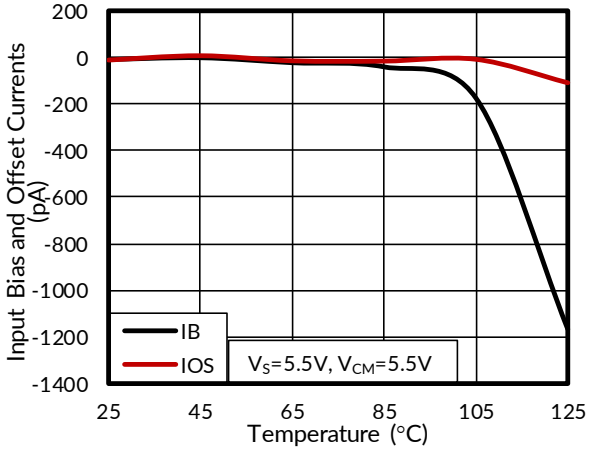


Figure 5. Input Bias, Offset Currents vs Ambient Temperature

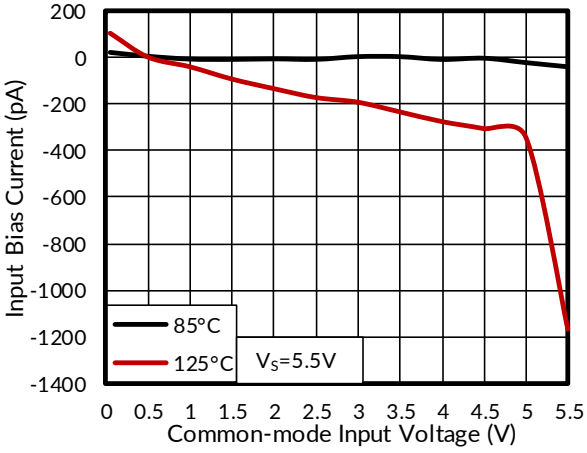


Figure 6. Input Bias Current vs Common-mode Input Voltage

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

Unless otherwise indicated: T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L, C_L = 60 pF.

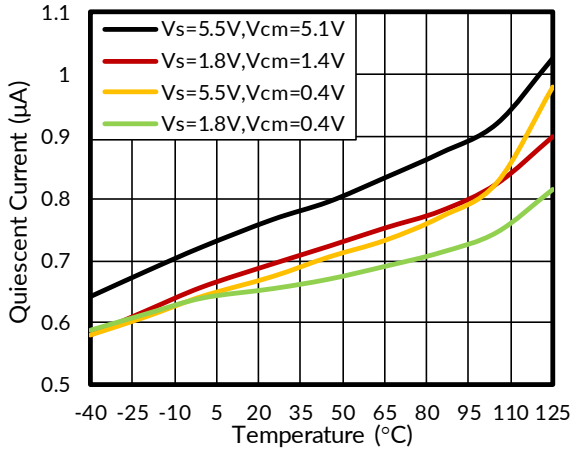


Figure 7. Quiescent Current vs Ambient Temperature

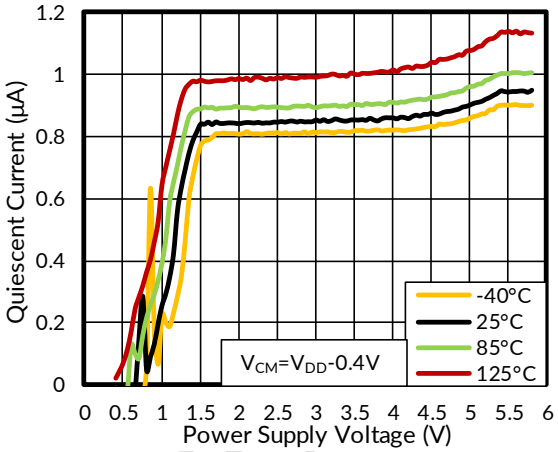


Figure 8. Quiescent Current vs Power Supply Voltage

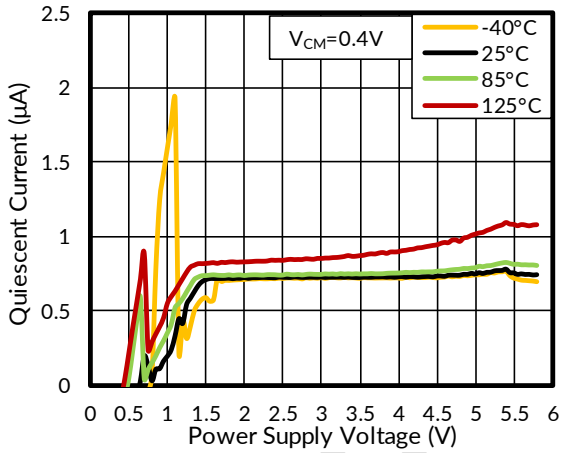


Figure 9. Quiescent Current vs Power Supply Voltage

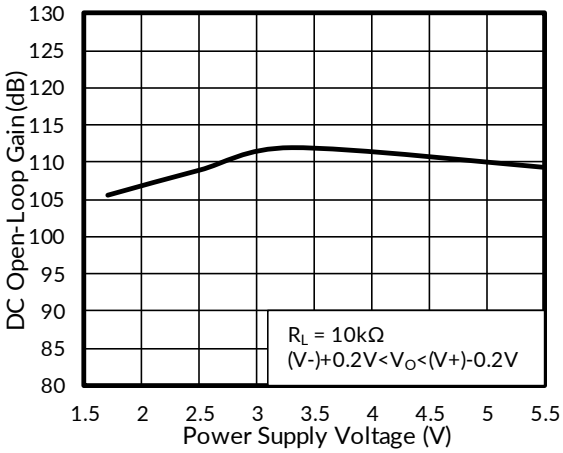


Figure 10. DC Open-Loop Gain vs Power Supply Voltage

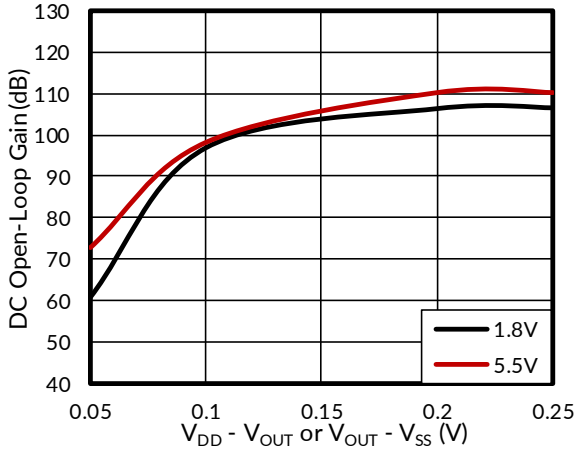


Figure 11. DC Open-Loop Gain vs Output Voltage Headroom

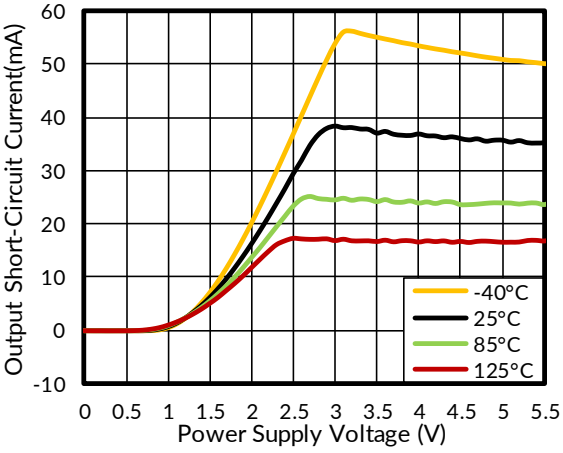


Figure 12. Output Short-Circuit Current vs Power Supply Voltage

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

Unless otherwise indicated: T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L, C_L = 60 pF.

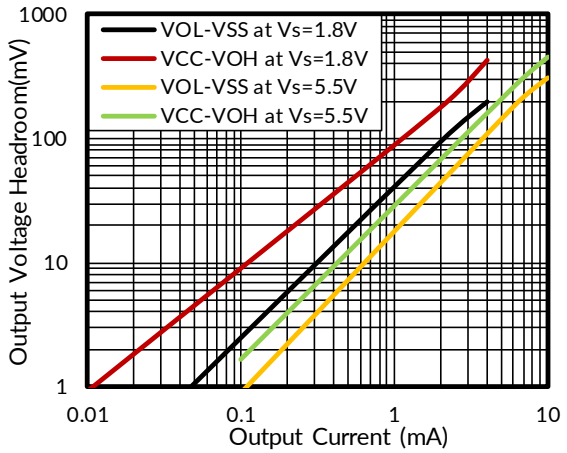


Figure 13. Output Voltage Headroom vs Output Current

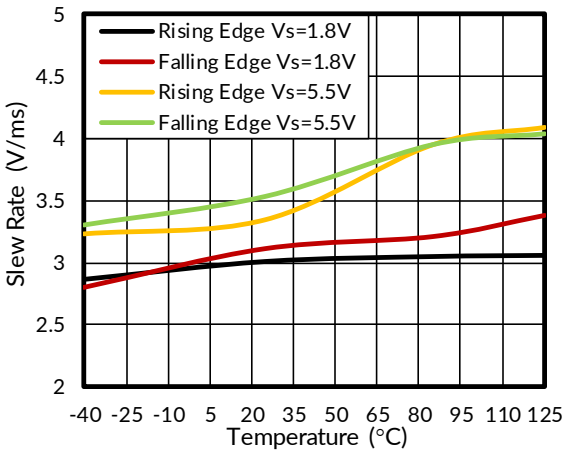


Figure 14. Slew Rate vs Ambient Temperature

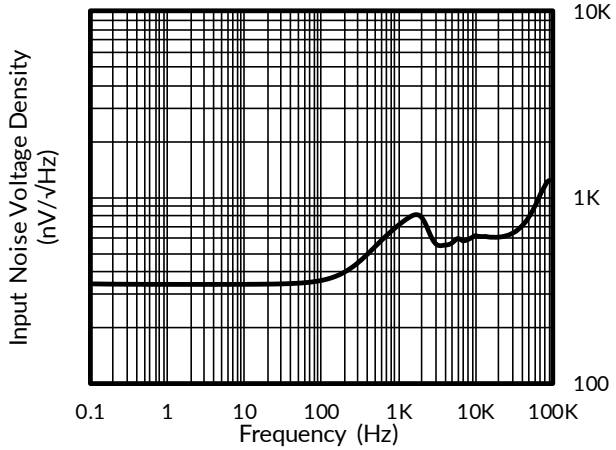


Figure 15. Input Noise Voltage Density vs Frequency

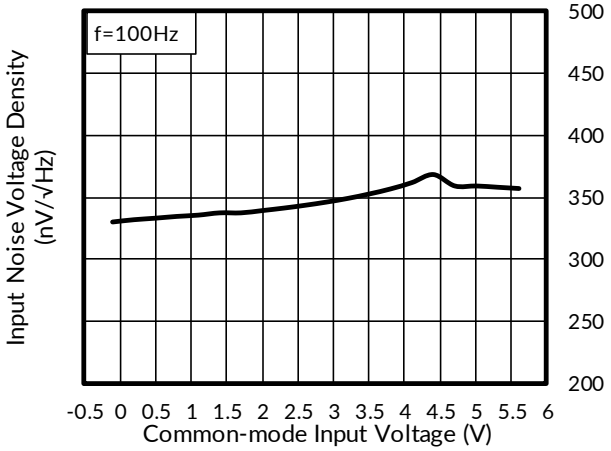


Figure 16. Input Noise Voltage Density vs Common-mode Input Voltage

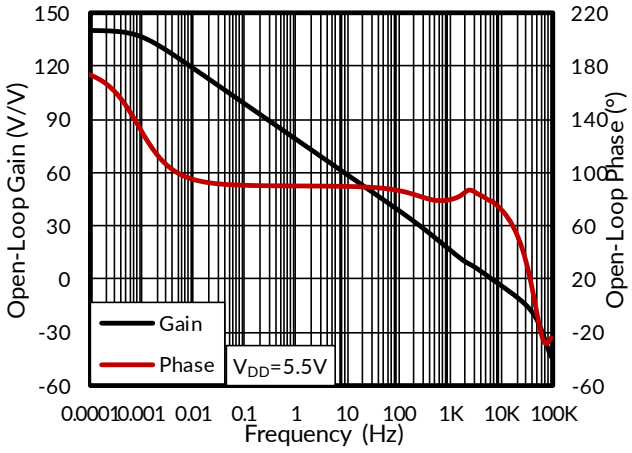


Figure 17. Open-Loop Gain, Phase vs Frequency

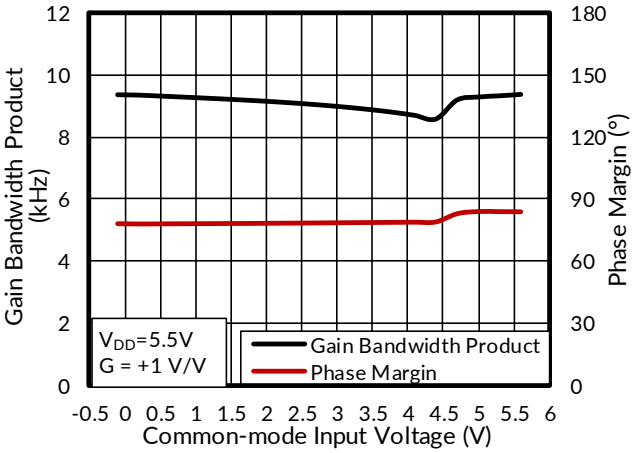


Figure 18. Gain Bandwidth Product, Phase Margin vs Common-mode Input Voltage

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

Unless otherwise indicated: T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L, C_L = 60 pF.

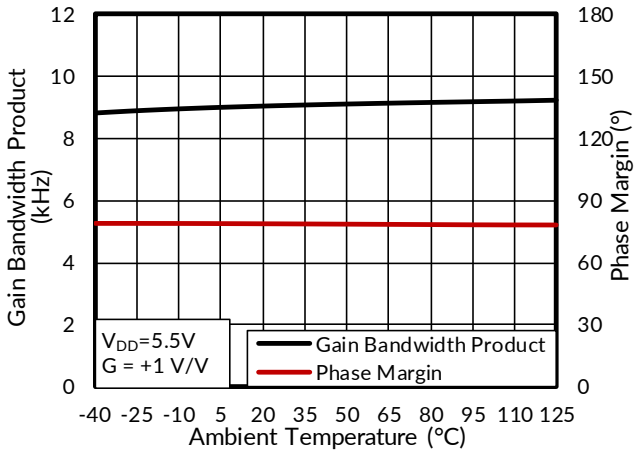


Figure 19. Gain Bandwidth Product, Phase Margin vs Ambient Temperature

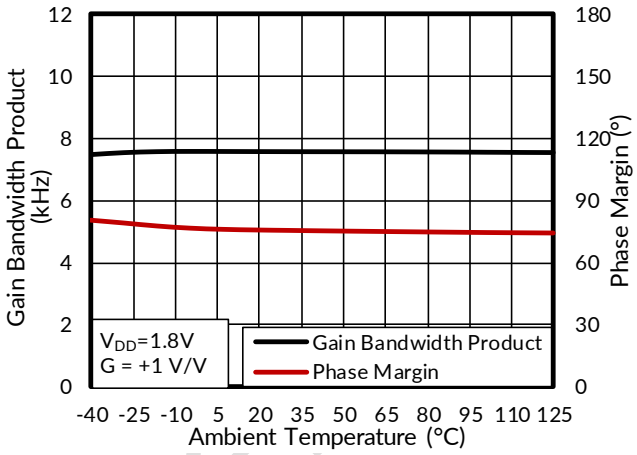


Figure 20. Gain Bandwidth Product, Phase Margin vs Ambient Temperature

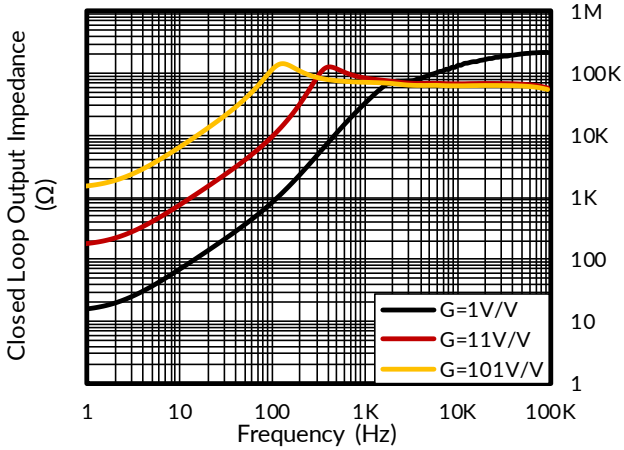


Figure 21. Closed-Loop Output Impedance vs Frequency

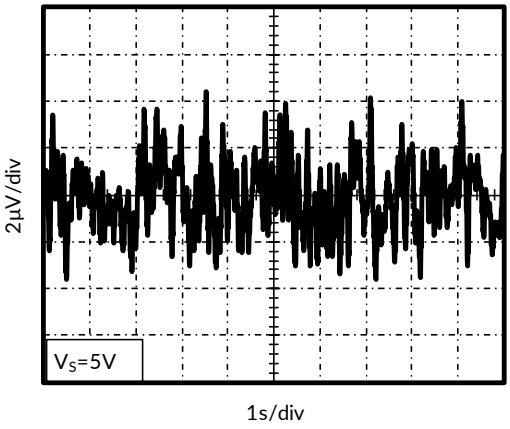


Figure 22. 0.1Hz~10Hz Noise

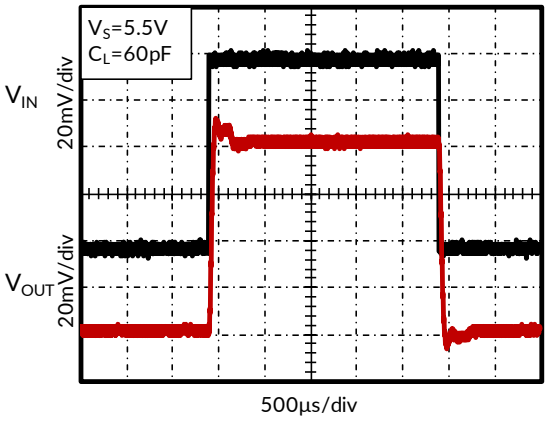


Figure 23. Small-Signal Noninverting Pulse Response

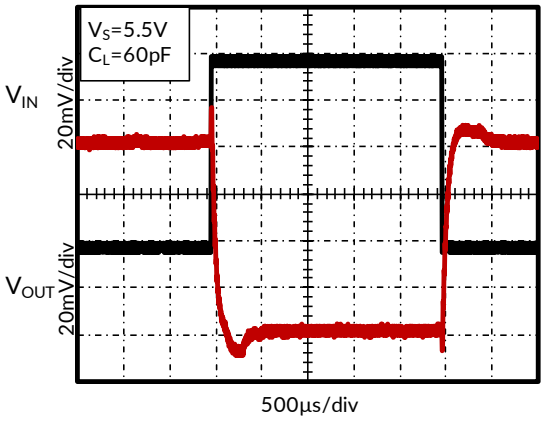


Figure 24. Small-Signal Inverting Pulse Response

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

Unless otherwise indicated: T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L, C_L = 60 pF.

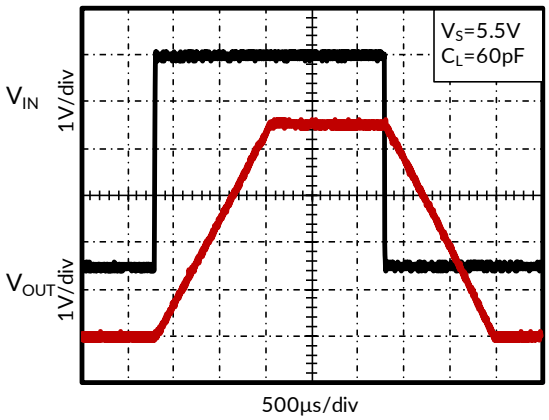


Figure 25. Large-Signal Noninverting Pulse Response

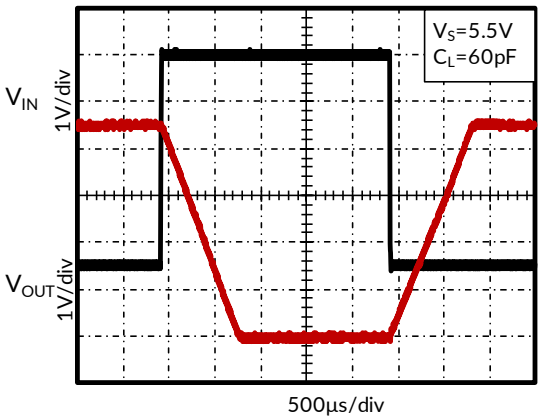


Figure 26. Large-Signal Inverting Pulse Response

7.6 Test Circuits

The test circuits used for the DC and AC tests are shown in Figure 27 and Figure 28. The bypass capacitors are laid out according to the rules discussed in Section 8.5 Supply Bypass.

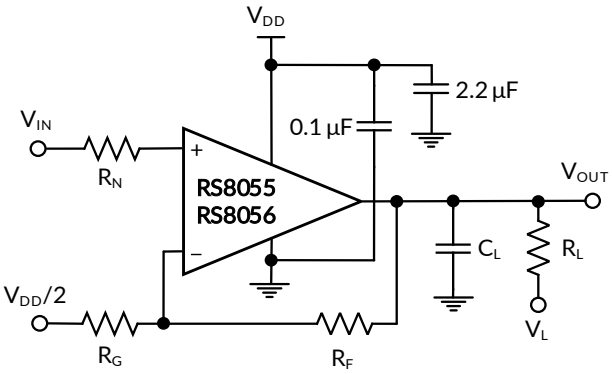


Figure 27. AC and DC Test Circuit for Most Noninverting Gain Conditions

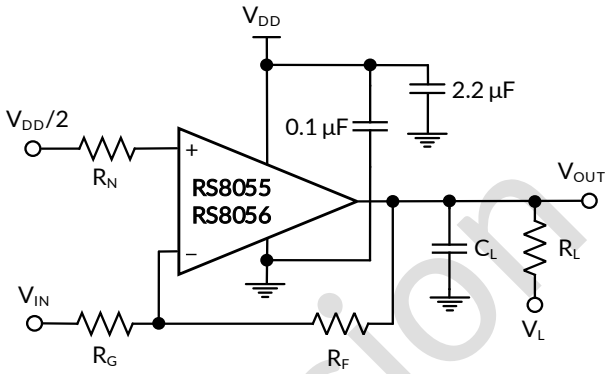


Figure 28. AC and DC Test Circuit for Most Inverting Gain Conditions

8 APPLICATION INFORMATION

The RS8055/RS8056 family of op amps are manufactured using state-of-the-art CMOS process and are specifically designed for low-power, high-precision applications.

8.1 Rail-to-Rail Input

8.1.1 Phase Reversal

The RS8055/RS8056 op amps are designed to prevent phase reversal when the input pins exceed the supply voltages.

8.1.2 Normal Operation

The input stage of the RS8055/RS8056 op amps uses two differential input stages in parallel. One operates at a low Common-mode input voltage (V_{CM}), while the other operates at a high V_{CM}. With this topology, the device operates with a V_{CM} up to 100 mV above V_{DD} and 100 mV below V_{SS}. The input offset voltage is measured at V_{CM} = V_{SS} – 0.1V and V_{DD} + 0.1V to ensure proper operation.

8.2 Rail-to-Rail Output

The output voltage range of the RS8055/RS8056 op amps is 5mV (typical) when R_L = 10 kΩ is connected to V_S/2 and V_S = 1.8V to 5.5V.

8.3 Output Loads and Battery Life

The RS8055/RS8056 op amp has outstanding quiescent current, which supports battery-powered applications.

Heavy resistive loads at the output can cause excessive battery drain. Driving a DC voltage of 2.5V across a 100 kΩ load resistor will cause the supply current to increase by 25 μA, depleting the battery 36 times as fast as I_Q (0.7 μA, typical) alone.

High-frequency signals (fast edge rate) across capacitive loads will also significantly increase supply current. For instance, a 0.1 μF capacitor at the output presents an AC impedance of 15.9 kΩ (1/2πfC) to a 100 Hz sinewave. It can be shown that the average power drawn from the battery by a 5.0 V_{p-p} sinewave (1.77 V_{rms}) under these conditions is

$$P_{Supply} = (V_{DD} - V_{SS})(I_Q + V_{L(p-p)}\, f\, C_L)$$
$$= (5V)(0.7\ \mu A + 5.0\ V_{p-p} \cdot 100\ Hz \cdot 0.1\ \mu F)$$
$$= 3.5\ \mu W + 50\ \mu W$$

This will drain the battery about 15 times as fast as I_Q alone.

8.4 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. While a unity gain buffer (G = +1) is the most sensitive to capacitive loads, all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., >100 pF when G = +1), a small series resistor at the output (R_{ISO} in Figure 29) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitance load.

Figure 30 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For noninverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is 1+|Signal Gain| (e.g., -1 V/V gives G_N = +2 V/V).

After selecting R_{ISO} for your circuit, double-check the resulting frequency response peaking and step response overshoot. Modify R_{ISO}'s value until the response is reasonable.

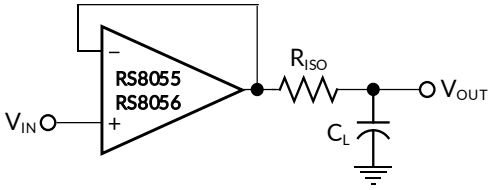


Figure 29. Output Resistor, R_{ISO}, Stabilizes Large Capacitive Loads

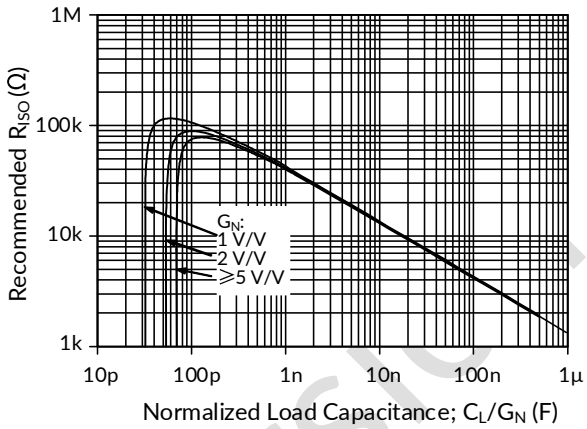


Figure 30. Recommended R_{ISO} Values for Capacitive Loads

8.5 Supply Bypass

With this operational amplifier, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high-frequency performance. It can use a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

8.6 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is 10^{12} Ω. A 5V difference would cause 5 pA of current to flow.

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 31.

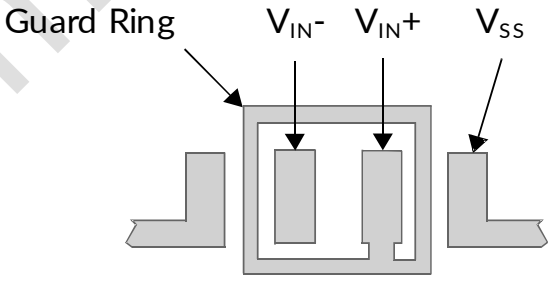


Figure 31. Example Guard Ring Layout for Inverting Gain

1. Noninverting Gain and Unity Gain Buffer:
   a) Connect the noninverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin (VIN-). This biases the guard ring to the Common-mode input voltage.
2. Inverting Gain and Transimpedance Gain Amplifiers (convert current to voltage, such as photo detectors):
   a) Connect the guard ring to the noninverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op amp (e.g., V_{DD}/2 or ground).
   b) Connect the inverting pin (V_{IN}-) to the input with a wire that does not touch the PCB surface.

8.7 Application Circuits

8.7.1 Battery Current Sensing

The RS8055/RS8056 op amps' Common-mode input range, which goes 0.1V beyond both supply rails, supports their use in high-side and low-side battery current sensing applications. The ultra-low quiescent current (0.7 μA, typical) helps prolong battery life and the rail-to-rail output supports detection of low currents.

Figure 32 shows a high-side battery current sensor circuit. The 10Ω resistor is sized to minimize power losses. The battery current (I_{DD}) through the 10Ω resistor causes its top terminal to be more negative than the bottom terminal. This keeps the Common-mode input voltage of the op amp below V_{DD}, which is within its allowed range. The output of the op amp will also be below V_{DD}, which is within its maximum output voltage swing specification.

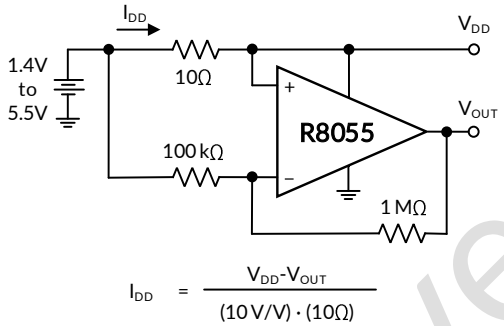


Figure 32. High-Side Battery Current Sensor

8.7.2 Precision Comparator

Use high gain before a comparator to improve the latter's input offset performance. Figure 33 shows a gain of 11 V/V placed before a comparator. The reference voltage, V_{REF}, can be any value between the supply rails.

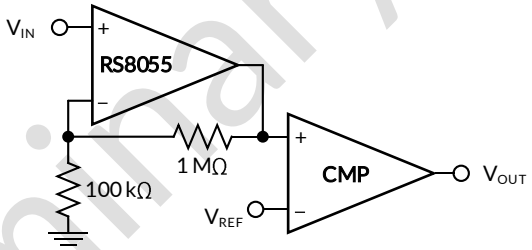
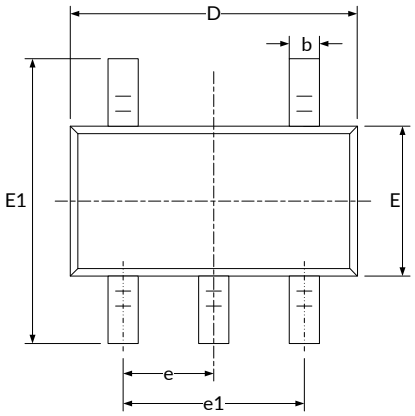
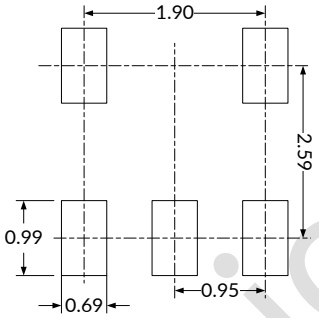


Figure 33. Precision, Noninverting Comparator

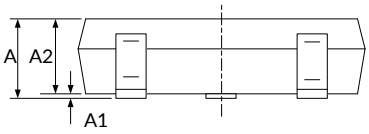
9 PACKAGE OUTLINE DIMENSIONS

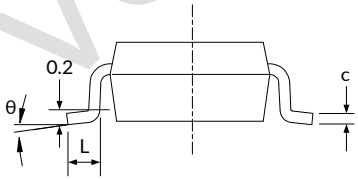
SOT23-5 (3)





RECOMMENDED LAND PATTERN (Unit: mm)



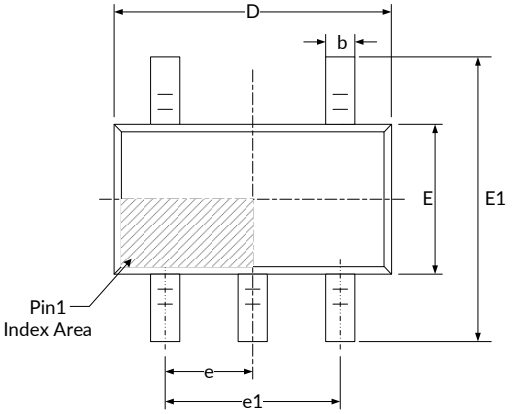


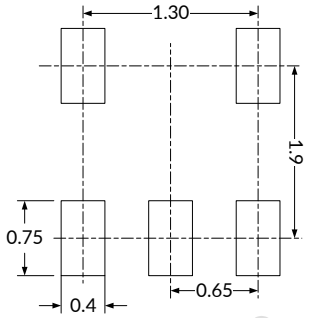
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D (1)	2.820	3.020	0.111	0.119
E (1)	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC) (2)		0.037(BSC) (2)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

NOTE:

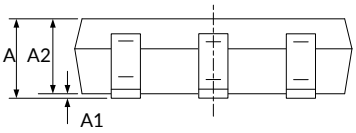
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

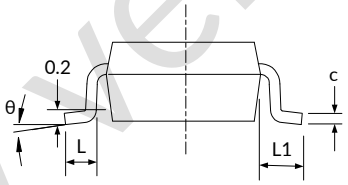
SC70-5 (3)





RECOMMENDED LAND PATTERN (Unit: mm)

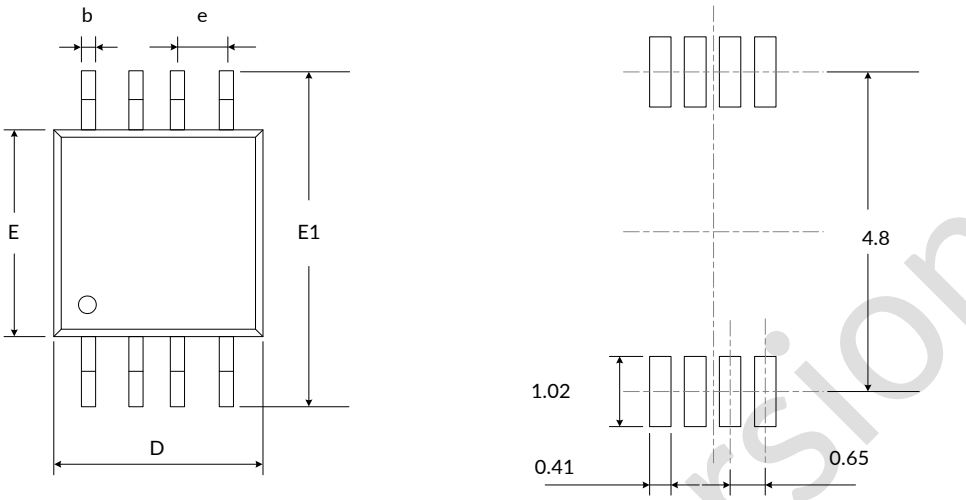




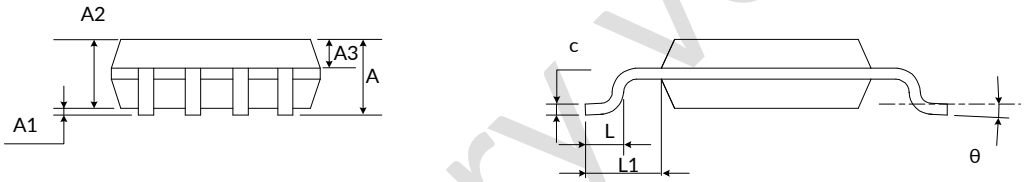
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.150	0.003	0.006
D (1)	2.000	2.200	0.079	0.087
E (1)	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650(BSC) (2)		0.026(BSC) (2)	
e1	1.300(BSC) (2)		0.051(BSC) (2)	
L	0.260	0.460	0.010	0.018
L1	0.525		0.021	
θ	0°	8°	0°	8°

NOTE:
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

MSOP8 (4)



RECOMMENDED LAND PATTERN (Unit: mm)

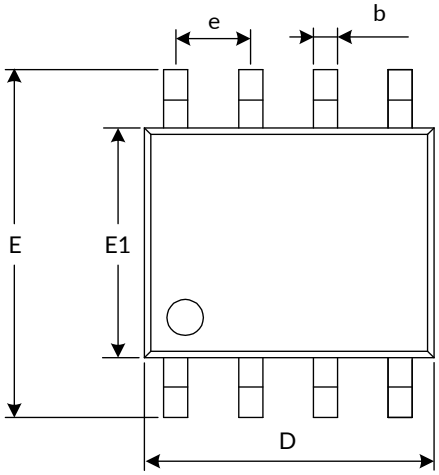


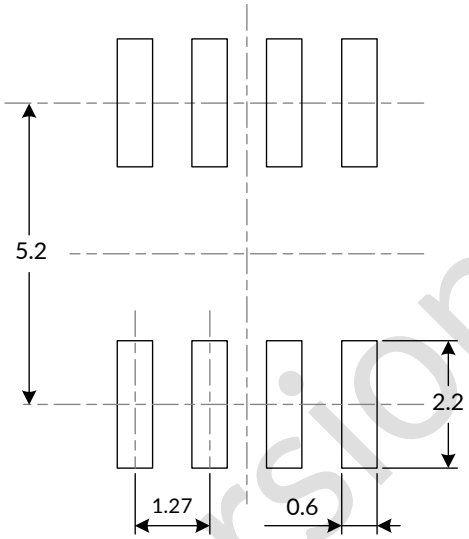
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.100		0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
A3	0.300	0.400	0.012	0.016
b	0.280	0.360	0.011	0.014
c	0.150	0.190	0.006	0.007
D (1)	2.900	3.100	0.114	0.122
e	0.650(BSC) (2)		0.026(BSC) (2)	
E (1)	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.200
L	0.400	0.700	0.016	0.027
L1	0.950(REF) (3)		0.037(REF) (3)	
θ	0°	8°	0°	8°

NOTE:

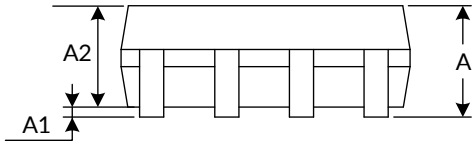
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. REF is the abbreviation for Reference.
4. This drawing is subject to change without notice.

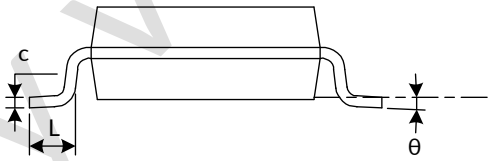
SOP8 (3)





RECOMMENDED LAND PATTERN (Unit: mm)



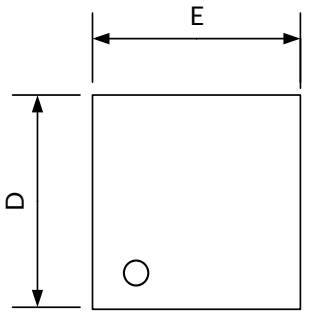


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D (1)	4.800	5.000	0.189	0.197
e	1.270(BSC) (2)		0.050(BSC) (2)	
E	5.800	6.200	0.228	0.244
E1 (1)	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

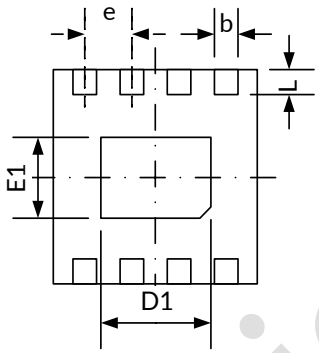
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

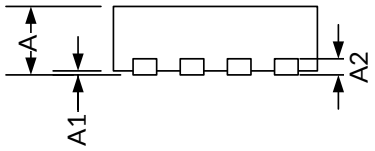
DFN2X2-8 (2)



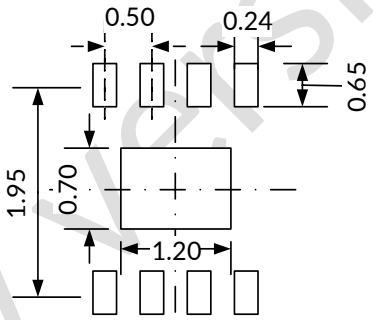
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203(TYP)		0.008(TYP)	
b	0.180	0.300	0.007	0.012
D (1)	1.900	2.100	0.075	0.083
D1	1.100	1.300	0.043	0.051
E (1)	1.900	2.100	0.075	0.083
E1	0.600	0.800	0.024	0.031
e	0.500(TYP)		0.020(TYP)	
L	0.250	0.450	0.010	0.018

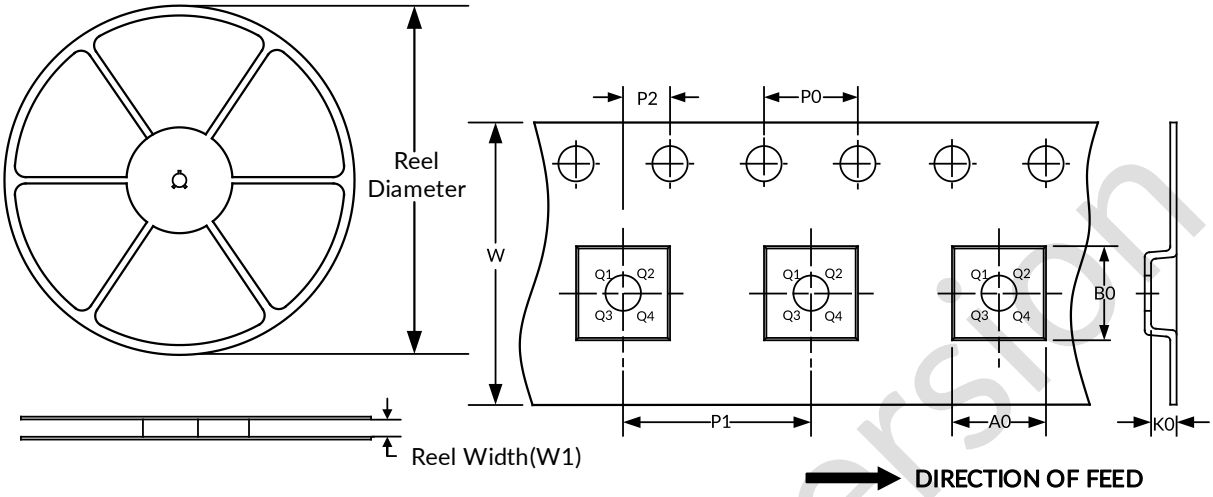
NOTE:

1. Plastic or metal protrusions of 0.075mm maximum per side are not included.
2. This drawing is subject to change without notice.

10 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT23-5	7”	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
SC70-5	7”	9.5	2.25	2.55	1.20	4.0	4.0	2.0	8.0	Q3
MSOP8	13”	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1
SOP8	13”	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
DFN2X2-8	7”	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q2

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

IMPORTANT NOTICE AND DISCLAIMER

Jiangsu RUNIC Technology Co., Ltd. will accurately and reliably provide technical and reliability data (including data sheets), design resources (including reference designs), application or other design advice, WEB tools, safety information and other resources, without warranty of any defect, and will not make any express or implied warranty, including but not limited to the warranty of merchantability Implied warranty that it is suitable for a specific purpose or does not infringe the intellectual property rights of any third party.

These resources are intended for skilled developers designing with RUNIC products You will be solely responsible for: (1) Selecting the appropriate products for your application; (2) Designing, validating and testing your application; (3) Ensuring your application meets applicable standards and any other safety, security or other requirements; (4) RUNIC and the RUNIC logo are registered trademarks of RUNIC INCORPORATED. All trademarks are the property of their respective owners; (5) For change details, review the revision history included in any revised document. The resources are subject to change without notice. Our company will not be liable for the use of this product and the infringement of patents or third-party intellectual property rights due to its use.