

# USB 2.0 + HiFi Audio Switch

## 1 FEATURES

- **Supply Voltage Range: 2.7V to 5.5V**
- **Control Pins Compatible with 1.8V Interfaces**
- **I<sub>CC</sub>: 46µA (TYP) at 5.5V**
- **High-Speed Data Path:**
  - **Input Signal Range: 0V to 3.5V**
  - **R<sub>DS(ON)</sub>: 5Ω (TYP)**
  - **C<sub>ON</sub>: 13pF (TYP)**
  - **Data Rate: USB 2.0-Compliant - up to 480Mbps**
- **Audio Path:**
  - **Input Signal Range: -2V to 2V**
  - **R<sub>DS(ON)</sub>: 1.3Ω (TYP)**
  - **R<sub>FLAT(ON)</sub>: 0.006Ω (TYP)**
  - **THD: 0.002% (TYP) (R<sub>L</sub> = 16Ω/V<sub>IS</sub> = 0.4V<sub>RMS</sub>)**
- **Extended Industrial Temperature Range: -40°C to 85°C**
- **Micro Size Packages: UQFN1.4X1.8-10**

## 3 DESCRIPTIONS

The RS2237 is a double-pole/double-throw (DPDT) analog switch for routing high speed differential data and audio. The high-speed data path is compliant with High Speed USB 2.0, Full Speed USB 1.1, Low Speed USB 1.0 and any generic UART protocol. The multi-purpose audio path is capable of passing signals with negative voltages as low as 2 V below ground and features shunt resistors to reduce Pop and Click noise in the audio system.

The RS2237 is available UQFN1.4X1.8-10 package. It operates over an ambient temperature range of -40°C to 85°C.

**Device Information <sup>(1)</sup>**

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS2237	UQFN1.4X1.8-10	1.80mm×1.40mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

## 2 APPLICATIONS

- Smartphones
- Tablets
- USB 2.0 Hosts/Peripherals
- Audio/High-Speed Data Switching

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## 4 REVISION HISTORY

Note: Page numbers for previous revisions may differ from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2025/11/17	Preliminary version completed
A.0.1	2026/01/12	Update HBM value in ESD Ratings

Preliminary version

**5 PACKAGE/ORDERING INFORMATION <sup>(1)</sup>**

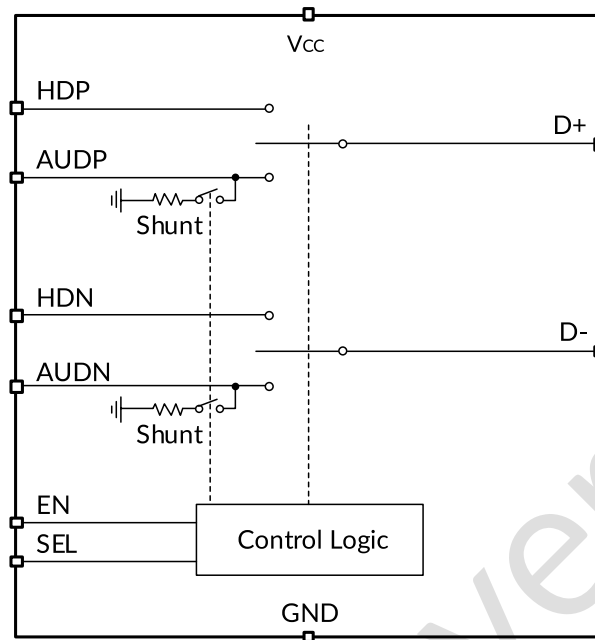
PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING <sup>(2)</sup>	MSL <sup>(3)</sup>	PACKAGE OPTION
RS2237	RS2237YUTAQK10	-40°C ~85°C	UQFN1.4X1.8-10	2237	MSL3	Tape and Reel, 4000

## NOTE:

- (1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.
- (2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.
- (3) Runic classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with Runic if your end application is quite critical to the preconditioning setting or if you have special requirement.

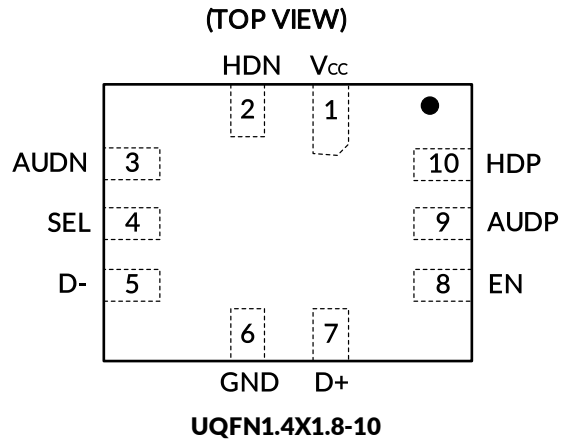
Preliminary version

## 6 FUNCTIONAL BLOCK DIAGRAM


**FUNCTION TABLE**

EN	SEL	Shunt Status	D+/D- Function
0	X	ON	No Connect
1	0	OFF	AUDP/AUDN
1	1	ON	HDP/HDN

## 7 PIN CONFIGURATIONS



### PIN DESCRIPTION

NAME	PIN	FUNCTION
	UQFN1.4X1.8-10	
V <sub>CC</sub>	1	Power Supply
HDN	2	High Speed Differential Data (-)
AUDN	3	Audio Signal (-)
SEL	4	Function Select
D-	5	Audio/Data Common I/O (-)
GND	6	Ground
D+	7	Audio/Data Common I/O (+)
EN	8	Chip Enable
AUDP	9	Audio Signal (+)
HDP	10	High Speed Differential Data (+)

## 8 SPECIFICATIONS

### 8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

SYMBOL	PARAMETER	MIN	MAX	UNIT	
V <sub>CC</sub>	Positive DC Supply Voltage Range	-0.3	6	V	
V <sub>IS</sub>	Analog Input/Output Voltage Range	HDP, HDN	3.7	V	
		AUDP, AUDN	-2	3.7	V
		D+, D-	-2	3.7	V
V <sub>IN</sub>	Digital Control Pin Voltage on EN, SEL	-0.3	V <sub>CC</sub> + 0.3	V	
θ <sub>JA</sub>	Package thermal impedance <sup>(2)</sup>		115	°C/W	
T <sub>J</sub>	Junction Temperature		150	°C	
T <sub>stg</sub>	Storage Temperature Range	-65	150	°C	
	Lead Temperature (Soldering, 10s)		260	°C	

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) The package thermal impedance is calculated in accordance with JEDEC-51.

### 8.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

		VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	Human-Body Model (HBM)	±4000	V
		Charged-Device Model (CDM)	±1000	V



#### ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	MIN	MAX	UNIT	
V <sub>CC</sub>	Supply Voltage	2.7	5.5	V	
V <sub>IS</sub>	Switch Input/Output Voltage Range	HDP, HDN	0	3.5	V
		AUDP, AUDN	-2	2	V
		D+, D-	-2	3.5	V
V <sub>IN</sub>	Digital Control Input Voltage Range	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature	-40	85	°C	

## 8.4 Electrical Characteristics

$V_{CC} = 2.7V$  to  $5.5V$ , FULL =  $-40^{\circ}C$  to  $85^{\circ}C$ . Typical values are at  $T_A = +25^{\circ}C$  (unless otherwise noted).

PARAMETER	SYMBOL	CONDITIONS	$T_A$	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
<b>DC Electrical Characteristic</b>							
<b>Power Supply</b>							
Supply Current	$I_{CC}$	$V_{CC} = 2.7V, I_{IS} = 0mA$	25°C		26	35	$\mu A$
			FULL			50	$\mu A$
		$V_{CC} = 5.5V, I_{IS} = 0mA$	25°C		46	55	$\mu A$
			FULL			70	$\mu A$
Input High Voltage	$V_{IH}$		FULL	1.8			V
Input Low Voltage	$V_{IL}$		FULL			0.4	V
Input Hysteresis	$V_{IHYS}$	$V_{CC} = 2.7V$	25°C		220		mV
Leakage Current	$I_{IN}$	$V_{CC} = 2.7V$ to $5.5V$	FULL			$\pm 50$	nA
<b>Audio Switch (AUDP/AUDN ↔ D+/D-)</b>							
On-Resistance	$R_{ON}$	$V_{CC} = 3.0V$ to $5.5V, V_{IS} = -2.0V$ to $2V, I_{IS} = 50mA$	25°C		1.3	1.6	$\Omega$
			FULL			1.8	
On-Resistance Matching - Between Channels	$\Delta R_{ON}$	$V_{CC} = 3.0V$ to $5.5V, V_{IS} = -2.0V$ to $2V, I_{IS} = 50mA$	25°C		0.02		$\Omega$
On-Resistance Flatness	$R_{FLAT(ON)}$	$V_{CC} = 3.0V$ to $5.5V, V_{IS} = -2.0V$ to $2V, I_{IS} = 50mA$	25°C		0.006		$\Omega$
Shunt Resistance	$R_{SH}$		25°C		760		$\Omega$
<b>Data Switch (HDP/HDN ↔ D+/D-)</b>							
On-Resistance	$R_{ON}$	$V_{CC} = 3.0V$ to $5.5V, V_{IS} = 0V$ to $1.7V, I_{IS} = 15mA$	25°C		5	6	$\Omega$
			FULL			7	$\Omega$
On-Resistance Matching - Between Channels	$\Delta R_{ON}$	$V_{CC} = 3.0V$ to $5.5V, V_{IS} = 0V$ to $1.7V, I_{IS} = 15mA$	25°C		0.05		$\Omega$
On-Resistance Flatness	$R_{FLAT(ON)}$	$V_{CC} = 3.0V$ to $5.5V, V_{IS} = 0V$ to $1.7V, I_{IS} = 15mA$	25°C		0.004		$\Omega$
Off-State Leakage	$I_{SW(OFF)}$	$V_{IS} = 0V$ to $3.5V$ , see Figure 7	FULL			$\pm 100$	nA
On-State Leakage	$I_{SW(ON)}$	$V_{IS} = 0V$ to $3.5V$ , see Figure 8	FULL			$\pm 100$	nA
<b>AC Electrical Characteristics</b>							
<b>Audio Switch (AUDP/AUDN ↔ D+/D-)</b>							
Audio THD	THD	$f = 20Hz$ to $20kHz, V_{IS} = 0.4V_{RMS}, DC$ bias = $0V$	$R_L = 16\Omega$	25°C		0.002	%
			$R_L = 32\Omega$	25°C		0.001	
		$f = 20Hz$ to $20kHz, V_{IS} = 4V_{P-P}, DC$ bias = $0V$	$R_L = 16\Omega$	25°C		0.002	%
			$R_L = 32\Omega$	25°C		0.002	
Power Supply Ripple Rejection	PSRR	From $V_{CC}$ to AUDP/AUDN, $f = 217Hz, R_L = 16\Omega$	25°C		-110		dB
<b>Data Switch (HDP/HDN ↔ D+/D-)</b>							
Equivalent On Capacitance	$C_{ON}$	Switch on, $f = 1MHz$	25°C		13		pF
Equivalent Off Capacitance	$C_{OFF}$	Switch off, $f = 1MHz$	25°C		6		pF
Differential Insertion Loss	$D_{IL}$	$f = 10MHz$ , See Figure 9	25°C		-0.62		dB
		$f = 800MHz$ , See Figure 9	25°C		-3.54		
Differential Off Isolation	$D_{ISO}$	$f = 10MHz$ , See Figure 10	25°C		-50		dB
		$f = 800MHz$ , See Figure 10	25°C		-27		
Differential Crosstalk	$D_{CTK}$	$f = 10MHz$ , See Figure 11	25°C		-58		dB
		$f = 800MHz$ , See Figure 11	25°C		-27		

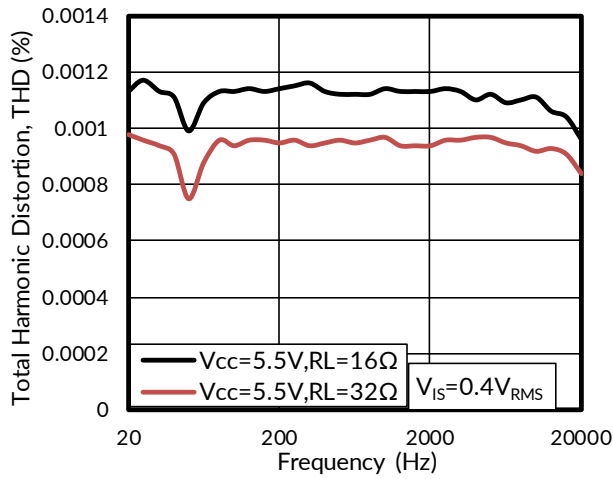
Power Supply Rejection Ratio	PSRR	PSRR From $V_{CC}$ to D+/D-, $f=217\text{Hz}$ , $R_L=50\Omega$	25°C		-110		dB
<b>Dynamic Timing</b>							
Propagation Delay <sup>(3)</sup>	$t_{PD}$	$V_{NOH}$ or $V_{NCH} = 0V$ , $R_L = 50\Omega$	25°C		1		ns
Bit - to - Bit Skew <sup>(4)</sup>	$t_{SK(B-B)}$	Within the same differential channel, see Figure 12	25°C		500		ps
Turn - On Time	$t_{ON}$	$V_{IS} = 1V$ , $R_L = 50\Omega$ , $C_L$ = 7pF (fixture only), see Figure 13	EN or SEL to AUDP/AUDN	25°C		11.5	ms
			EN or SEL to HDP/HDN	25°C		0.02	
Turn - Off Time	$t_{OFF}$	$V_{IS} = 1V$ , $R_L = 50\Omega$ , $C_L$ = 7pF (fixture only), see Figure 13	EN or SEL to AUDP/AUDN	25°C		10.5	$\mu\text{s}$
			EN or SEL to HDP/HDN	25°C		0.3	

**NOTE:**

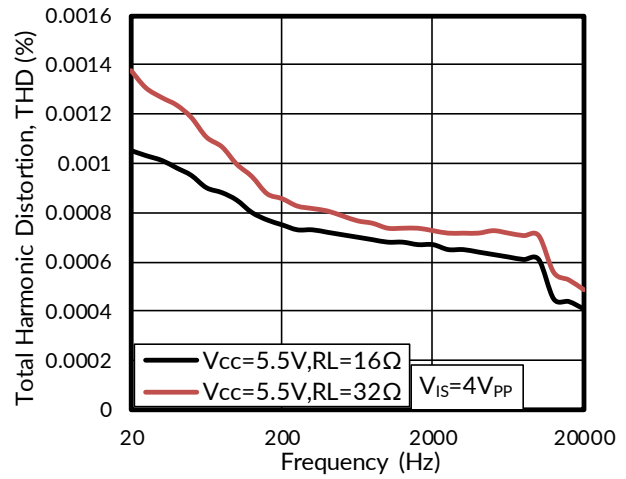
- (1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
- (2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
- (3) No delays other than the RC network formed by the load resistance and the load capacitance of the switch are added on the bus. For a 10pF load, this delay is 5ns which is much smaller than rise and fall time of typical driving systems. Propagation delays on the bus are determined by the driving circuit on the driving side and its interactions with the load of the driven side.
- (4) This parameter is ensured by design and/or characterization and is not tested in production.

### 8.5 Typical Characteristics

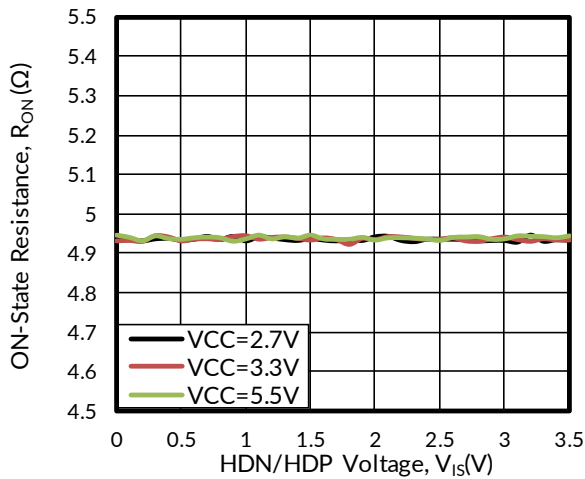
NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.



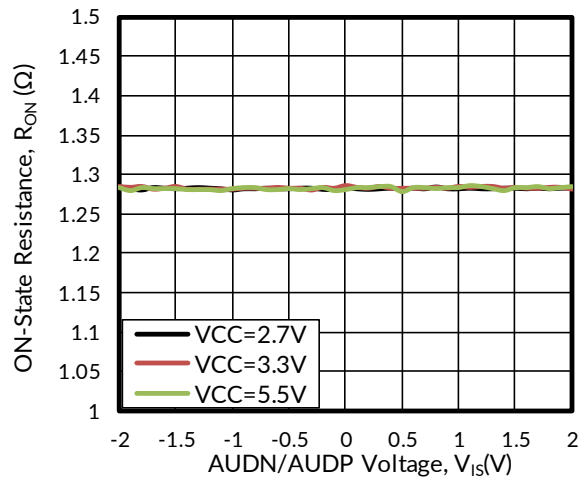
**Figure 1. Total Harmonic Distortion vs Frequency**



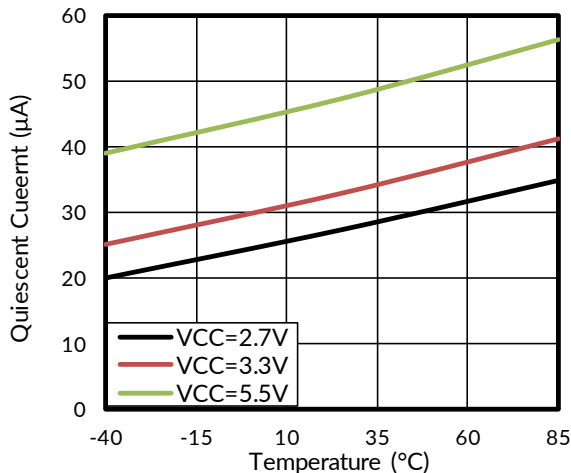
**Figure 2. Total Harmonic Distortion vs Frequency**



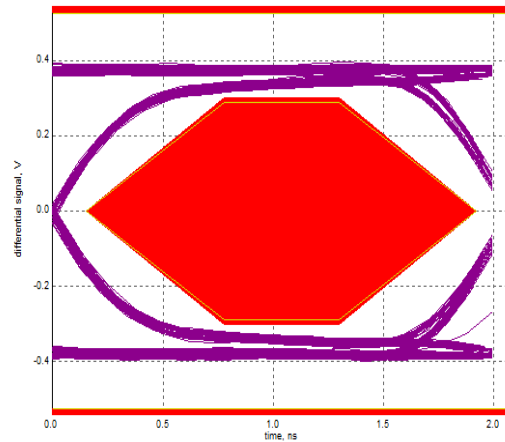
**Figure 3. ON-State Resistance vs HDN/HDP Voltage**



**Figure 4. ON-State Resistance vs AUDN/AUDP Voltage**

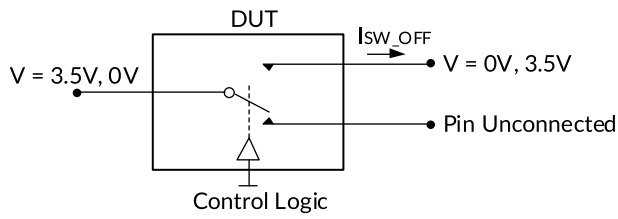
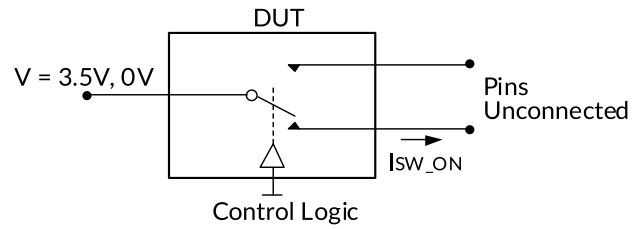
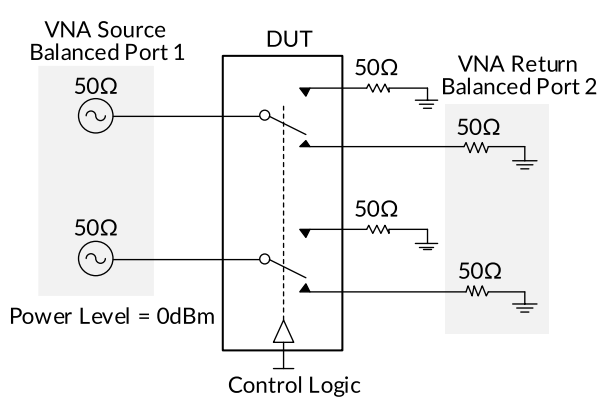
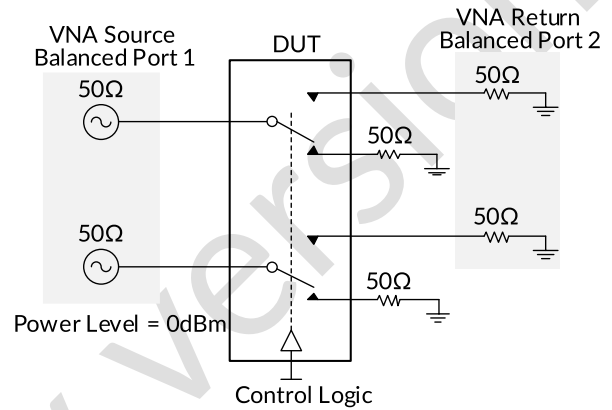
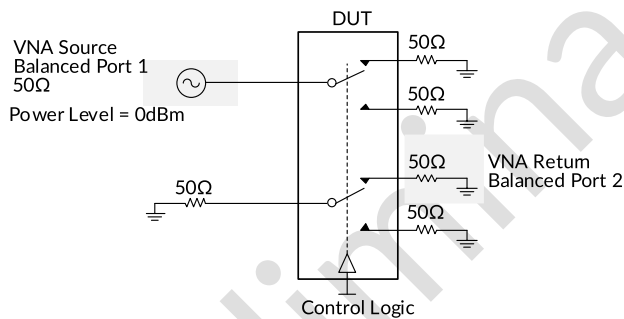
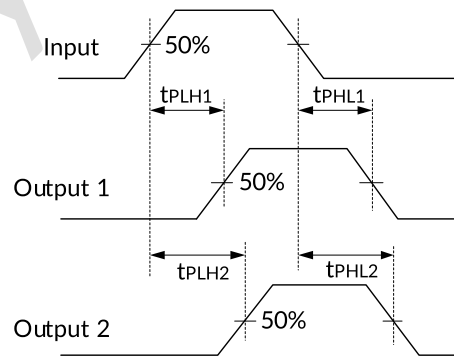
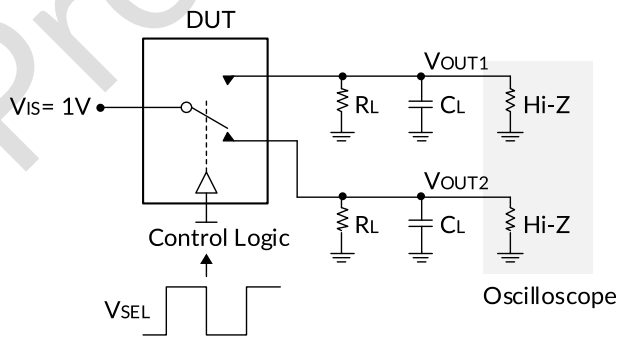
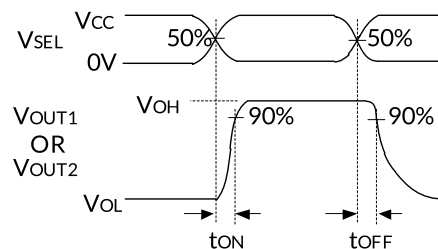


**Figure 5. Quiescent Current vs Temperature**



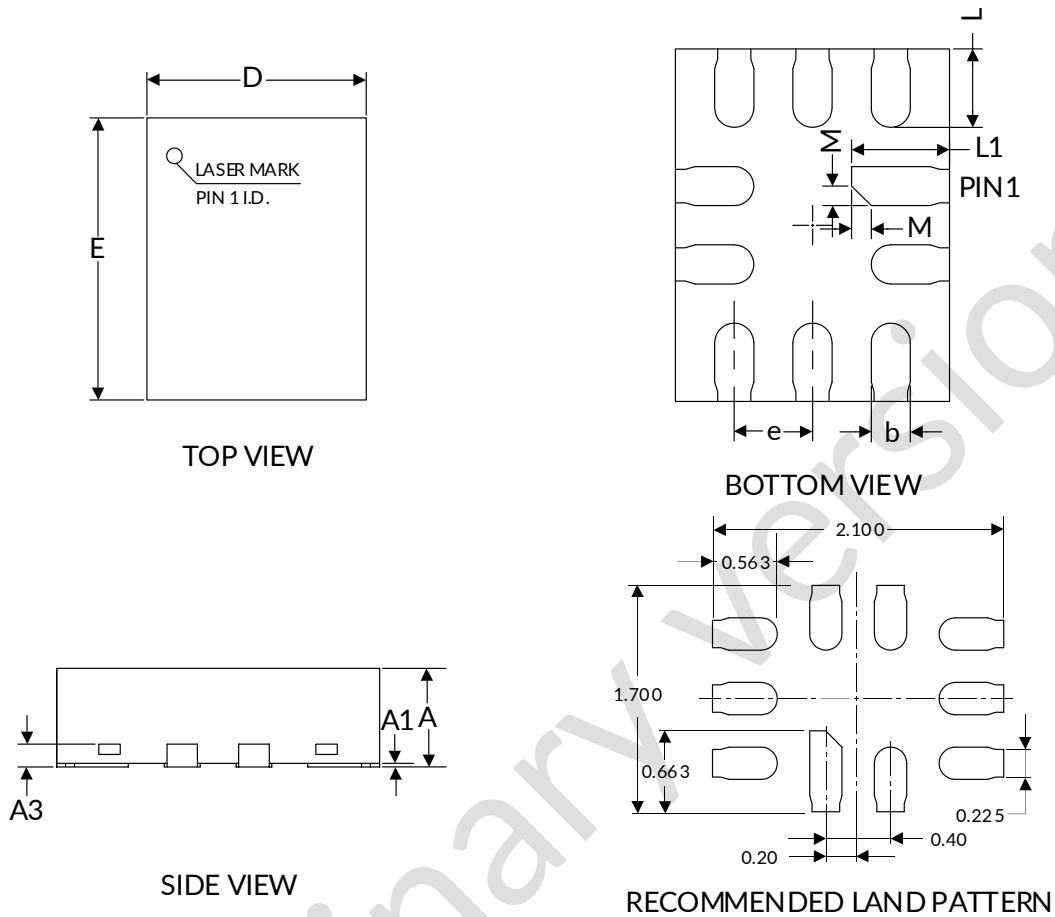
**Figure 6. Eye Pattern**

## 9 PARAMETER MEASUREMENT INFORMATION


**Figure 7. Off-State Leakage**

**Figure 8. On-State Leakage**

**Figure 9. Differential Insertion Loss ( $S_{DD21}$ )**

**Figure 10. Differential Off Isolation ( $S_{DD21}$ )**

**Figure 11. Differential Crosstalk ( $S_{DD21}$ )**

**Figure 12. Bit-to-Bit and Channel-to-Channel Skew**

**Figure 13. Turn-On and Turn-Off Times**


# 10 PACKAGE OUTLINE DIMENSIONS

## UQFN1.4X1.8-10<sup>(3)</sup>



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A <sup>(1)</sup>	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.127 REF <sup>(2)</sup>		0.005 REF <sup>(2)</sup>	
b	0.150	0.250	0.006	0.010
D <sup>(1)</sup>	1.350	1.450	0.053	0.057
E <sup>(1)</sup>	1.750	1.850	0.069	0.073
e	0.300	0.500	0.012	0.020
L	0.350	0.450	0.014	0.018
L1	0.450	0.550	0.018	0.022
M	0.100 REF <sup>(2)</sup>		0.004 REF <sup>(2)</sup>	

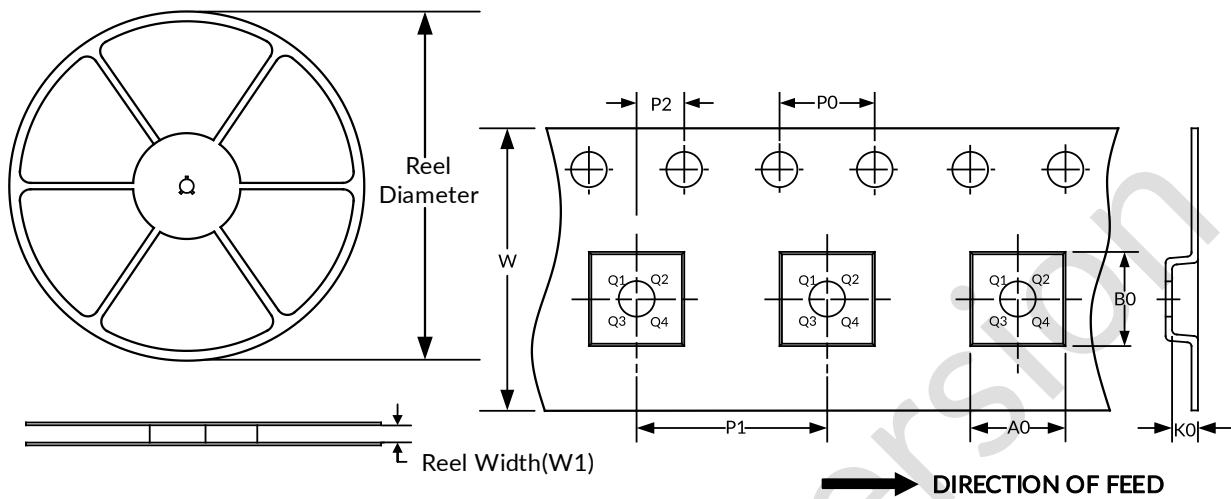
**NOTE:**

1. Plastic or metal protrusions of 0.075mm maximum per side are not included.
2. REF is the abbreviation for Reference.
3. This drawing is subject to change without notice.

# 11 TAPE AND REEL INFORMATION

## REEL DIMENSIONS

## TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

### KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
UQFN1.4X1.8-10	7"	9.0	1.60	2.00	0.85	4.0	4.0	2.0	8.0	Q1

NOTE:

1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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