RS895X Precision Comparator Family

1 FEATURES

- **1.8V to 5.5V Supply Range**
- **Precision Input Offset voltage 500µV**
- **Power-on Reset (POR) for Known Start-Up**
- **Rail-to-Rail Input with Fault-Tolerance**
- **95ns Typical Propagation Delay**
- **Low Quiescent Current 30µA per Channel**
- **Low Input Bias Current 12pA**
- **Push-Pull Output Option**
- **Full -40°C to +125°C Temperature Range**
- **Alternate Single Pinout (RS8950)**

2 APPLICATIONS

- **Appliances**
- **Building Automation**
- **Factory Automation & Control**
- **Motor Drives**
- **Infotainment & Cluster**

3 DESCRIPTIONS

The RS895X is a family of single, dual and quad channel comparators. The family offers low input offset voltage, fault-tolerant inputs and an excellent speed-to-power combination. The family has a propagation delay of 95ns with a quiescent supply current of only 30µA per channel.

The family also includes a Power-on Reset (POR) feature that makes sure the output is in a known state until the minimum supply voltage has been reached. This prevents output transients during system power-up and power-down.

These comparators also feature fault-tolerant inputs that can go up to 6V without damage and with no output phase inversion. This family of comparators is designed for precision voltage monitoring in harsh, noisy environments.

The RS895X have a push-pull output stage capable of sinking and sourcing many milliamps of current to drive LEDs or capacitive loads for MOSFET gates.

The RS8950 and RS8951 are alternate pinouts of the single device.

The family is specified for the Industrial temperature range of -40°C to +125°C and are available in a standard leaded and leadless packages.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS8950	SOT23-5	1.60mm×2.92mm
	SC70-5	2.10mm×1.25mm
RS8951	SOT23-5	1.60mm×2.92mm
	SC70-5	2.10mm×1.25mm
RS8952	SOP8	4.90mm×3.90mm
	MSOP8	3.00mm×3.00mm
RS8954	SOP14	8.65mm×3.90mm
	TSSOP14	5.00mm×4.40mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2025/12/23	Preliminary version completed
A.1	2026/04/17	Initial version completed

5 PACKAGE/ORDERING INFORMATION (1)

Orderable Device	Package Type	Pin	Channel	Op Temp(°C)	Device Marking (2)	MSL (3)	Package Qty
RS8950XF	SOT23-5	5	1	-40°C ~125°C	8950	MSL3	Tape and Reel, 3000
RS8950XC5	SC70-5 (4)	5	1	-40°C ~125°C	8950	MSL3	Tape and Reel, 3000
RS8951XF	SOT23-5	5	1	-40°C ~125°C	8951	MSL3	Tape and Reel, 3000
RS8951XC5	SC70-5 (4)	5	1	-40°C ~125°C	8951	MSL3	Tape and Reel, 3000
RS8952XK	SOP8	8	2	-40°C ~125°C	RS8952	MSL3	Tape and Reel, 4000
RS8952XM	MSOP8	8	2	-40°C ~125°C	RS8952	MSL3	Tape and Reel, 4000
RS8954XP	SOP14	14	4	-40°C ~125°C	RS8954	MSL3	Tape and Reel, 4000
RS8954XQ	TSSOP14	14	4	-40°C ~125°C	RS8954	MSL3	Tape and Reel, 4000

NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

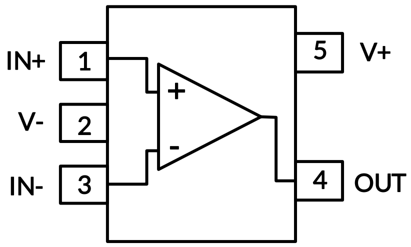
(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

(4) Equivalent to SOT353.

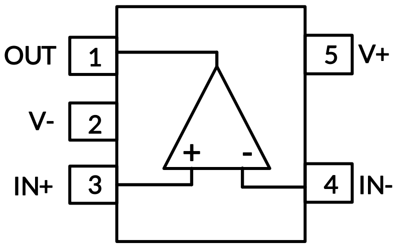
6 PIN CONFIGURATION AND FUNCTIONS

RS8950



SOT23-5/SC70-5

RS8951



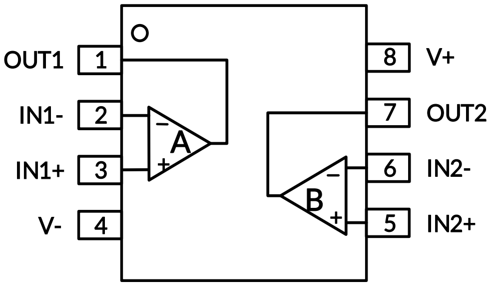
SOT23-5/SC70-5

PIN DESCRIPTION

NAME	PIN		I/O (1)	DESCRIPTION
	RS8950	RS8951		
	SOT23-5/SC70-5	SOT23-5/SC70-5		
IN+	1	3	I	Non-Inverting (Positive) Input
IN-	3	4	I	Inverting (Negative) Input
OUT	4	1	O	Output
V+	5	5	-	Positive Power Supply
V-	2	2	-	Negative Power Supply

(1) I=Input, O=Output.

RS8952



SOP8/MSOP8

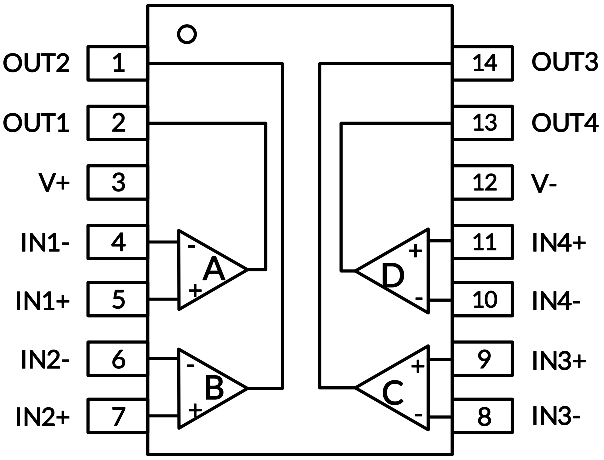
PIN DESCRIPTION

NAME	PIN	I/O (1)	DESCRIPTION
	SOP8/MSOP8		
OUT1	1	O	Output pin of the comparator 1
IN1-	2	I	Inverting input pin of comparator 1
IN1+	3	I	Noninverting input pin of comparator 1
V-	4	-	Negative (low) supply
IN2+	5	I	Noninverting input pin of comparator 2
IN2-	6	I	Inverting input pin of comparator 2
OUT2	7	O	Output pin of the comparator 2
V+	8	-	Positive supply

(1) I=Input, O=Output.

PIN CONFIGURATION AND FUNCTIONS

RS8954



SOP14/TSSOP14

PIN DESCRIPTION

NAME	PIN	I/O [1]	DESCRIPTION
	SOP14/TSSOP14		
OUT2	1	O	Output pin of the comparator 2
OUT1	2	O	Output pin of the comparator 1
V+	3	-	Positive supply
IN1-	4	I	Negative input pin of the comparator 1
IN1+	5	I	Positive input pin of the comparator 1
IN2-	6	I	Negative input pin of the comparator 2
IN2+	7	I	Positive input pin of the comparator 2
IN3-	8	I	Negative input pin of the comparator 3
IN3+	9	I	Positive input pin of the comparator 3
IN4-	10	I	Negative input pin of the comparator 4
IN4+	11	I	Positive input pin of the comparator 4
V-	12	-	Negative supply
OUT4	13	O	Output pin of the comparator 4
OUT3	14	O	Output pin of the comparator 3

(1) I=Input, O=Output.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Voltage	Supply, V_S=(V+) - (V-)		-0.3	6	V
	Input pins (IN+, IN-) from V- (2)		-0.3	6	
	Output (OUT) from V–		-0.3	(V+) + 0.3	
Current	Current into Input pins (IN+, IN–)		-10	10	mA
	Output short-circuit duration (3)			10	s
θ_{JA}	Package thermal impedance (4)	SOT23-5		230	°C/W
		SC70-5		380	
		SOP8		110	
		MSOP8		165	
		SOP14		105	
		TSSOP14		90	
Temperature	Junction, T_J (5)			150	°C
	Storage, T_{stg}		-65	150	

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Input terminals are diode-clamped to (V–). Input signals that can swing more than 0.3V beyond the supply rails must be current-limited to 10mA or less. Additionally, Inputs (IN+, IN–) can be greater than V+ and OUT as long as the input is within the –0.3V to 6V range

(3) Short-circuit to V- or V+. Short circuits from outputs can cause excessive heating and eventual destruction.

(4) The package thermal impedance is calculated in accordance with JESD-51.

(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), per JESD22-a114	±2000	V
		Charged-Device Model (CDM), per ANSI/ESDA/JEDEC JS-002-2022	±1000	

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage: V_S= (V+) - (V-)	1.8	5.5	V
Input voltage range (IN+, IN–) from (V–)	-0.2	5.7	V
Ambient temperature, T_A	-40	125	°C

7.4 Electrical Characteristics

For V_S (Total Supply Voltage) = (V+) – (V–) = 5V, V_{CM} = (V–) at T_A = 25°C, Full =-40°C to +125°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	T_A	RS895X			
				MIN(2)	TYP(3)	MAX(2)	UNIT
OFFSET VOLTAGE							
V_{OS}	Input Offset Voltage	V_S = 1.8V and 5V	25°C	-2	±0.5	2	mV
			Full	-3		3	
dV_{IO}/dT	Input Offset Voltage Drift	V_S = 1.8V and 5V	Full		±2		µV/°C
POWER SUPPLY							
I_Q	Quiescent Current per Channel	V_S = 1.8V and 5V, No Load, Output Low	25°C		30	40	µA
			Full			50	
PSRR	Power-Supply Rejection Ratio	V_S = 1.8V to 5V	25°C	75	90		dB
			Full	70			
INPUT BIAS CURRENT							
I_B	Input Bias Current	$V_{CM} = V_S/2$	25°C		12		pA
I_{OS}	Input Offset Current	$V_{CM} = V_S/2$	25°C		12		pA
INPUT VOLTAGE RANGE							
$V_{CM\text{-}Range}$	Common-Mode Voltage Rang	V_S = 1.8V and 5V	Full	(V-)-0.2		(V+)+0.2	V
CMRR	Common-Mode Rejection Ratio	V_S = 5V, (V–) – 0.2V < V_{CM} < (V+) + 0.2V	Full	60	70		dB
CMRR	Common-Mode Rejection Ratio	V_S = 1.8V, (V–) – 0.2V < V_{CM} < (V+) + 0.2V	Full	50	60		dB
OUTPUT							
V_{OL}	Voltage Swing from (V–)	I_{SINK} = 4mA	25°C		70	110	mV
			Full			150	
V_{OH}	Voltage Swing from (V+)	I_{SOURCE} = 4mA	25°C		60	110	mV
			Full			140	
I_{SC}	Short-Circuit Current	V_S = 5V, Sinking	25°C	80	100		mA
		V_S = 5V, Sourcing	25°C	80	100		
$T_{PD\text{-}LH}$	Propagation Delay Time, Low-to-High	V_{ID} = 100mV; Delay from mid-point of input to mid-point of output	25°C		95		ns
$T_{PD\text{-}HL}$	Propagation Delay Time, High-to-Low	V_{ID} = -100mV; Delay from mid-point of input to mid-point of output	25°C		95		ns
T_{FALL}	5V Output Fall Time, 50% to 50%	V_{ID} = 1V	25°C		3		ns
T_{RISE}	5V Output Rise Time, 50% to 50%	V_{ID} = 1V	25°C		3		ns
POWER ON TIME							
P_{ON}	Power On Time	V_S = 1.8V and 5V, V_{CM} = (V–), V_{ID} = –0.1V, Delay from $V_S/2$ to $V_{OUT}/2$ (R_L=1KΩ, C_L=100pF)	25°C		15		µs

NOTE:

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

7.5 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

T_A = 25°C, V_S = 5V, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

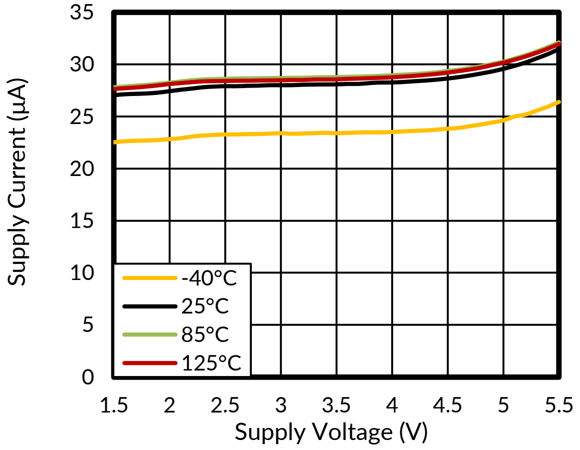


Figure 1. Supply Current vs Supply Voltage

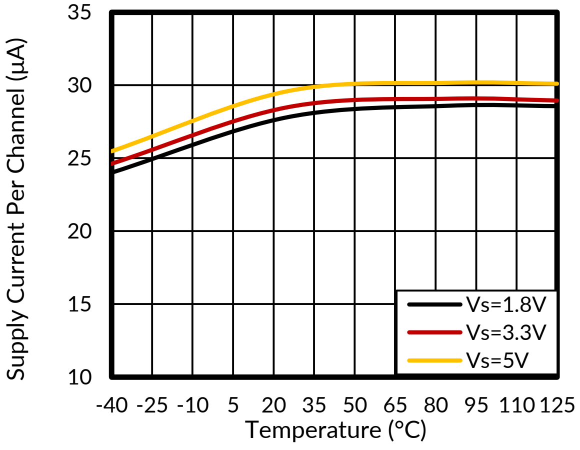


Figure 2. Supply Current vs Temperature

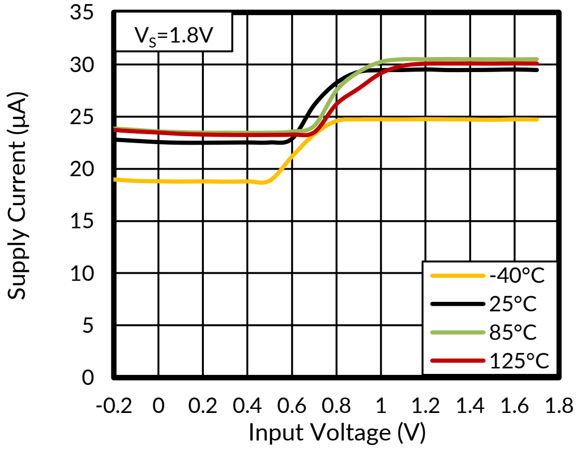


Figure 3. Supply Current vs Input Voltage

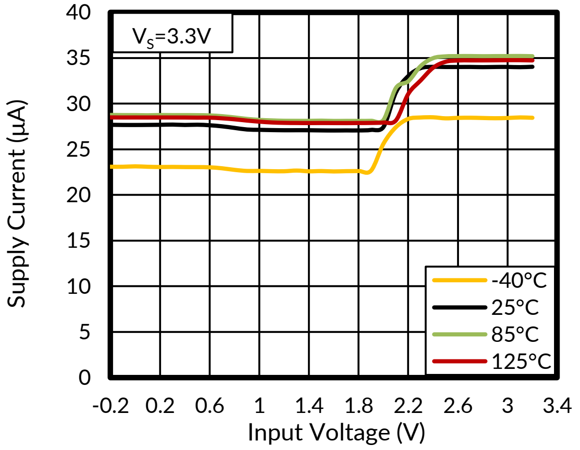


Figure 4. Supply Current vs Input Voltage

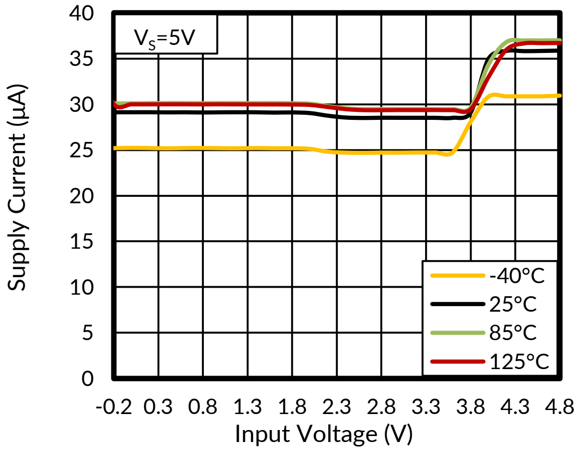


Figure 5. Supply Current vs Input Voltage

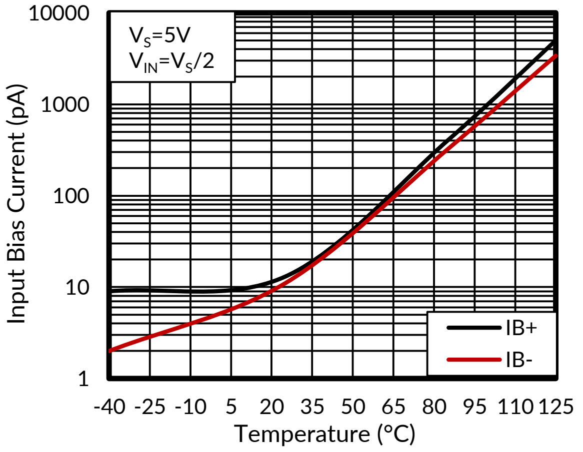


Figure 6. Input Bias Current vs Temperature

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

T_A = 25°C, V_S = 5V, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

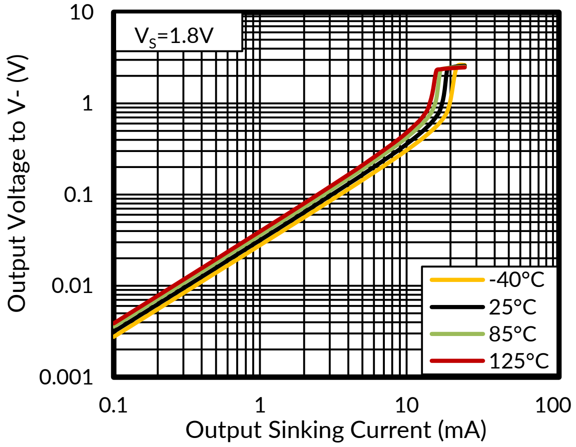


Figure 7. Output Voltage vs Output Sinking Current

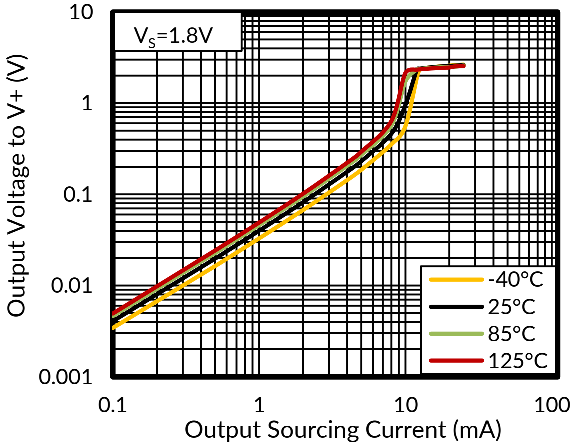


Figure 8. Output Voltage vs Output Sourcing Current

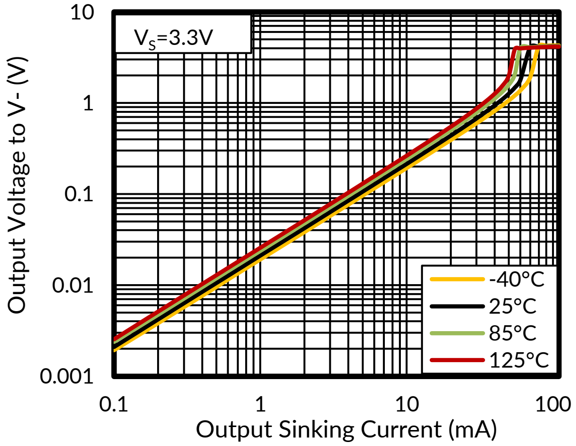


Figure 9. Output Voltage vs Output Sinking Current

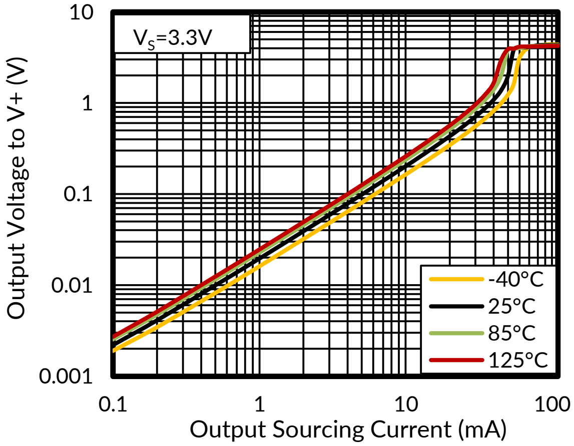


Figure 10. Output Voltage vs Output Sourcing Current

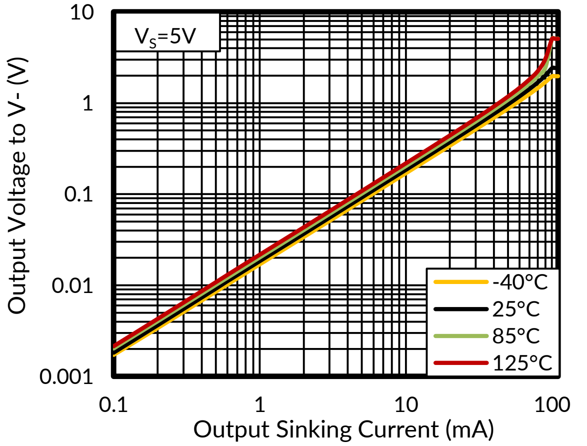


Figure 11. Output Voltage vs Output Sinking Current

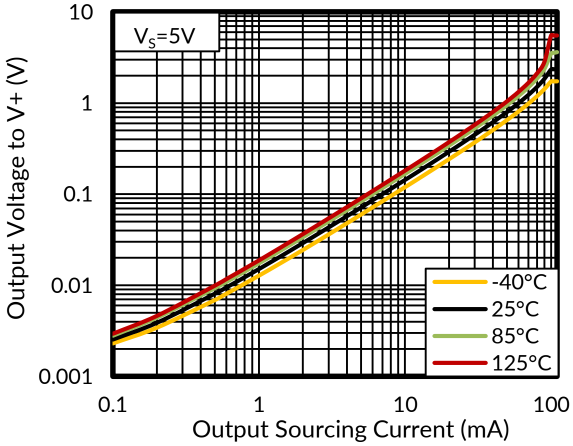


Figure 12. Output Voltage vs Output Sourcing Current

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

T_A = 25°C, V_S = 5V, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

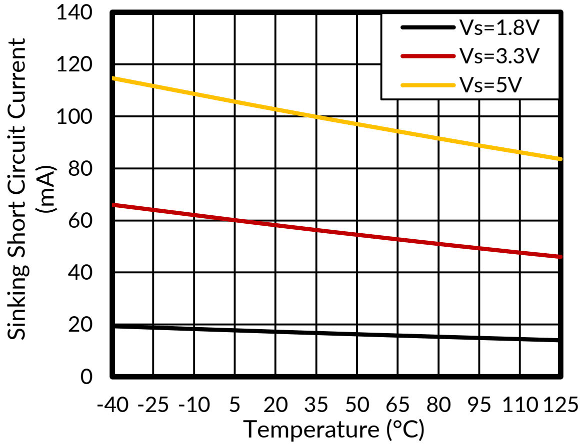


Figure 13. Sinking Short Circuit Current vs Temperature

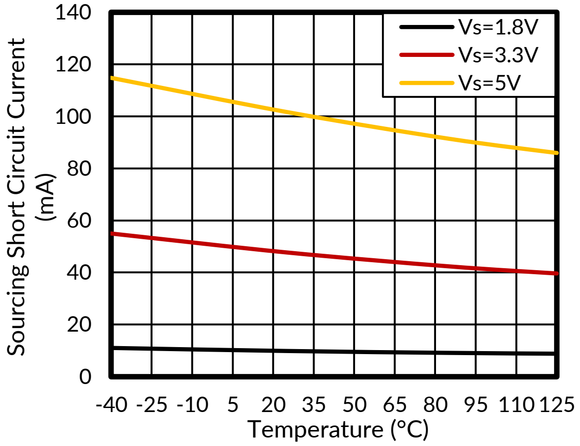


Figure 14. Sourcing Short Circuit Current vs Temperature

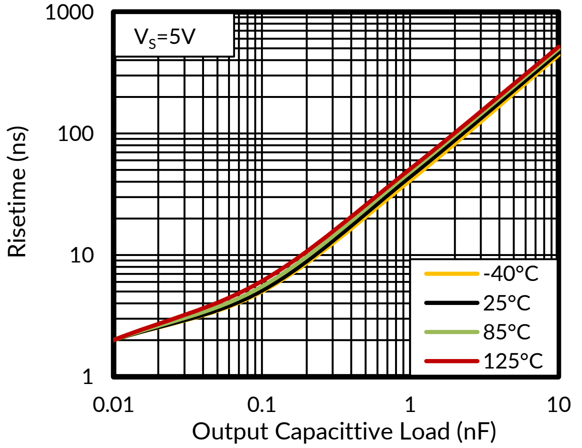


Figure 15. Risetime vs Capacitive Load

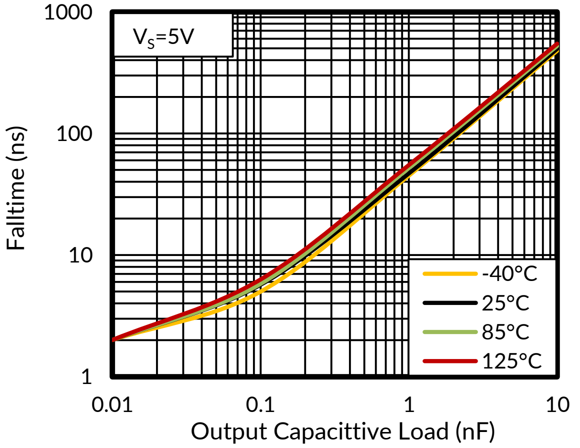


Figure 16. Falltime vs Capacitive Load

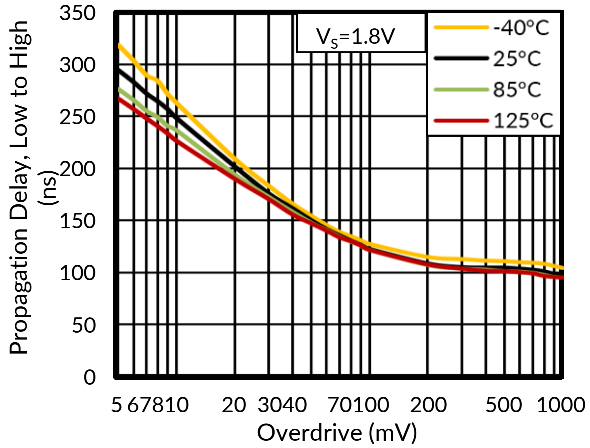


Figure 17. Low to High Propagation Delay vs Input Overdrive Voltage

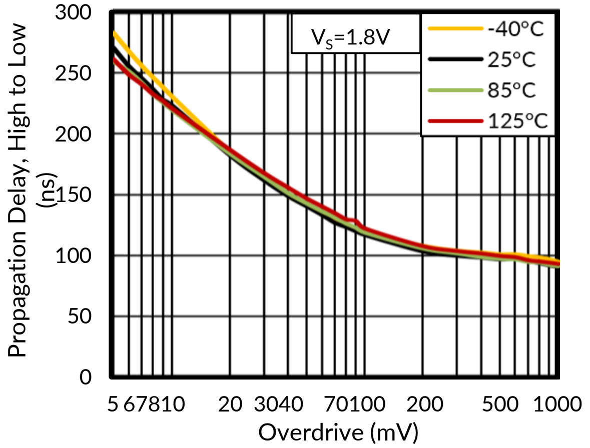


Figure 18. High to Low Propagation Delay vs Input Overdrive Voltage

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

T_A = 25°C, V_S = 5V, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

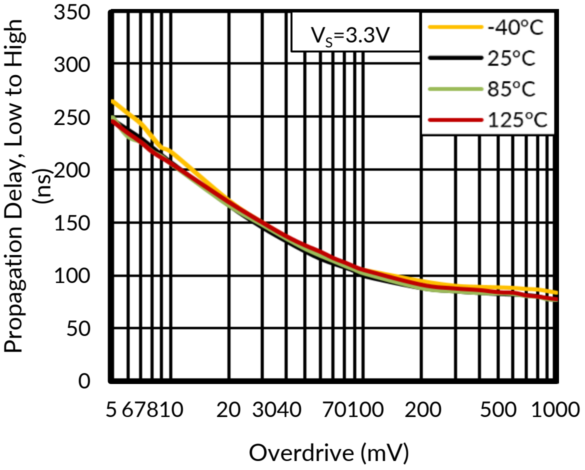


Figure 19. Low to High Propagation Delay vs Input Overdrive Voltage

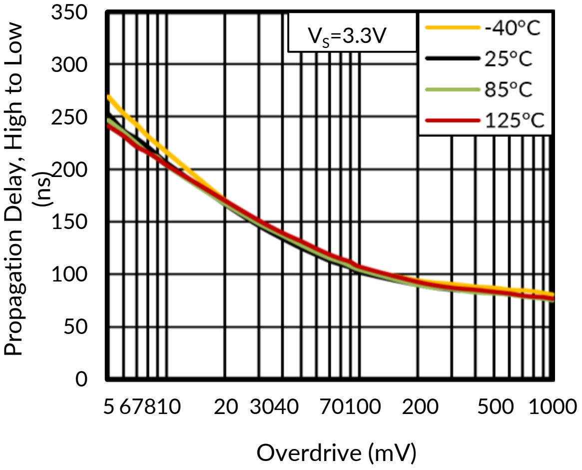


Figure 20. High to Low Propagation Delay vs Input Overdrive Voltage

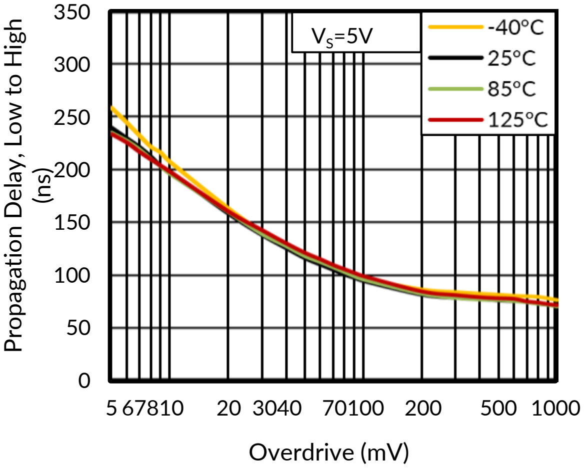


Figure 21. Low to High Propagation Delay vs Input Overdrive Voltage

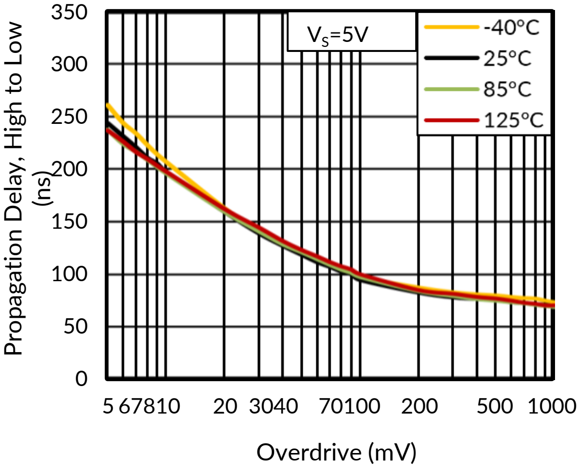


Figure 22. High to Low Propagation Delay vs Input Overdrive Voltage

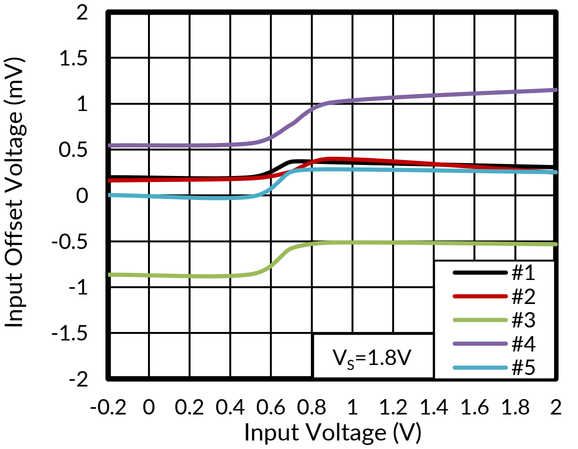


Figure 23. Offset Voltage vs Input Voltage at -40°C

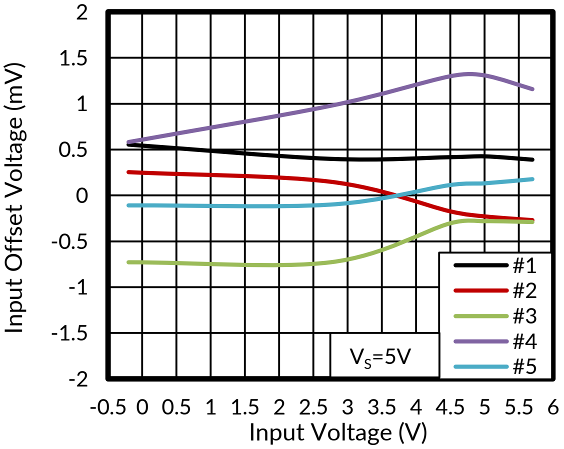


Figure 24. Offset Voltage vs Input Voltage at -40°C

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

T_A = 25°C, V_S = 5V, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

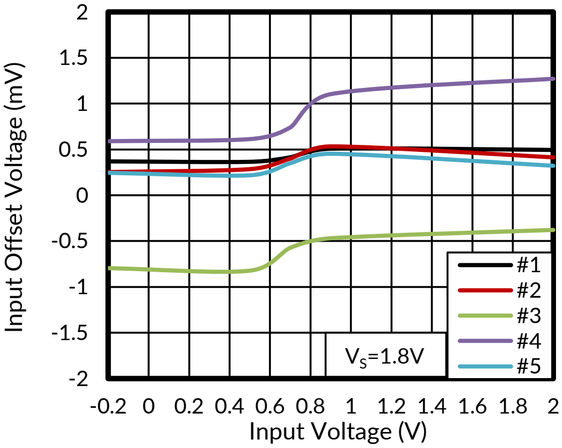


Figure 25. Offset Voltage vs Input Voltage at 25°C

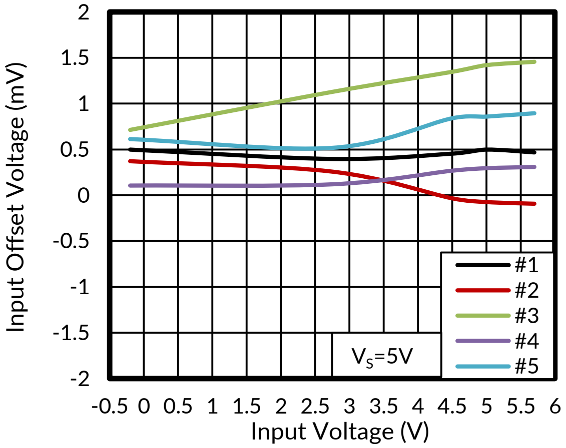


Figure 26. Offset Voltage vs Input Voltage at 25°C

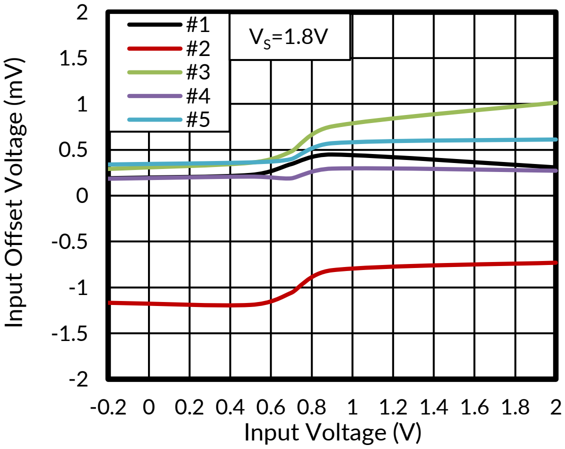


Figure 27. Offset Voltage vs Input Voltage at 125°C

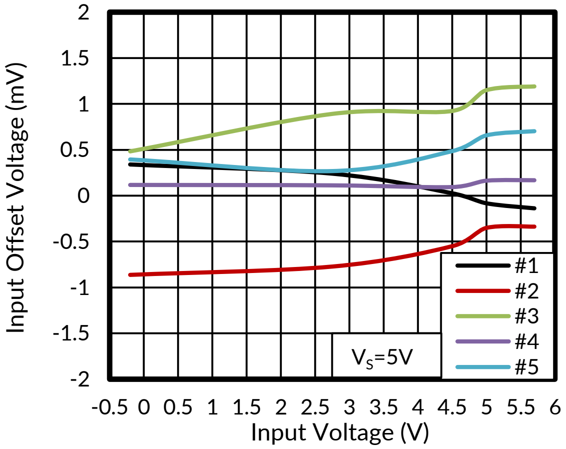


Figure 28. Offset Voltage vs Input Voltage at 125°C

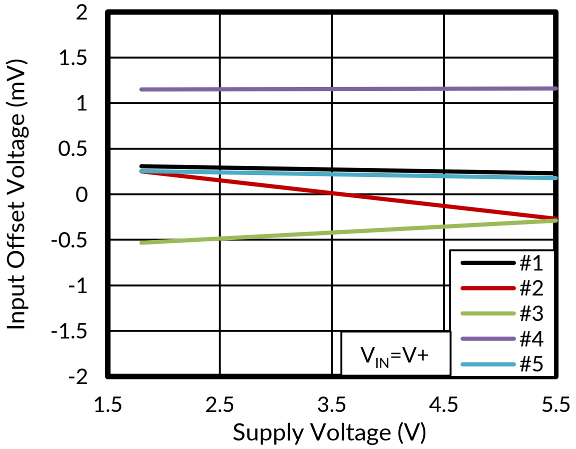


Figure 29. Input Offset Voltage vs Supply Voltage at -40°C

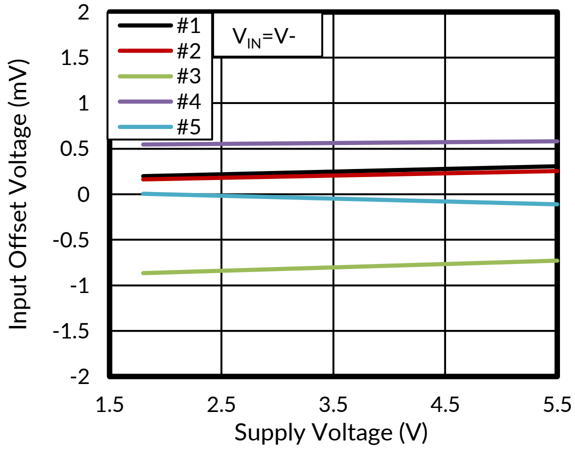


Figure 30. Input Offset Voltage vs Supply Voltage at -40°C

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

T_A = 25°C, V_S = 5V, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

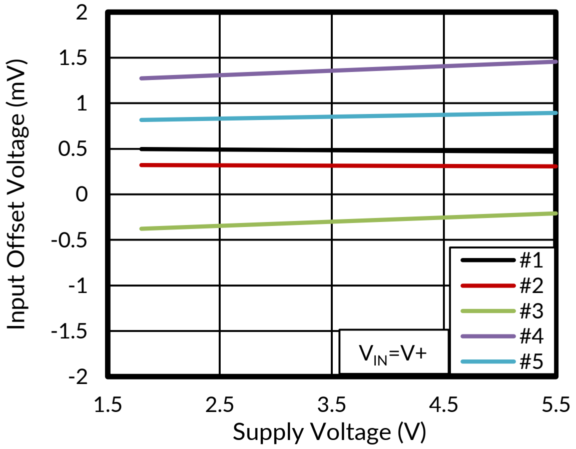


Figure 31. Input Offset Voltage vs Supply Voltage at 25°C

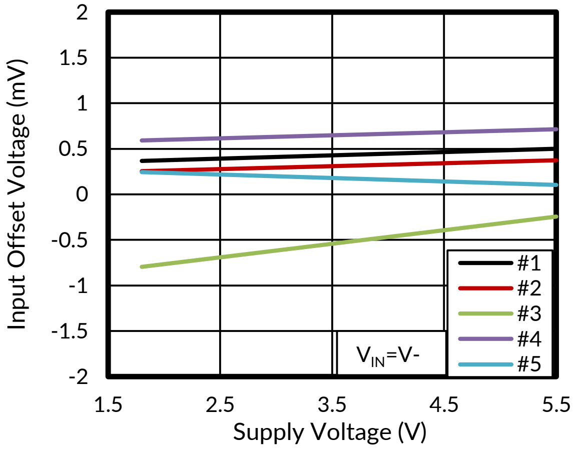


Figure 32. Input Offset Voltage vs Supply Voltage at 25°C

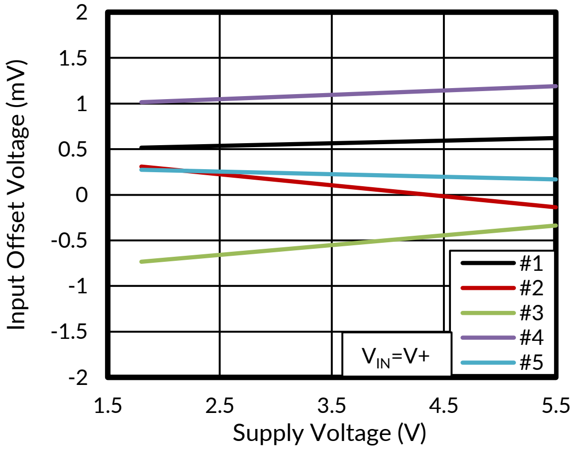


Figure 33. Input Offset Voltage vs Supply Voltage at 125°C

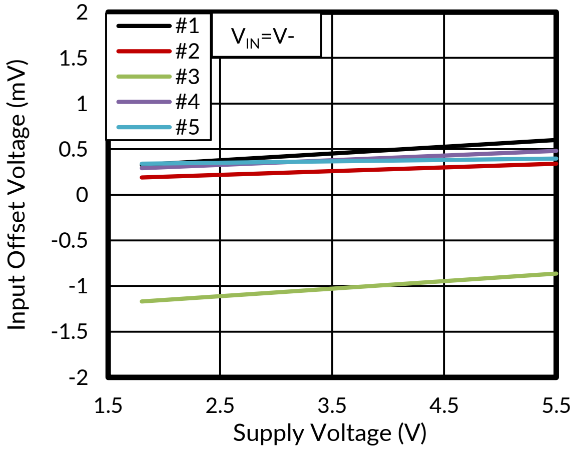


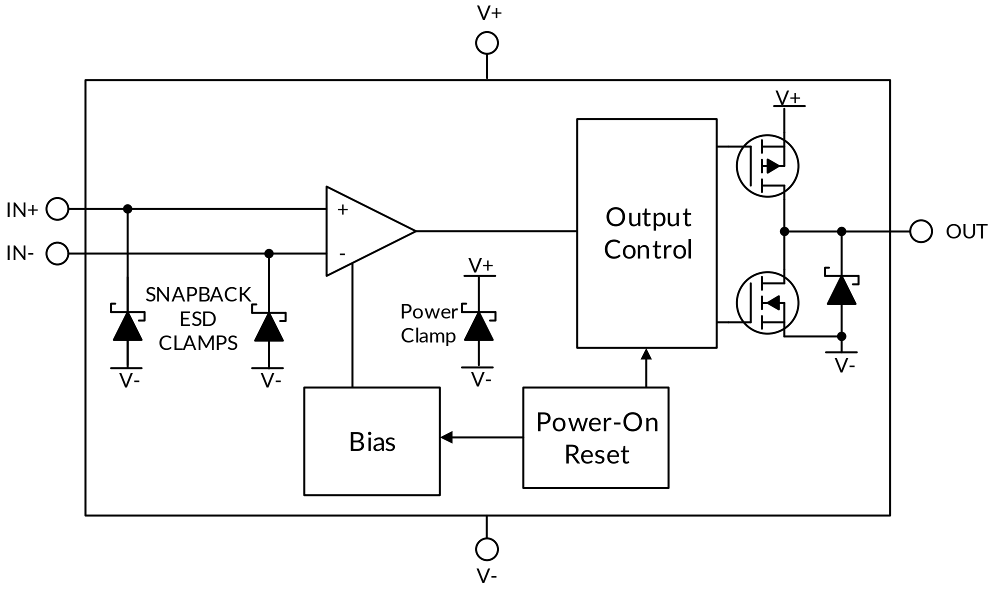
Figure 34. Input Offset Voltage vs Supply Voltage at 125°C

8 DETAILED DESCRIPTION

8.1 Overview

The RS895X devices are micro-power comparators with push-pull outputs and low input offset voltage. Operating down to 1.8V while consuming only 30µA per channel, the RS895X is designed for portable, automotive and industrial applications. An internal power-on reset circuit makes sure that the output remains in a known state during power-up and power-down while fail-safe inputs can tolerate input transients without damage or false outputs.

8.2 Functional Block Diagram



8.3 Feature Description

The RS895X devices are micro-power comparators that have low input offset voltages and are capable of operating at low voltages. The RS895X family feature a rail-to-rail input stage capable of operating up to 200mV beyond the power supply rails. The comparators also feature push-pull output stage options and Power-on Reset for known start-up conditions.

8.4 Device Functional Modes

8.4.1 Outputs

8.4.1.1 RS8952 and RS8954 Push-Pull Output

The RS895X features a push-pull output stage capable of both sinking and sourcing current. This allows driving loads such as LED's and MOSFET gates, as well as eliminating the need for a power-wasting external pull-up resistor. The push-pull output must never be connected to another output.

Unused push-pull outputs must be left floating, and never tied to a supply, ground, or another output. While an individual output can typically sink and source up to 100mA, the total combined current for all channels must be less than 200mA.

8.4.2 Power-On Reset (POR)

The RS895X has an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply (Vs) is ramping up or down, the POR circuitry is activated for up to 15µs after the minimum supply voltage threshold of 1.5V is crossed, or immediately when the supply voltage drops below 1.5V. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input (V_{ID}).

The POR circuit keeps the output high impedance (HI-Z) during the POR period (t_{on}).

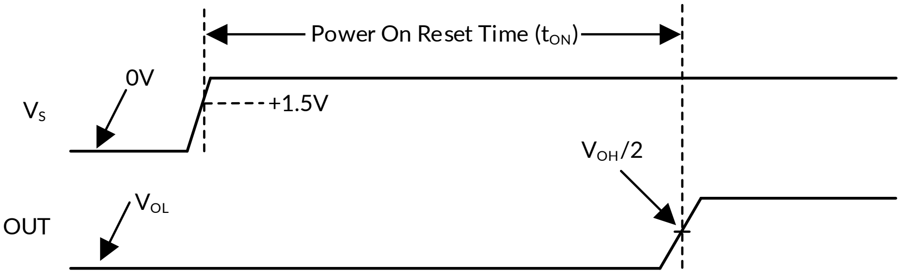


Figure 35. Power-On Reset Timing Diagram

Note that an open collector output voltage rises with the pull-up voltage during the POR period.

For the RS895X push-pull output devices, the output is "floating" during the POR period. A light pull-up (to V+) or pull-down (to V-) resistor (recommended the resistance value should be kept higher than 500kΩ) can be used to pre-bias the output condition to prevent a floating output.

8.4.3 Inputs

8.4.3.1 Rail to Rail Input

The RS895X input voltage range extends from 200mV below V- to 200mV above V+. The differential input voltage (V_{ID}) can be any voltage within these limits. No phase-inversion of the comparator output occurs when the input pins exceed V+ or V-.

8.4.3.2 Fault Tolerant Inputs

The RS895X inputs are fault tolerant up to 5.5V independent of V_S. Fault tolerant is defined as maintaining the same high input impedance when V_S is unpowered or within the recommended operating ranges.

The fault tolerant inputs can be any value between 0V and 5.5V, even while V_S is zero or ramping up or down. This feature avoids power sequencing issues as long as the input voltage range and supply voltage are within the specified ranges. This is possible since the inputs are not clamped to V+ and the input current maintains the value even when a higher voltage is applied to the inputs.

As long as one of the input pins remains within the valid input range, and the supply voltage is valid and not in POR, the output state is correct.

The following is a summary of input voltage excursions and the outcomes:

1. When both IN- and IN+ are within the specified input voltage range:
    a. If IN- is higher than IN+ and the offset voltage, the output is low.
    b. If IN- is lower than IN+ and the offset voltage, the output is high.
2. When IN- is higher than the specified input voltage range and IN+ is within the specified voltage range, the output is low.
3. When IN+ is higher than the specified input voltage range and IN- is within the specified input voltage range, the output is high.
4. When IN- and IN+ are both outside the specified input voltage range, the output is indeterminate (random). Do not operate in this region.

Even with the fault tolerant feature, RUNIC strongly recommends keeping the inputs within the specified input voltage range during normal system operation to maintain data sheet specifications. Operating outside the specified input range can cause changes in specifications such as propagation delay and input bias current, which can lead to unpredictable behavior.

8.4.3.3 Input Protection

The input bias current is typically 12pA for input voltages between V+ and V-. The comparator inputs are protected from negative voltage by the internal ESD diodes connected to V-. As the input voltage goes under V-, or above the input Absolute Maximum ratings, the protection diodes become forward biased and begin to conduct causing the input bias current to increase exponentially. Input bias current doubles for each 10°C temperature increase.

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, RUNIC recommends adding a current-limiting resistor in series with the input to limit any transient currents when the clamps conduct. See the ESD section for more information.

8.4.4 ESD Protection

The RS895X family incorporates internal ESD protection circuits on all pins. The inputs, and the open-drain output, use a proprietary "snapback" type ESD clamp from each pin to V-, which allows the pins to exceed the supply voltage (V+). While shown as Zener diodes, snapback "short" and go low impedance (like an SCR) when the threshold is exceeded, as opposed to clamping to a defined voltage like a Zener.

The RS895X protection consists of a ESD clamp between the output and V- and the output must not exceed the supply rails because of the push-pull output.

If the inputs are to be connected to a low impedance source, RUNIC recommends adding a current-limiting resistor in series with the input to limit input currents when the clamps conduct. The current must be limited 10mA or less. This series resistance can be part of any resistive input dividers or networks. RUNIC does not specify the performance of the ESD clamps and external clamping must be added if the inputs or output can exceed the maximum ratings as part of normal operation.

8.4.5 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency oscillations as the device triggers on it's own internal wideband noise. Instead, the inputs must be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage, or even V+ as long as the input is directly connected to the V+ pin to avoid transients.

8.4.6 Hysteresis

The RS895X family does not have internal hysteresis. Due to the wide effective bandwidth and low input offset voltage, there is a possibility for the output to "chatter" (oscillate) when the absolute differential voltage near zero as the comparator triggers on internal wideband noise. This is normal comparator behavior and is expected. RUNIC recommends that the user add external hysteresis if slow moving signals are expected. See Section 9.1.2 in the following section.

9 APPLICATION AND IMPLEMENTATION

Information in the following applications sections is not part of the RUNIC component specification, and RUNIC does not warrant its accuracy or completeness. RUNIC's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Basic Comparator Definitions

9.1.1.1 Operation

The basic comparator compares the input voltage (V_{IN}) on one input to a reference voltage (V_{REF}) on the other input. In the Comparator Timing Diagram example below, if V_{IN} is less than V_{REF}, the output voltage (V_O) is logic low (V_{OL}). If V_{IN} is greater than V_{REF}, the output voltage (V_O) is at logic high (V_{OH}). Output Conditions summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

Table 1. Output Conditions

Inputs Condition	Output
IN+ > IN-	HIGH (V_{OH})
IN+ = IN-	Indeterminate (chatters - see Hysteresis)
IN+ < IN	LOW (V_{OL})

9.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as t_{pLH} and t_{pHL} in Figure 36 and is measured from the mid-point of the input to the midpoint of the output.

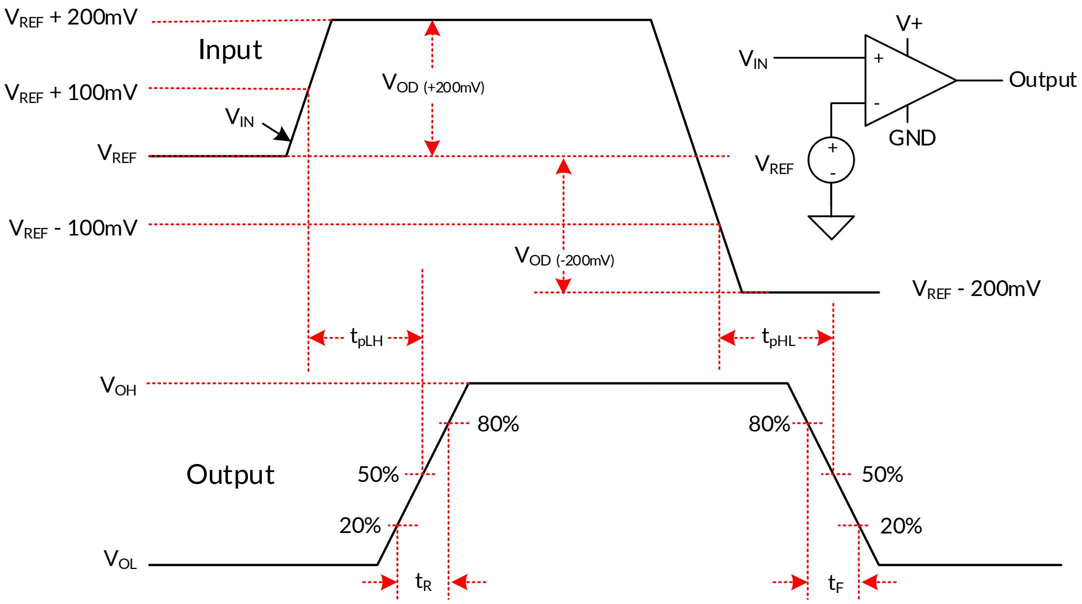


Figure 36. Comparator Timing Diagram

9.1.1.3 Overdrive Voltage

The overdrive voltage, V_{OD}, is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 200mV as shown in the Figure 36 example. The overdrive voltage can influence the propagation delay (tp). The smaller the overdrive voltage, the longer the propagation delay, particularly when <100mV. If the fastest speeds are desired, RUNIC recommends applying the highest amount of overdrive possible.

The risetime (t_r) and falltime (t_f) is the time from the 20% and 80% points of the output waveform.

9.1.2 Hysteresis

The basic comparator configuration can oscillate or produce a noisy 'chatter' output if the applied differential input voltage is near the comparator's offset voltage. This usually occurs when the input signal is moving very slowly across the switching threshold of the comparator.

This problem can be prevented by the addition of hysteresis or positive feedback.

The hysteresis transfer curve is shown in Figure 37. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and V_{IN-}. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

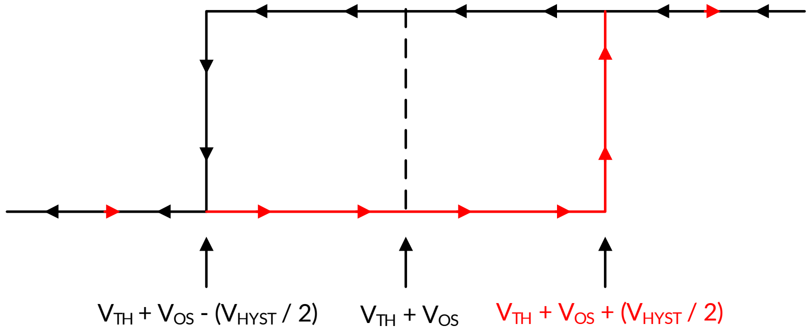


Figure 37. Hysteresis Transfer Curve

9.1.2.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V+), as shown in Figure 38.

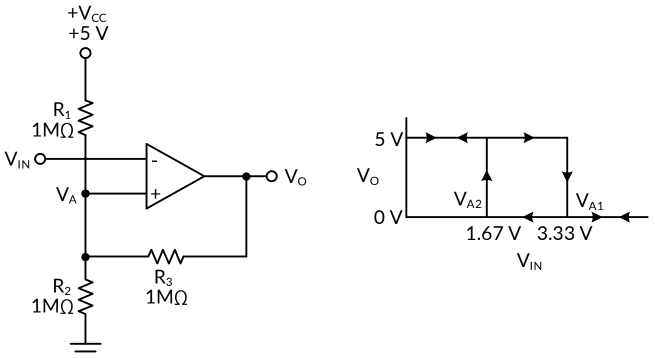


Figure 38. RS895X in an Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in Figure 38.

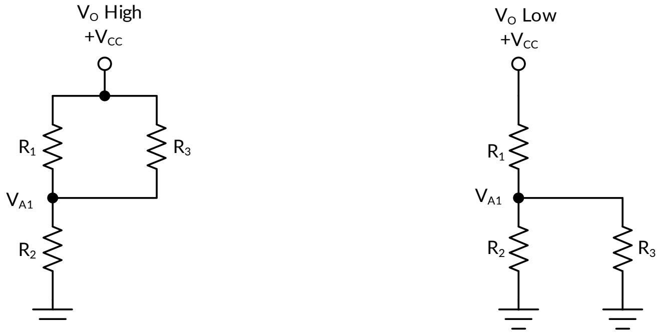


Figure 39. Inverting Configuration Resistor Equivalent Networks

When V_{IN} is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2, as shown in Figure 39.

Equation 1 below defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \tag{1}$$

When VIN is greater than VA, the output voltage is low. In this case, the three network resistors can be presented as R2 || R3 in series with R1, as shown in Equation 2.

Use Equation 2 to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \tag{2}$$

Equation 3 defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \tag{3}$$

9.1.2.2 Non-Inverting Comparator With Hysteresis

A noninverting comparator with hysteresis requires a two-resistor network and a voltage reference (V_{REF}) at the inverting input, as shown in Figure 40,

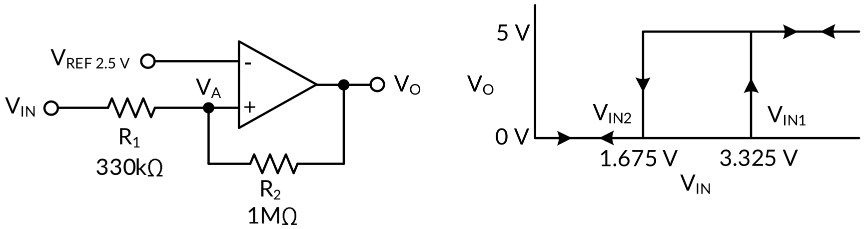


Figure 40. RS895X in a Non-Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in Figure 41.

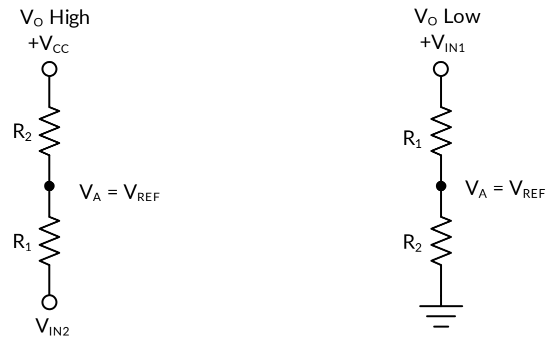


Figure 41. Non-Inverting Configuration Resistor Networks

When V_{IN} is less than V_{REF}, the output is low. For the output to switch from low to high, V_{IN} must rise above the V_{IN1} threshold. Use Equation 4 to calculate V_{IN1}.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \tag{4}$$

When V_{IN} is greater than V_{REF}, the output is high. For the comparator to switch back to a low state, V_{IN} must drop below V_{IN2}. Use Equation 5 to calculate V_{IN2}.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as shown in Equation 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

9.2 Typical Applications

9.2.1 Square-Wave Oscillator

Square-wave oscillator can be used as low cost timing reference or system supervisory clock source. A push-pull output (RS895X) is recommended for best symmetry.

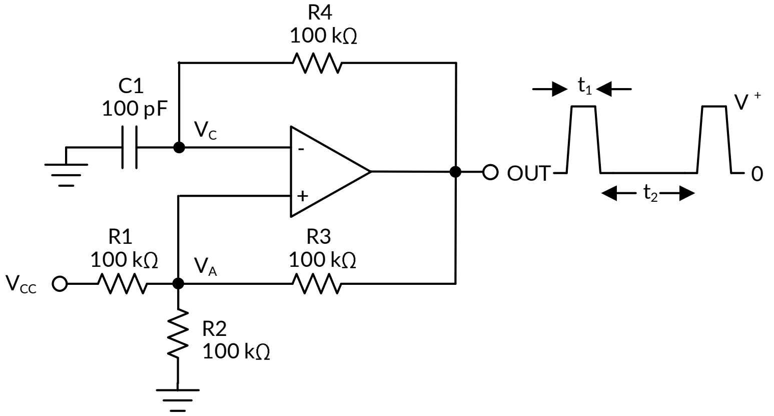


Figure 42. Square-Wave Oscillator

9.2.1.1 Design Requirements

The square-wave period is determined by the RC time constant of the capacitor C_1 and resistor R_4. The maximum frequency is limited by propagation delay of the device and the capacitance load at the output. The low input bias current allows a lower capacitor value and larger resistor value combination for a given oscillator frequency, which can help to reduce BOM cost and board space. R_4 must be over several kilo-ohms to minimize loading the output.

9.2.1.2 Detailed Design Procedure

The oscillation frequency is determined by the resistor and capacitor values. The following calculation provides details of the steps.

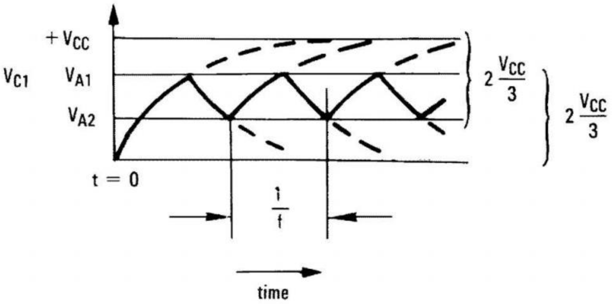


Figure 43. Square-Wave Oscillator Timing Thresholds

First consider the output of Figure 42 as high, which indicates the inverted input V_C is lower than the noninverting input (V_A). This causes the C_1 to be charged through R_4, and the voltage V_C increases until the inverting input is equal to the noninverting input. The value of V_A at the point is calculated by Equation 7.

$$V_{A1} = \frac{V_{CC} \times R_2}{R_2 + R_1 \, || \, R_3} \tag{7}$$

if $R_1 = R_2 = R_3$, then $V_{A1} = 2V_{CC}/3$

At this time the comparator output trips pulling down the output to the negative rail. The value of V_A at this point is calculated by Equation 8.

$$V_{A2} = \frac{V_{CC}\,(R_2 \, || \, R_3)}{R_1 + R_2 \, || \, R_3} \tag{8}$$

if $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$

The C_1 now discharges though the R_4, and the voltage V_{CC} decreases until the voltage reaches V_{A2}. At this point, the output switches back to the starting state. The oscillation period equals to the time duration from for C_1 from $2V_{CC}/3$ to $V_{CC}/3$ then back to $2V_{CC}/3$, which is given by $R_4C_1 \times \ln 2$ for each trip. Therefore, the total time duration is calculated as $2\,R_4C_1 \times \ln 2$.

The oscillation frequency can be obtained by Equation 9:

$$f = 1/\,(2\,R4 \times C1 \times \ln 2) \tag{9}$$

9.2.1.3 Application Curve

Figure 44 shows the simulated results of an oscillator using the following component values:

- $R_1 = R_2 = R_3 = R_4 = 100k\Omega$
- $C_1 = 100pF$, $C_L = 20pF$
- V+ = 5V, V– = GND
- C_{stray} (not shown) from V_A TO GND = 10pF

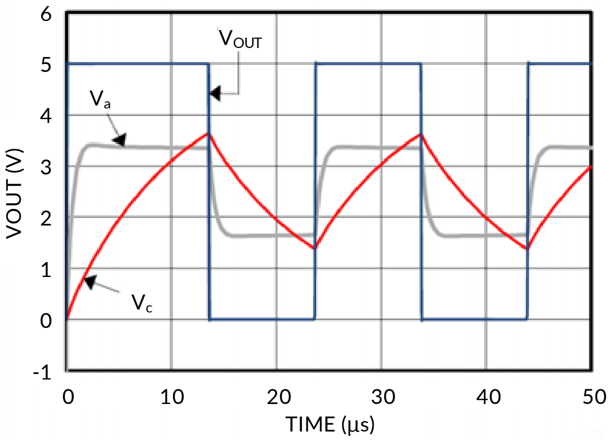


Figure 44. Square-Wave Oscillator Output Waveform

9.2.2 Adjustable Pulse Width Generator

Figure 45 is a variation on the Square-Wave Oscillator that allows adjusting the pulse widths.

R_4 and R_5 provide separate charge and discharge paths for the capacitor C depending on the output state.

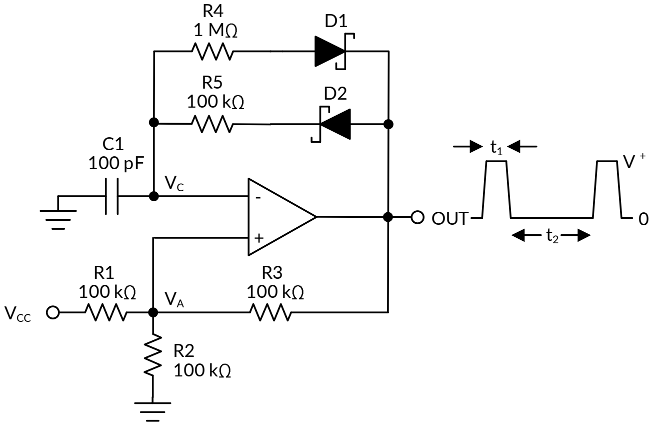


Figure 45. Adjustable Pulse Width Generator

The charge path is set through R_5 and D_2 when the output is high. Similarly, the discharge path for the capacitor is set by R_4 and D_1 when the output is low.

The pulse width t_1 is determined by the RC time constant of R_5 and C. Thus, the time t_2 between the pulses can be changed by varying R_4, and the pulse width can be altered by R_5. The frequency of the output can be changed by varying both R_4 and R_5. At low voltages, the effects of the diode forward drop (0.8V, or 0.15V for Shottky) must be taken into account by altering output high and low voltages in the calculations.

9.2.3 One-Shot Multivibrator

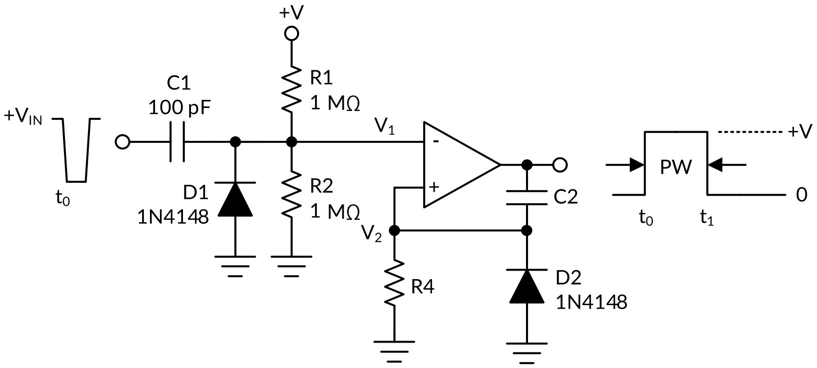


Figure 46. One-Shot Multivibrator

A monostable multivibrator has one stable state in which the output can remain indefinitely. The circuit can be triggered externally to another quasi-stable state. A monostable multivibrator can thus be used to generate a pulse of desired width.

The desired pulse width is set by adjusting the values of C_2 and R_4. The resistor divider of R_1 and R_2 can be used to determine the magnitude of the input trigger pulse. The output changes state when $V_1 < V_2$. Diode D_2 provides a rapid discharge path for capacitor C_2 to reset at the end of the pulse. The diode also prevents the non-inverting input from being driven below ground.

9.2.4 Bi-Stable Multivibrator

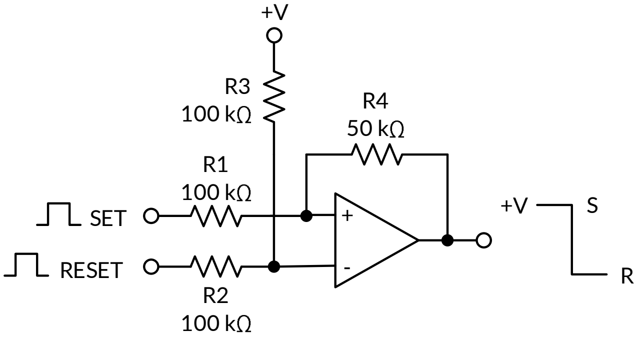


Figure 47. Bi-Stable Multivibrator

A bi-stable multivibrator has two stable states. The reference voltage is set up by the voltage divider of R_2 and R_3. A pulse applied to the SET terminal that sets the output of the comparator high. The resistor divider of R_1, R_4, and R_5 now clamps the non-inverting input to a voltage greater than the reference voltage. A pulse applied to RESET toggles the output low.

9.2.5 Zero Crossing Detector

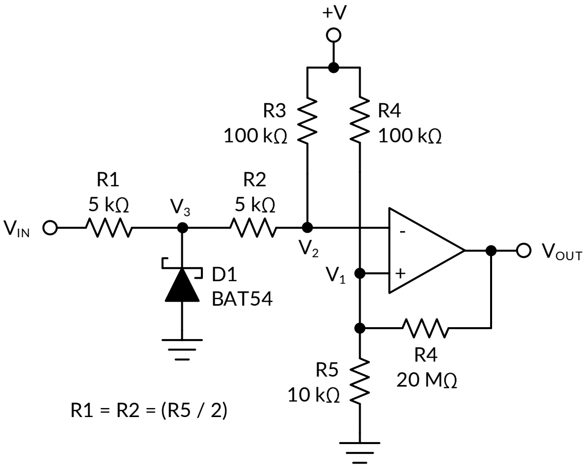


Figure 48. Zero Crossing Detector

A voltage divider of R_4 and R_5 establishes a reference voltage V_1 at the non-inverting input. By making the series resistance of R_1 and R_2 equal to R_5, the comparator switches when $V_{IN} = 0$. Diode D_1 makes sure that V_3 clamps near ground. The voltage divider of R_2 and R_3 then prevents V_2 from going below ground. A small amount of hysteresis is used to provide rapid output voltage transitions.

9.2.6 Pulse Slicer

A Pulse Slicer is a variation of the Zero Crossing Detector and is used to detect the zero crossings on an input signal with a varying baseline level. This circuit works best with symmetrical waveforms. The RC network of R_1 and C_1 establishes an mean reference voltage V_{REF}, which tracks the mean amplitude of the V_{IN} signal. The noninverting input is directly connected to V_{REF} through R_2. R_2 and R_3 are used to produce hysteresis to keep transitions free of spurious toggles. The time constant is a tradeoff between long-term symmetry and response time to changes in amplitude.

When the waveform is data, RUNIC recommends that the data be encoded in NRZ (Non-Return to Zero) format to maintain proper average baseline. Asymmetrical inputs can suffer from timing distortions caused by the changing V_{REF} average voltage.

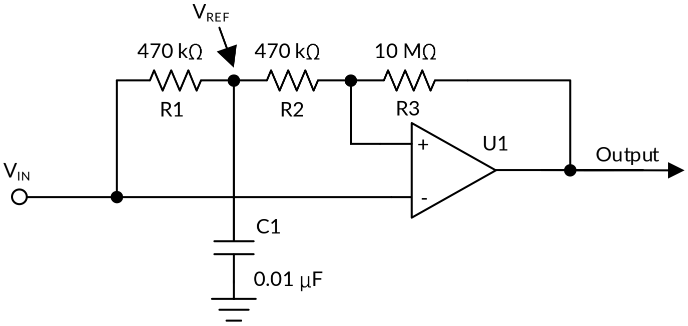


Figure 49. Pulse Slicer Using RS895X

For this design, follow these design requirements:

- The RC constant value (R_2 and C_1) must support the targeted data rate to maintain a valid tripping threshold.
- The hysteresis introduced with R_2 and R_3 helps to avoid spurious output toggles.

Figure 50 shows the results of a 9600 baud data signal riding on a varying baseline.

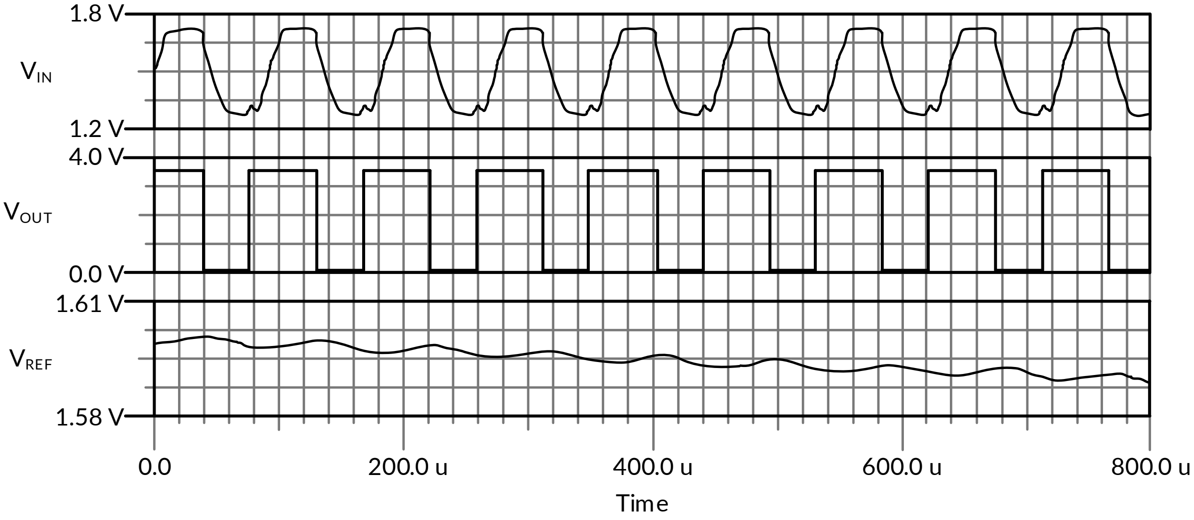


Figure 50. Pulse Slicer Waveforms

9.3 Power Supply Recommendations

Due to the fast output edges, proper supply bypassing is critical to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at each device with a low ESR 0.1µF ceramic bypass capacitor directly between V_{CC} pin and ground pins. Narrow, peak currents can be drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device can be powered from either "split" supplies (V+, V- & GND), or a "single" supply (V+ and GND), with GND applied to the V- pin.

Input signals must stay within the specified input range (between V+ and V-) for either type.

Note that on "split" supplies, the output now swings "low" (V_{OL}) to V- potential and not GND.

10 LAYOUT

10.1 Layout Guidelines

For accurate comparator applications a stable power supply with minimized noise and glitches. Output rise and fall times are in the tens of nanoseconds, and must be treated as high speed logic devices. The bypass capacitor must be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the V_{CC} and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a V_{CC} or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (<100 ohms) resistor can also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations must be used when routing long distances.

10.2 Layout Example

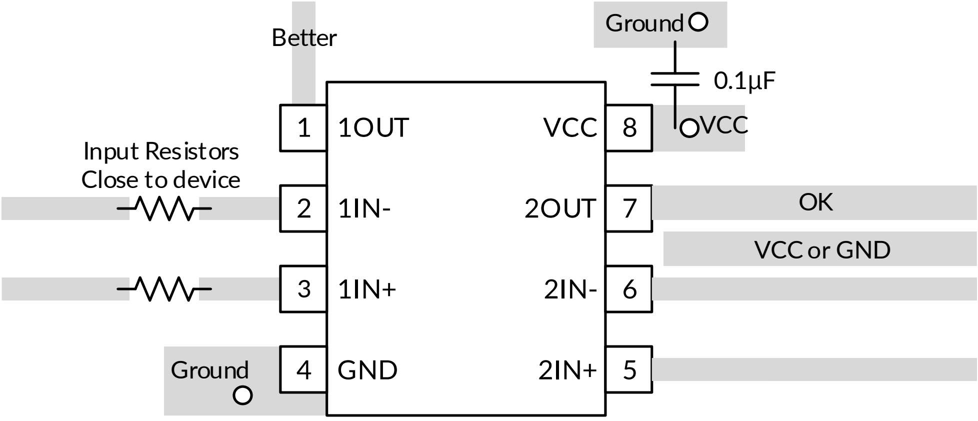
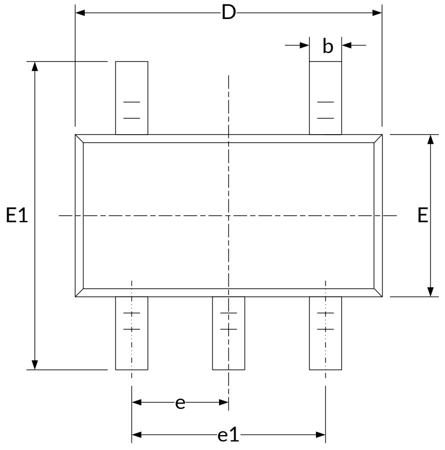
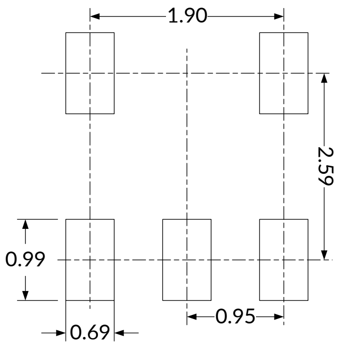


Figure 51. Dual Layout Example

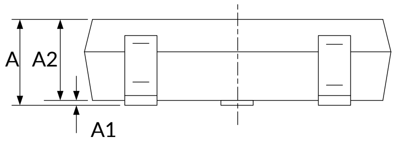
11 PACKAGE OUTLINE DIMENSIONS

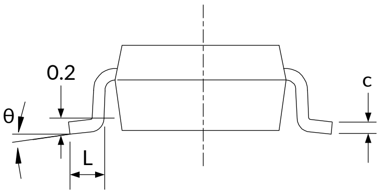
SOT23-5 (3)





RECOMMENDED LAND PATTERN (Unit: mm)



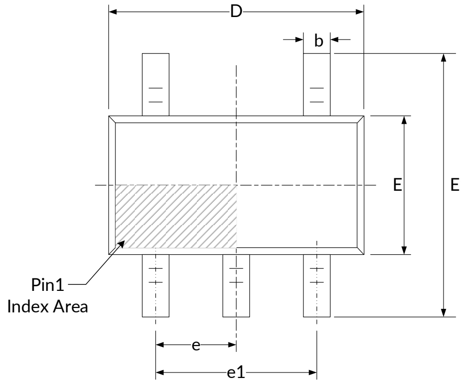


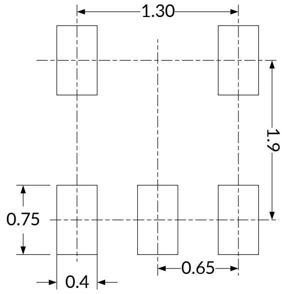
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D (1)	2.820	3.020	0.111	0.119
E (1)	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC) (2)		0.037(BSC) (2)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

NOTE:

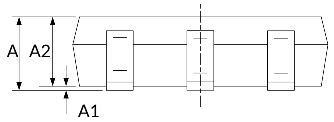
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

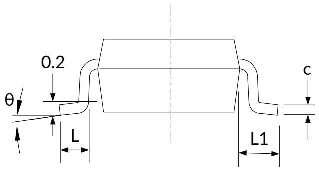
SC70-5 (3)





RECOMMENDED LAND PATTERN (Unit: mm)



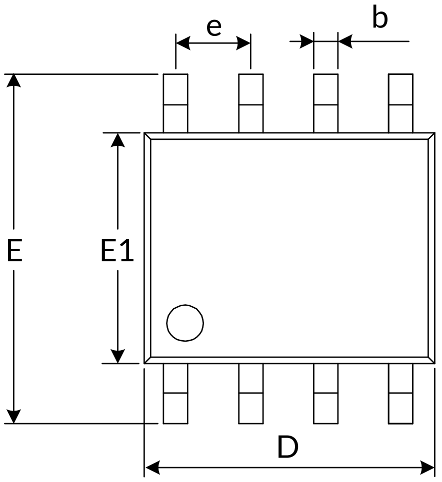


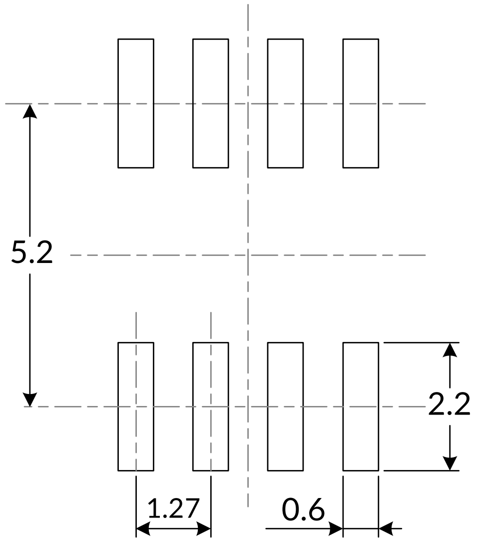
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.150	0.003	0.006
D (1)	2.000	2.200	0.079	0.087
E (1)	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650(BSC) (2)		0.026(BSC) (2)	
e1	1.300(BSC) (2)		0.051(BSC) (2)	
L	0.260	0.460	0.010	0.018
L1	0.525		0.021	
θ	0°	8°	0°	8°

NOTE:

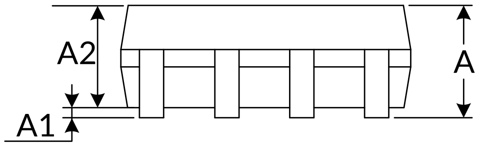
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

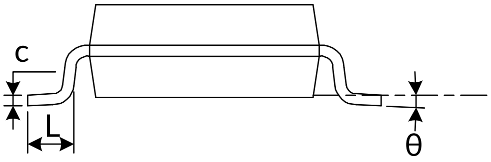
SOP8 (3)





RECOMMENDED LAND PATTERN (Unit: mm)



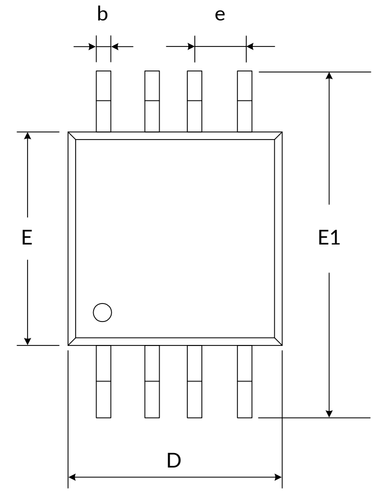


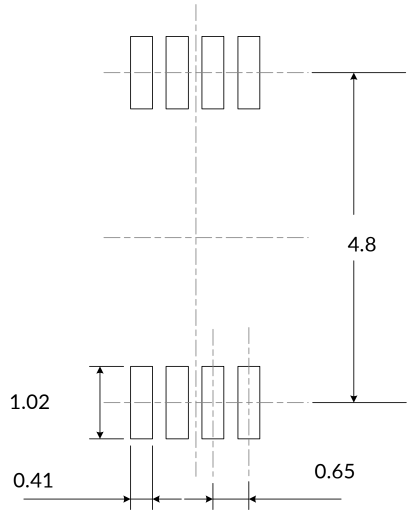
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D (1)	4.800	5.000	0.189	0.197
e	1.270(BSC) (2)		0.050(BSC) (2)	
E	5.800	6.200	0.228	0.244
E1 (1)	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTE:

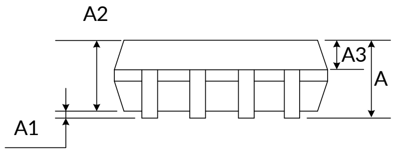
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

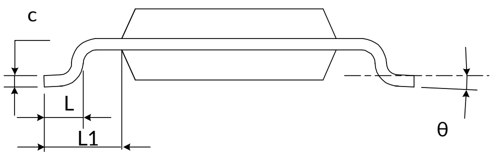
MSOP8 (4)





RECOMMENDED LAND PATTERN (Unit: mm)



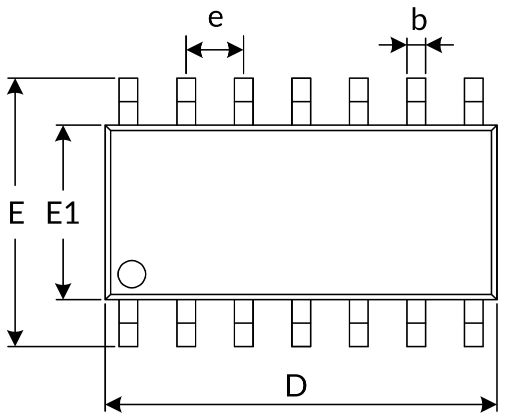


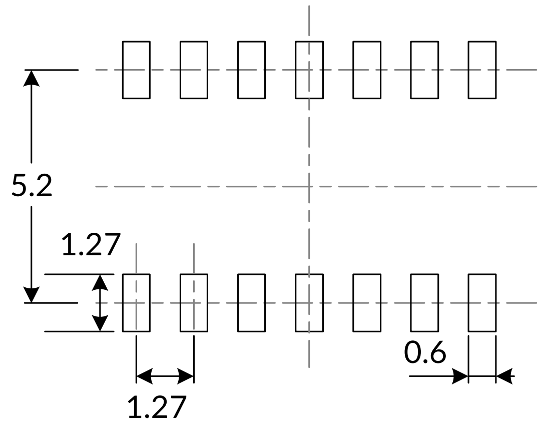
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.100		0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
A3	0.300	0.400	0.012	0.016
b	0.280	0.360	0.011	0.014
c	0.150	0.190	0.006	0.007
D (1)	2.900	3.100	0.114	0.122
e	0.650(BSC) (2)		0.026(BSC) (2)	
E (1)	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.200
L	0.400	0.700	0.016	0.027
L1	0.950(REF) (3)		0.037(REF) (3)	
θ	0°	8°	0°	8°

NOTE:

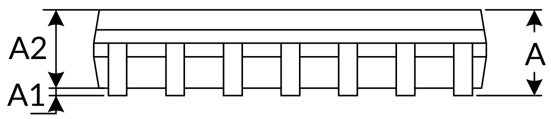
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. REF is the abbreviation for Reference.
4. This drawing is subject to change without notice.

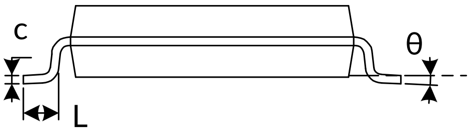
SOP14 (3)





RECOMMENDED LAND PATTERN (Unit: mm)

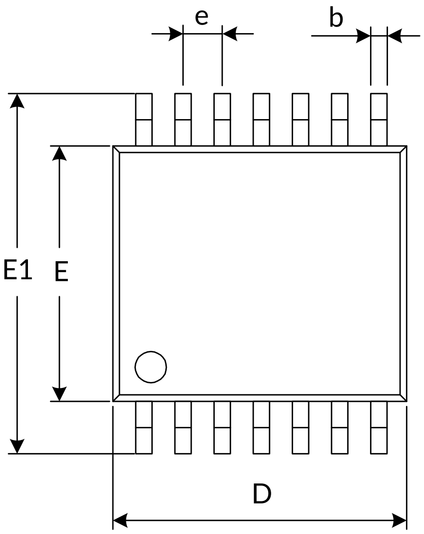


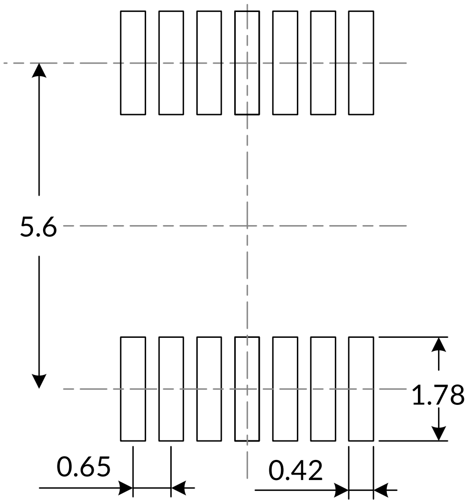


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D (1)	8.450	8.850	0.333	0.348
e	1.270(BSC) (2)		0.050(BSC) (2)	
E	5.800	6.200	0.228	0.244
E1 (1)	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

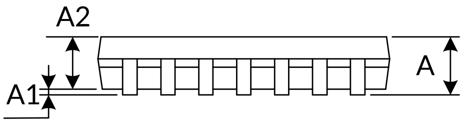
NOTE:
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

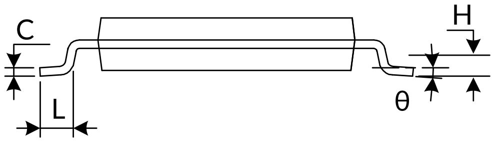
TSSOP14 (3)





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D (1)	4.860	5.100	0.191	0.201
E (1)	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650(BSC) (2)		0.026(BSC) (2)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

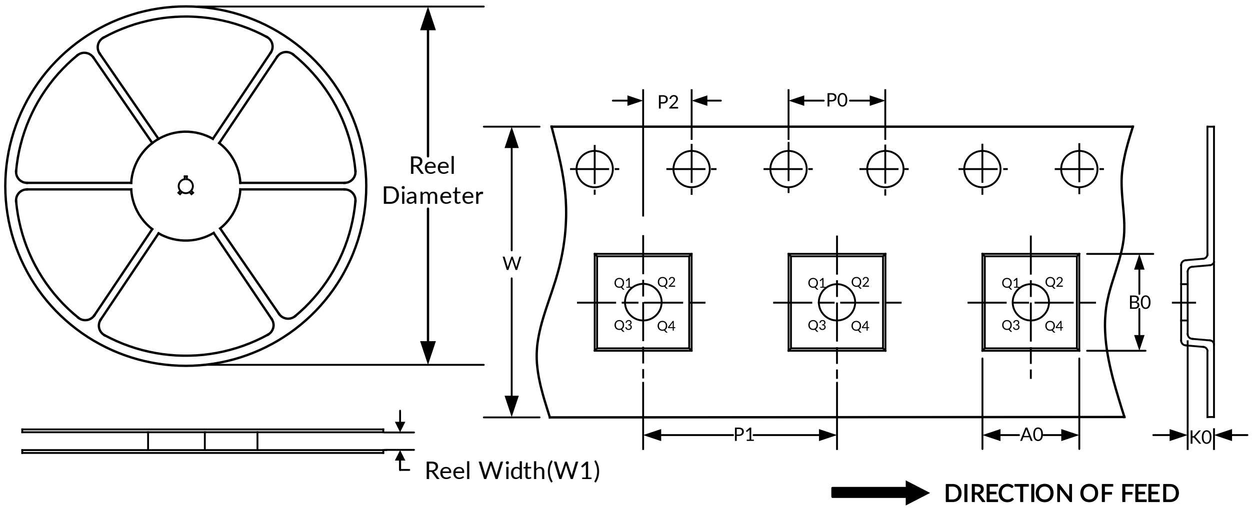
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

12 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT23-5	7”	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
SC70-5	7”	9.5	2.25	2.55	1.20	4.0	4.0	2.0	8.0	Q3
SOP8	13”	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
MSOP8	13”	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1
SOP14	13”	16.4	6.60	9.30	2.10	4.0	8.0	2.0	16.0	Q1
TSSOP14	13”	12.4	6.95	5.60	1.20	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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