RS894X Precision Comparator Family

1 FEATURES

- **1.8V to 5.5V Supply Range**
- **Precision Input Offset voltage 500μV**
- **Power-on Reset (POR) for Known Start-Up**
- **Rail-to-Rail Input with Fault-Tolerance**
- **100ns Typical Propagation Delay**
- **Low Quiescent Current 30μA per Channel**
- **Low Input Bias Current 12pA**
- **Open-Drain Output Option**
- **Full -40°C to +125°C Temperature Range**

2 APPLICATIONS

- **Appliances**
- **Building Automation**
- **Factory Automation & Control**
- **Motor Drives**
- **Infotainment & Cluster**

3 DESCRIPTIONS

The RS894X is a family of single, dual and quad channel comparators. The family offers low input offset voltage, fault-tolerant inputs and an excellent speed-to-power combination. The family has a propagation delay of 100ns with a quiescent supply current of only 30μA per channel.

The family also includes a Power-on Reset (POR) feature that makes sure the output is in a known state until the minimum supply voltage has been reached. This prevents output transients during system power-up and power-down.

These comparators also feature fault-tolerant inputs that can go up to 6V without damage and with no output phase inversion. This family of comparators is designed for precision voltage monitoring in harsh, noisy environments.

The RS894X have an open-drain output that can be pulled-up below or beyond the supply voltage. These devices are designed for low voltage logic translators.

The family is specified for the Industrial temperature range of -40°C to +125°C and are available in a standard leaded and leadless packages.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS8940	SOT23-5	1.60mm×2.92mm
RS8942	SOP8	4.90mm×3.90mm
	MSOP8	3.00mm×3.00mm
RS8944	SOP14	8.65mm×3.90mm
	TSSOP14	5.00mm×4.40mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2025/08/07	Preliminary version completed
A.0.1	2025/10/22	1. Update ESD Ratings 2. Update DETAILED DESCRIPTION
A.1	2026/04/17	Initial version completed

5 PACKAGE/ORDERING INFORMATION (1)

Orderable Device	Package Type	Pin	Channel	Op Temp(°C)	Device Marking (2)	MSL (3)	Package Qty
RS8940XF	SOT23-5	5	1	-40°C ~125°C	8940	MSL3	Tape and Reel, 3000
RS8942XK	SOP8	8	2	-40°C ~125°C	RS8942	MSL3	Tape and Reel, 4000
RS8942XM	MSOP8	8	2	-40°C ~125°C	RS8942	MSL3	Tape and Reel, 4000
RS8944XP	SOP14	14	4	-40°C ~125°C	RS8944	MSL3	Tape and Reel, 4000
RS8944XQ	TSSOP14	14	4	-40°C ~125°C	RS8944	MSL3	Tape and Reel, 4000

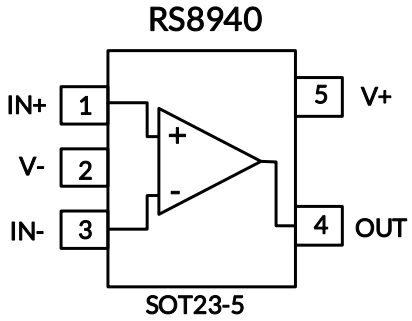
NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

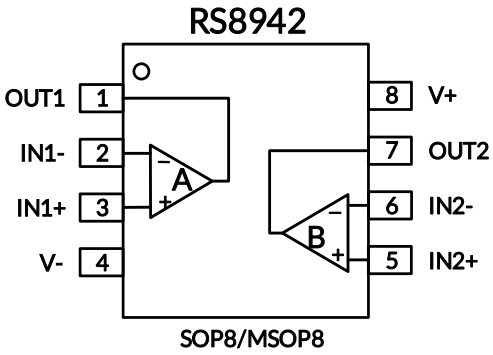
6 PIN CONFIGURATION AND FUNCTIONS



PIN DESCRIPTION

NAME	PIN	I/O (1)	DESCRIPTION
	RS8940		
	SOT23-5		
IN+	1	I	Non-Inverting (Positive) Input
IN-	3	I	Inverting (Negative) Input
OUT	4	O	Output
V+	5	-	Positive Power Supply
V-	2	-	Negative Power Supply

(1) I=Input, O=Output.

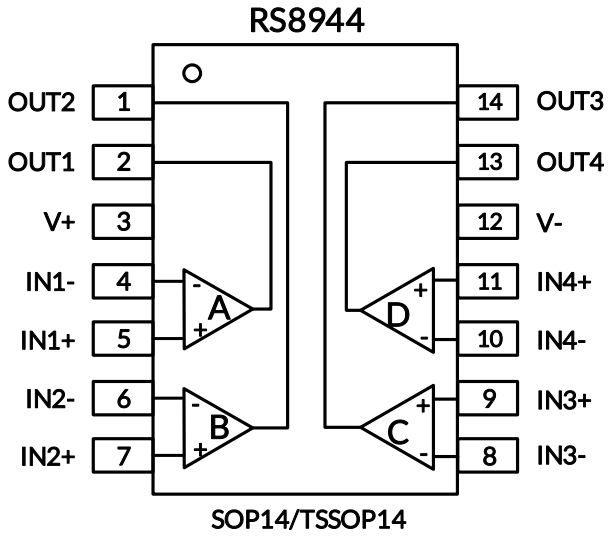


PIN DESCRIPTION

NAME	PIN	I/O (1)	DESCRIPTION
	SOP8/MSOP8		
OUT1	1	O	Output pin of the comparator 1
IN1-	2	I	Inverting input pin of comparator 1
IN1+	3	I	Noninverting input pin of comparator 1
V-	4	-	Negative (low) supply
IN2+	5	I	Noninverting input pin of comparator 2
IN2-	6	I	Inverting input pin of comparator 2
OUT2	7	O	Output pin of the comparator 2
V+	8	-	Positive supply

(1) I=Input, O=Output.

PIN CONFIGURATION AND FUNCTIONS



PIN DESCRIPTION

NAME	PIN	I/O (1)	DESCRIPTION
	SOP14/TSSOP14		
OUT2	1	O	Output pin of the comparator 2
OUT1	2	O	Output pin of the comparator 1
V+	3	-	Positive supply
IN1-	4	I	Negative input pin of the comparator 1
IN1+	5	I	Positive input pin of the comparator 1
IN2-	6	I	Negative input pin of the comparator 2
IN2+	7	I	Positive input pin of the comparator 2
IN3-	8	I	Negative input pin of the comparator 3
IN3+	9	I	Positive input pin of the comparator 3
IN4-	10	I	Negative input pin of the comparator 4
IN4+	11	I	Positive input pin of the comparator 4
V-	12	-	Negative supply
OUT4	13	O	Output pin of the comparator 4
OUT3	14	O	Output pin of the comparator 3

(1) I=Input, O=Output.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Voltage	Supply, V_S=(V+) - (V-)		-0.3	6	V
	Input pins (IN+, IN-) from V- (2)		-0.3	6	
	Output (OUT) from V– (3)		-0.3	6	
Current	Current into Input pins (IN+, IN–)		-10	10	mA
	Output short-circuit duration (4)			10	s
θ_{JA}	Package thermal impedance (5)	SOT23-5		230	°C/W
		SOP8		110	
		MSOP8		165	
		SOP14		105	
		TSSOP14		90	
Temperature	Junction, T_J (6)			150	°C
	Storage, T_{stg}		-65	150	

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to (V–). Input signals that can swing more than 0.3V beyond the supply rails must be current-limited to 10mA or less. Additionally, Inputs (IN+, IN–) can be greater than V+ and OUT as long as the input is within the –0.3V to 6V range.
(3) Output (OUT) for open drain can be greater than V+ and inputs (IN+, IN–) as long as the pins are within the –0.3V to 6V range.
(4) Short-circuit to V- or V+. Short circuits from outputs can cause excessive heating and eventual destruction.
(5) The package thermal impedance is calculated in accordance with JESD-51.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), per EIA/JESD22-a114	±2000	V
		Charged-Device Model (CDM), per ANSI/ESDA/JEDEC JS-002-2022	±1000	

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage: V_S= (V+) - (V-)	1.8	5.5	V
Input voltage range (IN+, IN–) from (V–)	-0.2	5.7	V
Ambient temperature, T_A	-40	125	°C

7.4 Electrical Characteristics

For V_S (Total Supply Voltage) = (V+) – (V–) = 5V, V_{CM} = (V–) at T_A = 25°C, Full =-40°C to +125°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	T_A	RS894X			
				MIN(2)	TYP(3)	MAX(2)	UNIT
OFFSET VOLTAGE							
V_{OS}	Input Offset Voltage	V_S = 1.8V and 5V	25°C	-2	±0.5	2	mV
			Full	-3		3	
dV_{IO}/dT	Input Offset Voltage Drift	V_S = 1.8V and 5V	Full		±2		µV/°C
POWER SUPPLY							
I_Q	Quiescent Current per Channel	V_S = 1.8V and 5V, No Load, Output Low	25°C		30	40	µA
			Full			50	
PSRR	Power-Supply Rejection Ratio	V_S = 1.8V to 5V	25°C	75	90		dB
			Full	70			
INPUT BIAS CURRENT							
I_B	Input Bias Current	V_{CM} = V_S/2	25°C		12		pA
I_{OS}	Input Offset Current	V_{CM} = V_S/2	25°C		12		pA
INPUT VOLTAGE RANGE							
$V_{CM-Range}$	Common-Mode Voltage Rang	V_S = 1.8V and 5V	Full	(V-)-0.2		(V+)+0.2	V
CMRR	Common-Mode Rejection Ratio	V_S = 5V, (V–) – 0.2V < V_{CM} < (V+) + 0.2V	Full	60	70		dB
CMRR	Common-Mode Rejection Ratio	V_S = 1.8V, (V–) – 0.2V < V_{CM} < (V+) + 0.2V	Full	50	60		dB
OUTPUT							
V_{OL}	Voltage Swing from (V–)	I_{SINK} = 4mA	25°C		70	110	mV
			Full			150	
I_{LKG}	Open-Drain Output Leakage Current	V_{PULLUP} = (V+)	25°C		100		pA
I_{SC}	Short-Circuit Current	V_S = 5V, Sinking	25°C	80	100		mA
T_{PD-LH}	Propagation Delay Time, Low-to-High	V_{ID} = 100mV; R_P = 2.5kΩ, C_L=15pF, Delay from mid-point of input to mid-point of output	25°C		150		ns
T_{PD-HL}	Propagation Delay Time, High-to-Low	V_{ID} = -100mV; R_P = 2.5kΩ Delay from mid-point of input to mid-point of output	25°C		100		ns
T_{FALL}	5V Output Fall Time, 50% to 50%	V_{ID} = 1V	25°C		3		ns
POWER ON TIME							
P_{ON}	Power On Time	V_S = 1.8V and 5V, V_{CM} = (V–), V_{ID} = –0.1V, Delay from V_S/2 to V_{OUT}/2, R_P = 2.5kΩ (C_L=100pF)	25°C		20		µs

NOTE:

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

7.5 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

T_A = 25°C, V_S = 5V, R_{PULLUP} = 2.5kΩ, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

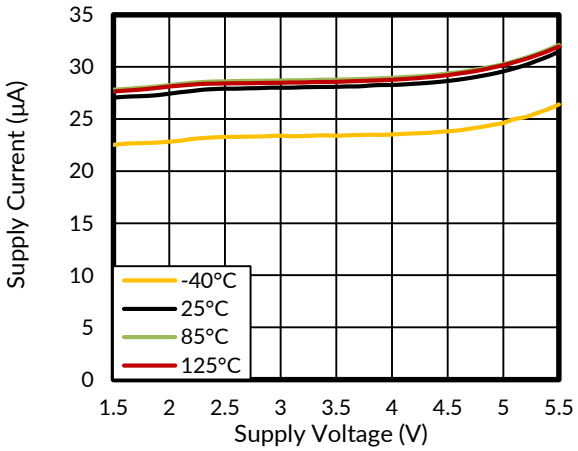


Figure 1. Supply Current vs Supply Voltage

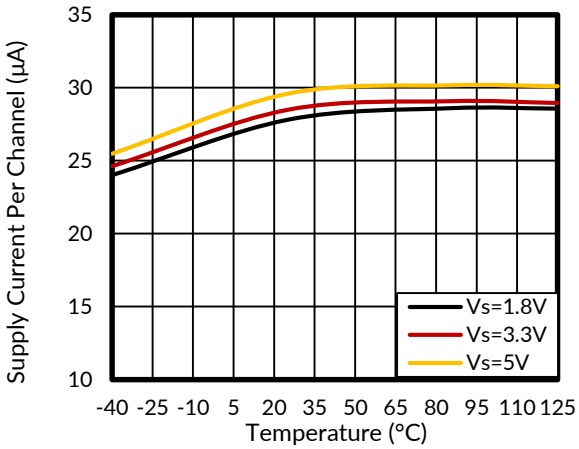


Figure 2. Supply Current vs Temperature

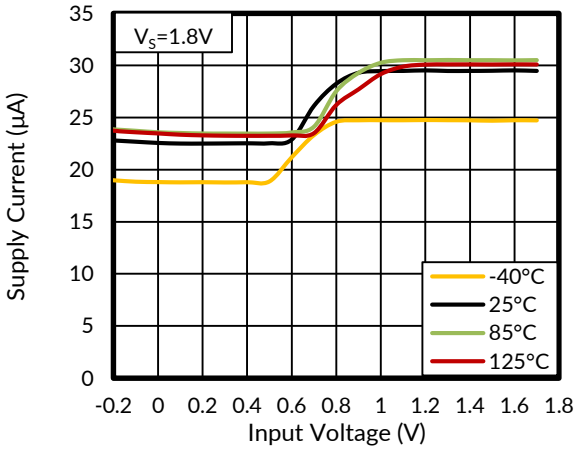


Figure 3. Supply Current vs Input Voltage

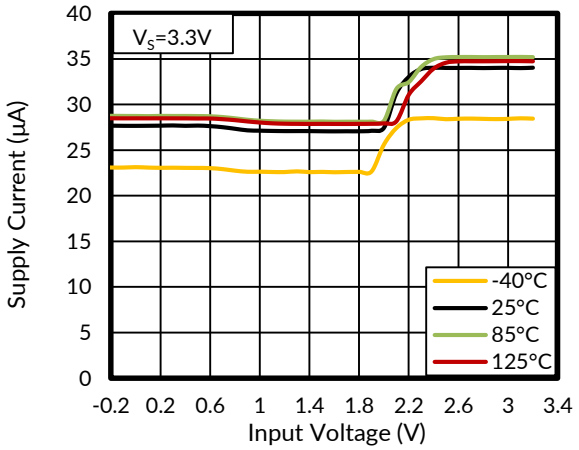


Figure 4. Supply Current vs Input Voltage

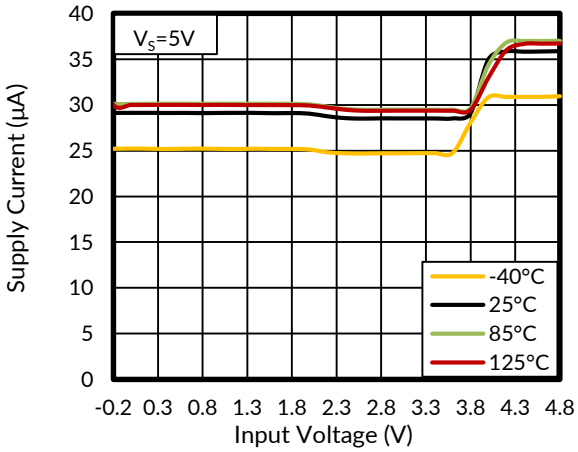


Figure 5. Supply Current vs Input Voltage

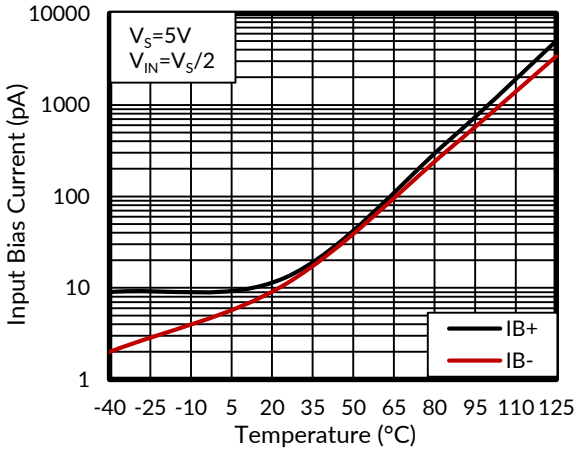


Figure 6. Input Bias Current vs Temperature

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

T_A = 25°C, V_S = 5V, R_{PULLUP} = 2.5kΩ, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

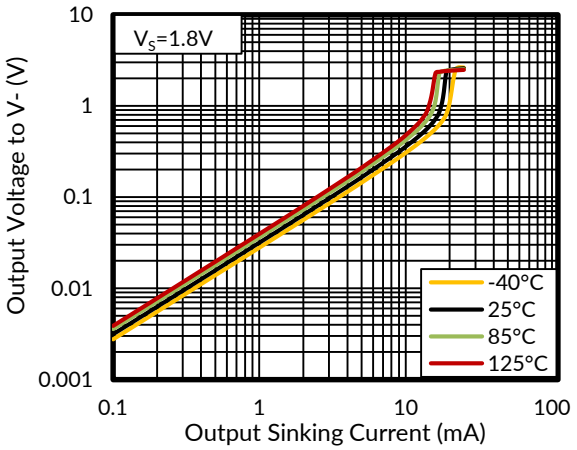


Figure 7. Output Voltage vs Output Sinking Current

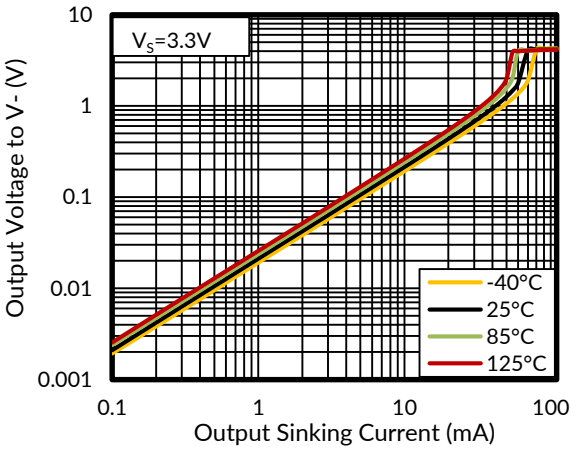


Figure 8. Output Voltage vs Output Sinking Current

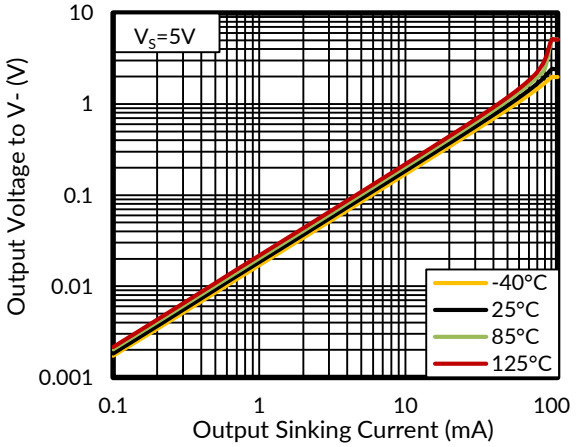


Figure 9. Output Voltage vs Output Sinking Current

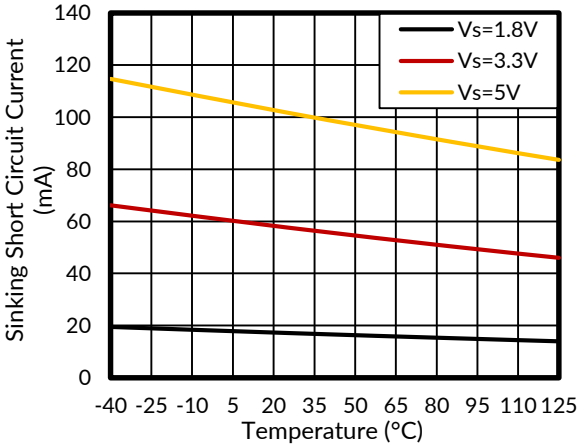


Figure 10. Sinking Short Circuit Current vs Temperature

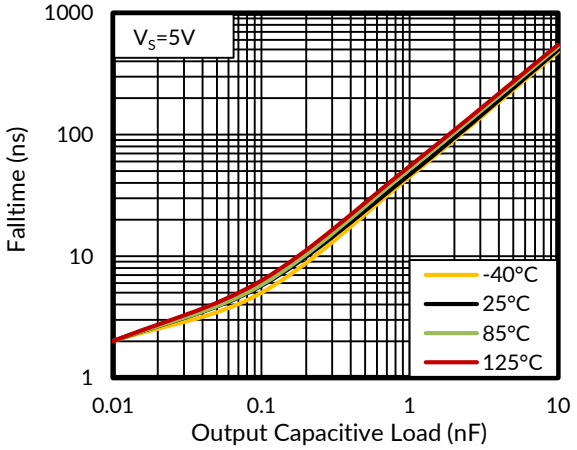


Figure 11. Falltime vs Capacitive Load

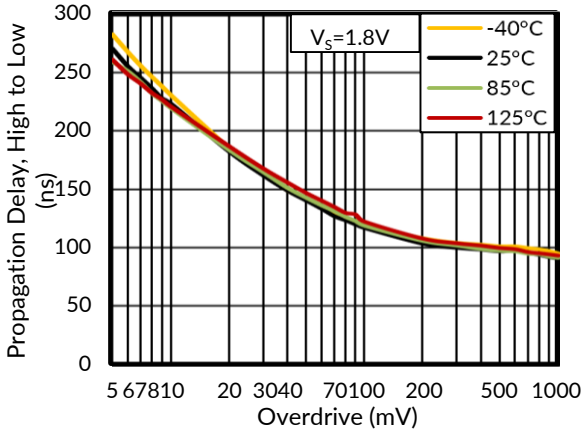


Figure 12. High to Low Propagation Delay vs Input Overdrive Voltage

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

T_A = 25°C, V_S = 5V, R_{PULLUP} = 2.5kΩ, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

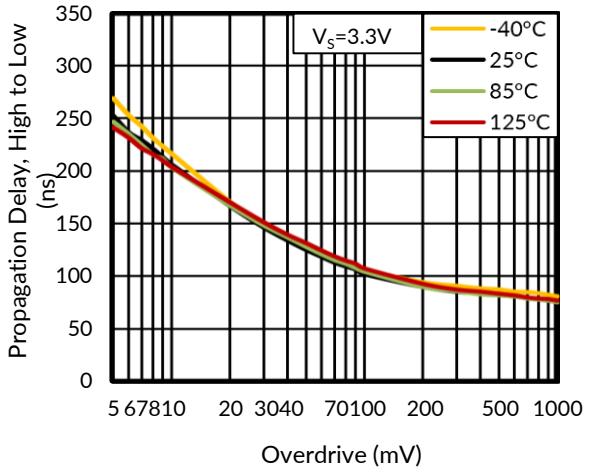


Figure 13. High to Low Propagation Delay vs Input Overdrive Voltage

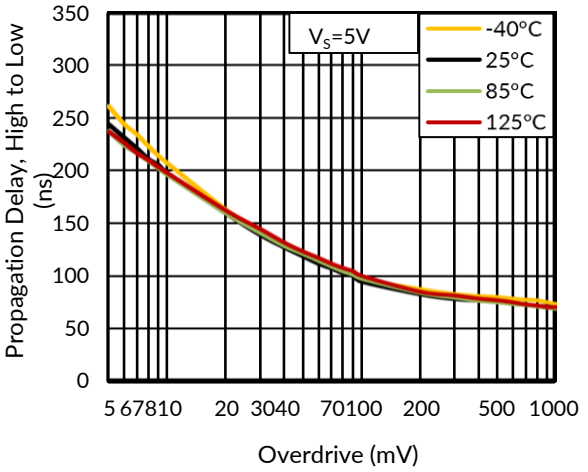


Figure 14. High to Low Propagation Delay vs Input Overdrive Voltage

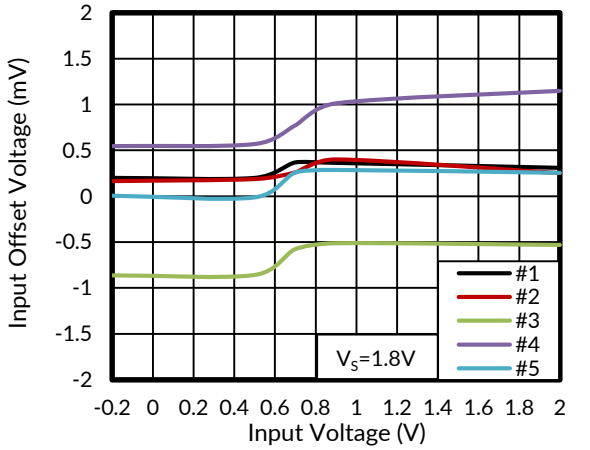


Figure 15. Offset Voltage vs Input Voltage at -40°C

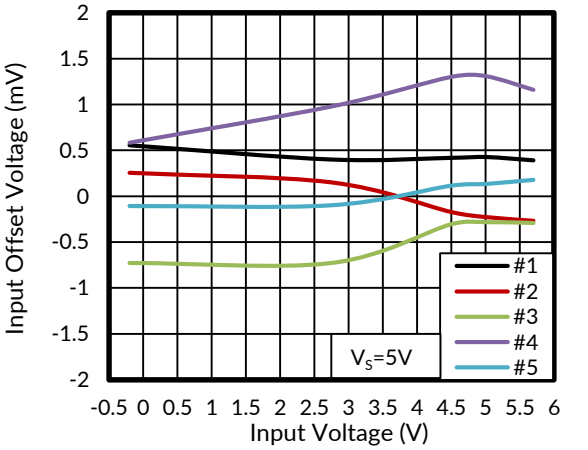


Figure 16. Offset Voltage vs Input Voltage at -40°C

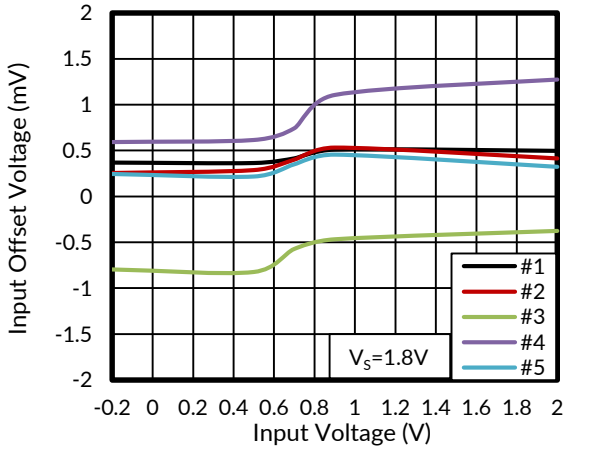


Figure 17. Offset Voltage vs Input Voltage at 25°C

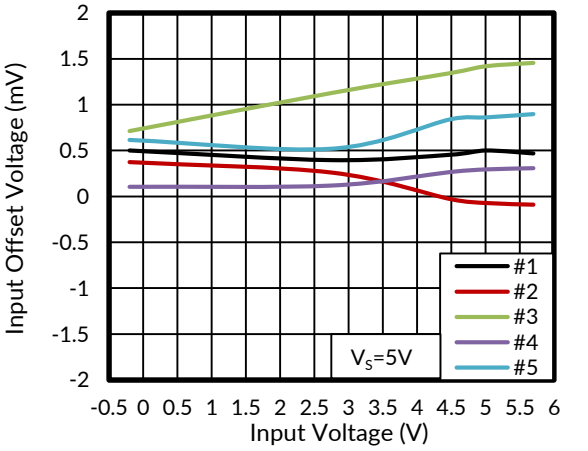


Figure 18. Offset Voltage vs Input Voltage at 25°C

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

T_A = 25°C, V_S = 5V, R_{PULLUP} = 2.5kΩ, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

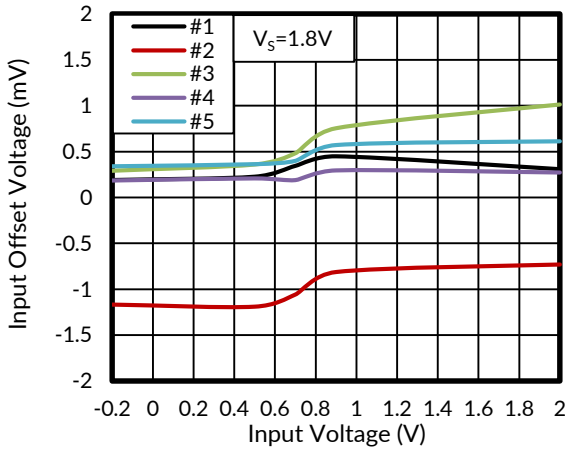


Figure 19. Offset Voltage vs Input Voltage at 125°C

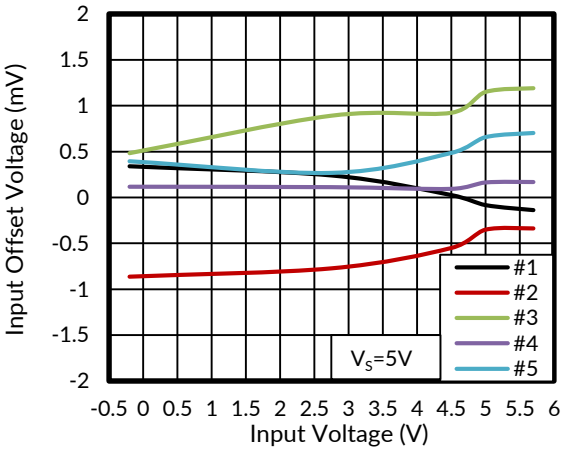


Figure 20. Offset Voltage vs Input Voltage at 125°C

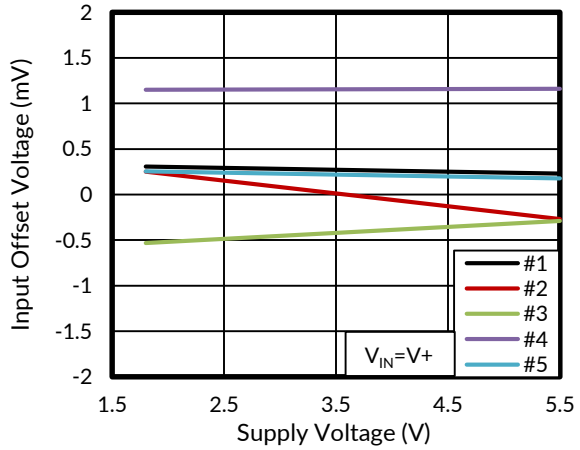


Figure 21. Input Offset Voltage vs Supply Voltage at -40°C

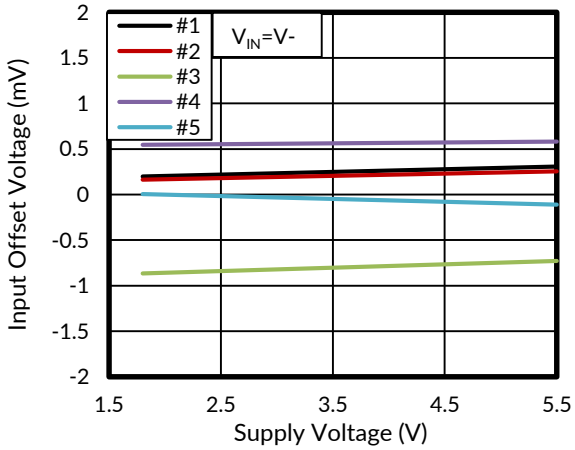


Figure 22. Input Offset Voltage vs Supply Voltage at -40°C

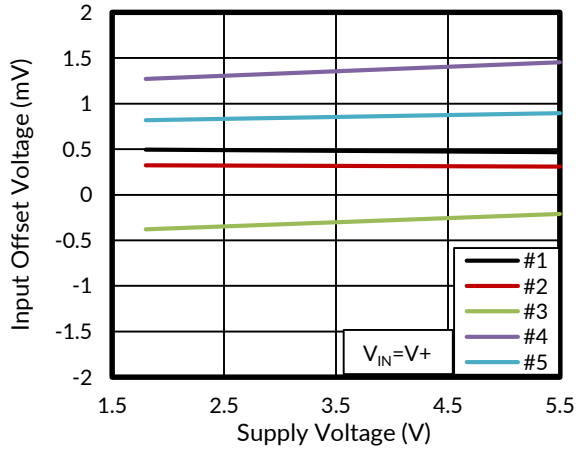


Figure 23. Input Offset Voltage vs Supply Voltage at 25°C

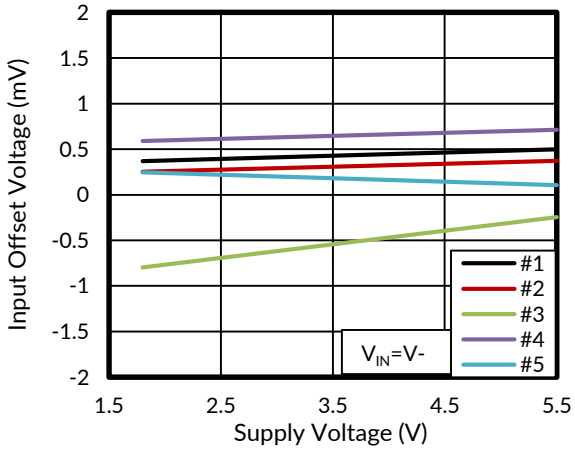


Figure 24. Input Offset Voltage vs Supply Voltage at 25°C

Typical Characteristics

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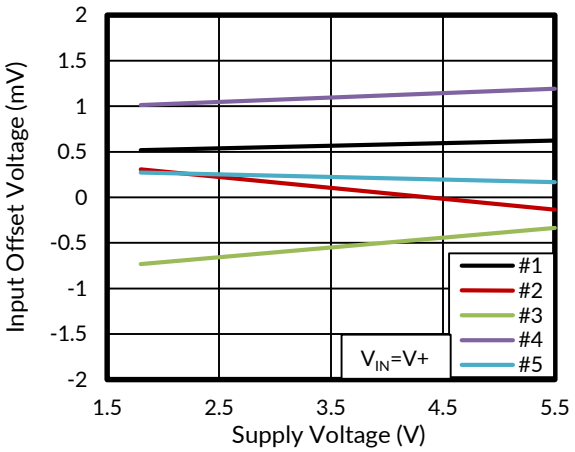


Figure 25. Input Offset Voltage vs Supply Voltage at 125°C

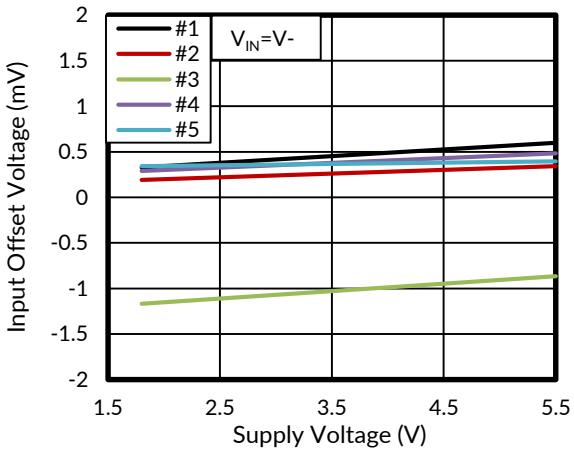


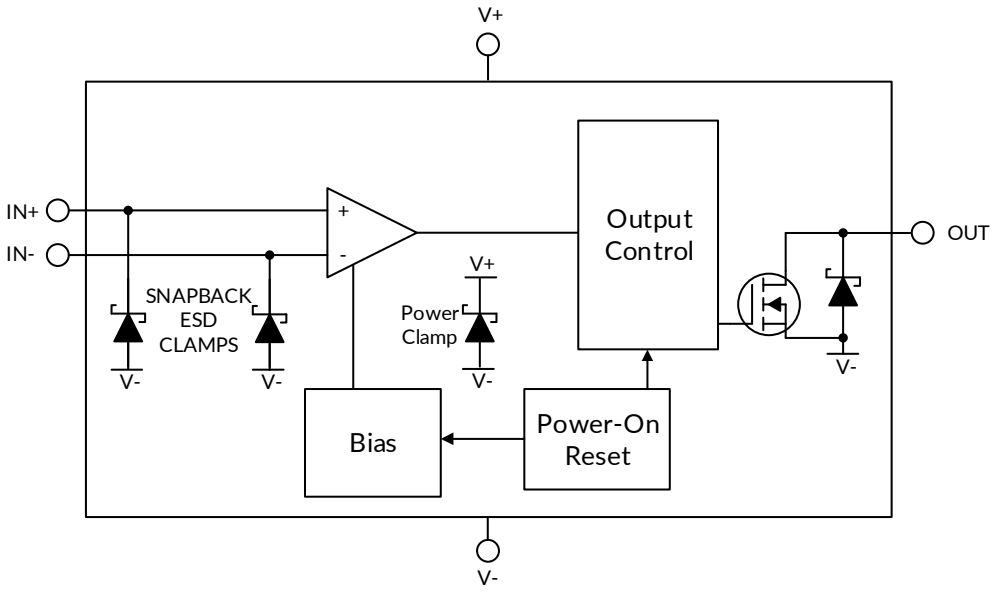
Figure 26. Input Offset Voltage vs Supply Voltage at 125°C

8 DETAILED DESCRIPTION

8.1 Overview

The RS894X devices are micro-power comparators with open-drain outputs and low input offset voltage. Operating down to 1.8V while consuming only 30μA per channel, the RS894X is designed for portable, automotive and industrial applications. An internal power-on reset circuit makes sure that the output remains in a known state during power-up and power-down while fail-safe inputs can tolerate input transients without damage or false outputs.

8.2 Functional Block Diagram



8.3 Feature Description

The RS894X devices are micro-power comparators that have low input offset voltages and are capable of operating at low voltages. The RS894X family feature a rail-to-rail input stage capable of operating up to 200mV beyond the power supply rails. The comparators also feature open-drain output stage and Power-on Reset for known start-up conditions.

8.4 Device Functional Modes

8.4.1 Outputs

8.4.1.1 RS8942 and RS8944 Open Drain Output

The RS894X features an open-drain (also commonly called open collector) sinking-only output stage enabling the output logic levels to be pulled up to an external voltage from 0V up to 5.5V, independent of the comparator supply voltage (V_S). The open-drain output also allows logical OR'ing of multiple open drain outputs and logic level translation. RUNIC recommends setting the pull-up resistor current to between 100μA and 1mA. Lower pull-up resistor values help increase the rising edge risetime, but at the expense of increasing V_{OL} and higher power dissipation. The risetime is dependant on the time constant of the total pull-up resistance and total load capacitance. Large value pull-up resistors (>1MΩ) creates an exponential rising edge due to the RC time constant and increases the risetime.

Unused open drain outputs must be left floating, or can be tied to the V- pin if floating pins are not allowed. While an individual output can typically sink up to 100mA, the total combined current for all channels must be less than 200mA.

8.4.2 Power-On Reset (POR)

The RS894X has an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply (Vs) is ramping up or down, the POR circuitry is activated for up to 20µs after the minimum supply voltage threshold of 1.5V is crossed, or immediately when the supply voltage drops below 1.5V. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input (V_{ID}).

The POR circuit keeps the output high impedance (HI-Z) during the POR period (t_{on}).

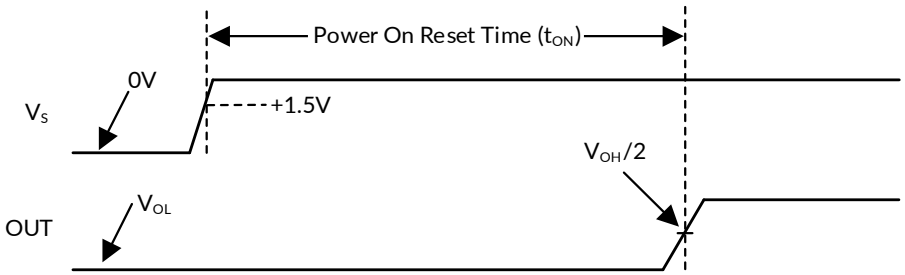


Figure 27. Power-On Reset Timing Diagram

Note that an open collector output voltage rises with the pull-up voltage during the POR period.

8.4.3 Inputs

8.4.3.1 Rail to Rail Input

The RS894X input voltage range extends from 200mV below V- to 200mV above V+. The differential input voltage (V_{ID}) can be any voltage within these limits. No phase-inversion of the comparator output occurs when the input pins exceed V+ or V-.

8.4.3.2 Fault Tolerant Inputs

The RS894X inputs are fault tolerant up to 5.5V independent of V_S. Fault tolerant is defined as maintaining the same high input impedance when V_S is unpowered or within the recommended operating ranges.

The fault tolerant inputs can be any value between 0V and 5.5V, even while V_S is zero or ramping up or down. This feature avoids power sequencing issues as long as the input voltage range and supply voltage are within the specified ranges. This is possible since the inputs are not clamped to V+ and the input current maintains the value even when a higher voltage is applied to the inputs.

As long as one of the input pins remains within the valid input range, and the supply voltage is valid and not in POR, the output state is correct.

The following is a summary of input voltage excursions and the outcomes:

1. When both IN- and IN+ are within the specified input voltage range:
   a. If IN- is higher than IN+ and the offset voltage, the output is low.
   b. If IN- is lower than IN+ and the offset voltage, the output is high.
2. When IN- is higher than the specified input voltage range and IN+ is within the specified voltage range, the output is low.
3. When IN+ is higher than the specified input voltage range and IN- is within the specified input voltage range, the output is high.
4. When IN- and IN+ are both outside the specified input voltage range, the output is indeterminate (random). Do not operate in this region.

Even with the fault tolerant feature, RUNIC strongly recommends keeping the inputs within the specified input voltage range during normal system operation to maintain data sheet specifications. Operating outside the

specified input range can cause changes in specifications such as propagation delay and input bias current, which can lead to unpredictable behavior.

8.4.3.3 Input Protection

The input bias current is typically 12pA for input voltages between V+ and V-. The comparator inputs are protected from negative voltage by the internal ESD diodes connected to V-. As the input voltage goes under V-, or above the input Absolute Maximum ratings, the protection diodes become forward biased and begin to conduct causing the input bias current to increase exponentially. Input bias current doubles for each 10°C temperature increase.

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, RUNIC recommends adding a current-limiting resistor in series with the input to limit any transient currents when the clamps conduct. See the ESD section for more information.

8.4.4 ESD Protection

The RS894X family incorporates internal ESD protection circuits on all pins. The inputs, and the open-drain output, use a proprietary "snapback" type ESD clamp from each pin to V-, which allows the pins to exceed the supply voltage (V+). While shown as Zener diodes, snapback "short" and go low impedance (like an SCR) when the threshold is exceeded, as opposed to clamping to a defined voltage like a Zener.

The RS894X open-drain output protection also consists of a ESD clamp between the output and V- to allow the output to be pulled above V+ to a maximum of 5.5V.

If the inputs are to be connected to a low impedance source, RUNIC recommends adding a current-limiting resistor in series with the input to limit input currents when the clamps conduct. The current must be limited 10mA or less. This series resistance can be part of any resistive input dividers or networks. RUNIC does not specify the performance of the ESD clamps and external clamping must be added if the inputs or output can exceed the maximum ratings as part of normal operation.

8.4.5 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency oscillations as the device triggers on it's own internal wideband noise. Instead, the inputs must be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage, or even V+ as long as the input is directly connected to the V+ pin to avoid transients.

8.4.6 Hysteresis

The RS894X family does not have internal hysteresis. Due to the wide effective bandwidth and low input offset voltage, there is a possibility for the output to "chatter" (oscillate) when the absolute differential voltage near zero as the comparator triggers on internal wideband noise. This is normal comparator behavior and is expected. RUNIC recommends that the user add external hysteresis if slow moving signals are expected. See Section 9.1.2 in the following section.

9 APPLICATION AND IMPLEMENTATION

Information in the following applications sections is not part of the RUNIC component specification, and RUNIC does not warrant its accuracy or completeness. RUNIC's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Basic Comparator Definitions

9.1.1.1 Operation

The basic comparator compares the input voltage (V_{IN}) on one input to a reference voltage (V_{REF}) on the other input. In the Comparator Timing Diagram example below, if V_{IN} is less than V_{REF}, the output voltage (V_O) is logic low (V_{OL}). If V_{IN} is greater than V_{REF}, the output voltage (V_O) is at logic high (V_{OH}). Output Conditions summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

Table 1. Output Conditions

Inputs Condition	Output
IN+ > IN-	HIGH (V_{OH})
IN+ = IN-	Indeterminate (chatters - see Hysteresis)
IN+ < IN	LOW (V_{OL})

9.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as t_{pLH} and t_{pHL} in Figure 28 and is measured from the mid-point of the input to the midpoint of the output.

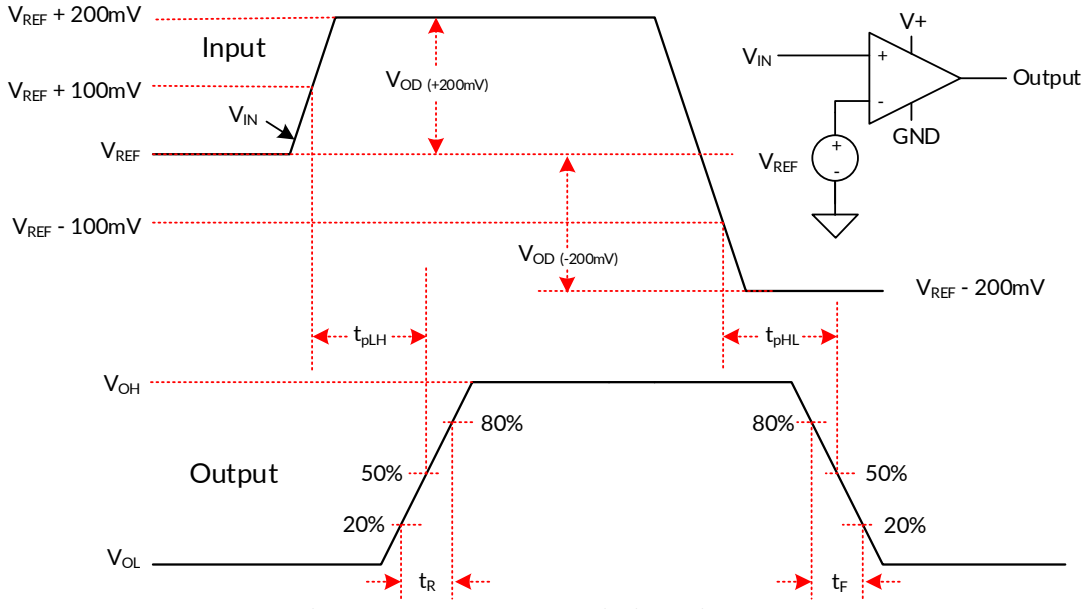


Figure 28. Comparator Timing Diagram

9.1.1.3 Overdrive Voltage

The overdrive voltage, V_{OD}, is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 200mV as shown in the Figure 28 example. The overdrive voltage can influence the propagation delay (tp). The smaller the overdrive voltage, the longer the propagation delay,

particularly when <100mV. If the fastest speeds are desired, RUNIC recommends applying the highest amount of overdrive possible.

The risetime (t_r) and falltime (t_f) is the time from the 20% and 80% points of the output waveform.

9.1.2 Hysteresis

The basic comparator configuration can oscillate or produce a noisy 'chatter' output if the applied differential input voltage is near the comparator's offset voltage. This usually occurs when the input signal is moving very slowly across the switching threshold of the comparator.

This problem can be prevented by the addition of hysteresis or positive feedback.

The hysteresis transfer curve is shown in Figure 29. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and V_{IN-}. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

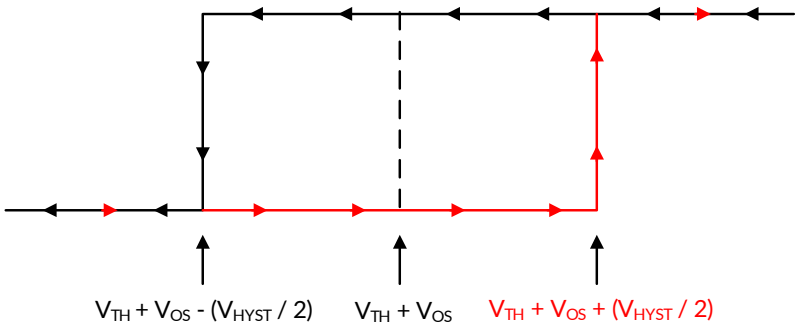


Figure 29. Hysteresis Transfer Curve

9.1.2.1 Inverting and Non-Inverting Hysteresis Using Open-Drain Output

An open drain output device, the RS894X, can be used as inverting and non-inverting hysteresis, and the output pull-up resistor must be taken into account in the calculations. The pull-up resistor is seen in series with the feedback resistor when the output is high. RUNIC recommends that the pull-up resistor be at least 10 times less than the feedback resistor value.

9.1.2.2 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V+), as shown in Figure 30.

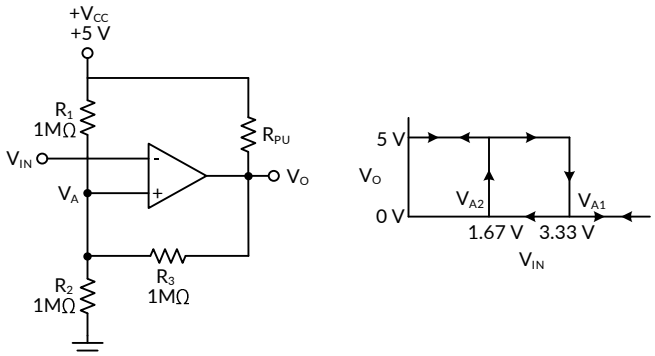


Figure 30. RS894X in an Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in Figure 30.

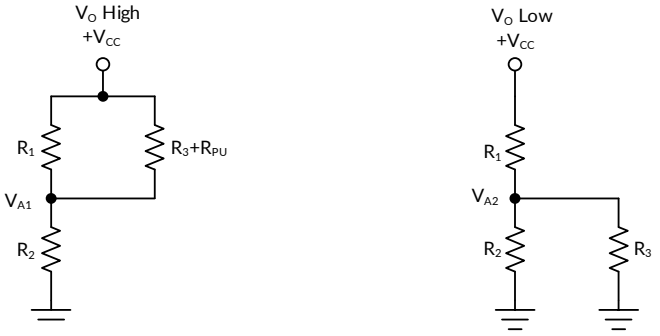


Figure 31. Inverting Configuration Resistor Equivalent Networks

When V_{IN} is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || (R3+R_{PU}) in series with R2, as shown in Figure 31.

Equation 1 below defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel (R3+R_{PU})) + R2} \quad (1)$$

When V_{IN} is greater than V_A, the output voltage is low. In this case, the three network resistors can be presented as R2 || R3 in series with R1, as shown in Equation 2.

Use Equation 2 to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \quad (2)$$

Equation 3 defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \quad (3)$$

9.1.2.3 Non-Inverting Comparator With Hysteresis

A noninverting comparator with hysteresis requires a two-resistor network and a voltage reference (V_{REF}) at the inverting input, as shown in Figure 32,

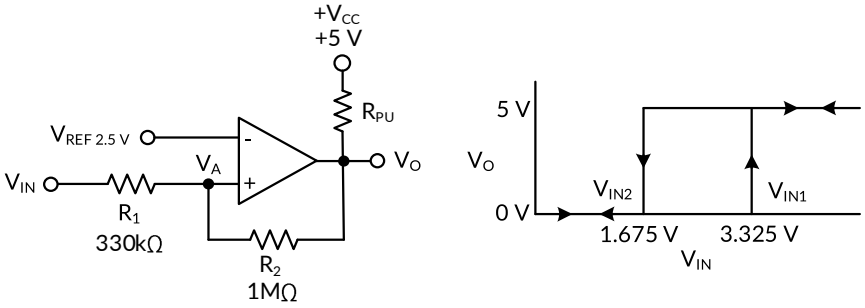


Figure 32. RS894X in a Non-Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in Figure 33.

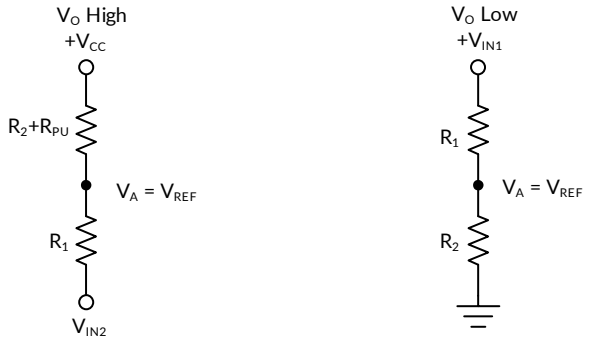


Figure 33. Non-Inverting Configuration Resistor Networks

When V_{IN} is less than V_{REF}, the output is low. For the output to switch from low to high, V_{IN} must rise above the V_{IN1} threshold. Use Equation 4 to calculate V_{IN1}.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \quad (4)$$

When V_{IN} is greater than V_{REF}, the output is high. For the comparator to switch back to a low state, V_{IN} must drop below V_{IN2}. Use Equation 5 to calculate V_{IN2}.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2 + R_{PU}) - V_{CC} \times R1}{R2 + R_{PU}} \quad (5)$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as shown in Equation 6.

$$\Delta V_{IN} = \frac{R1 \times V_{REF} \times R_{PU} + V_{CC} \times R1 \times R2}{R2(R2 + R_{PU})} \quad (6)$$

9.2 Typical Applications

9.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. Figure 34 shows a simple window comparator circuit. Window comparators require open drain outputs (RS894X) if the outputs are directly connected together.

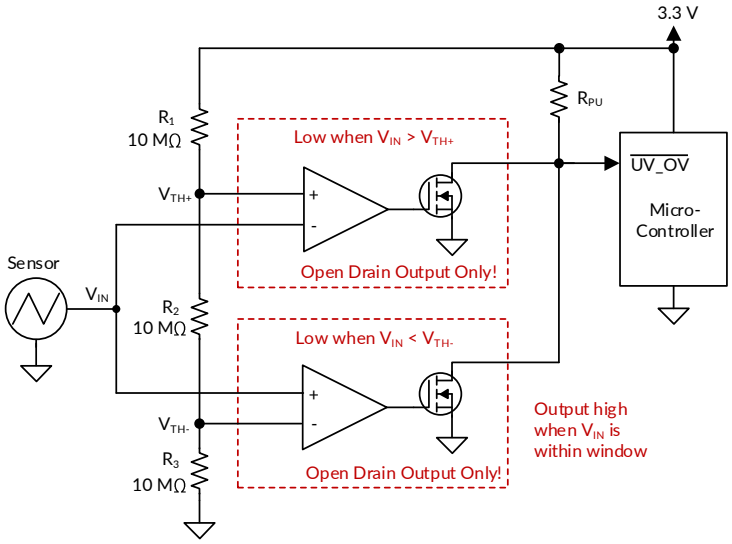


Figure 34. Window Comparator

9.2.1.1 Design Requirements

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 1.1V
- Alert (logic low output) when an input signal is greater than 2.2V
- Alert signal is active low
- Operate from a 3.3V power supply

9.2.1.2 Detailed Design Procedure

Configure the circuit as shown in Figure 34. Connect V_{CC} to a 3.3V power supply and V_{EE} to ground. Make R1, R2 and R3 each 10MΩ resistors. These three resistors are used to create the positive and negative thresholds for the window comparator (V_{TH+} and V_{TH-}).

With each resistor being equal, V_{TH+} is 2.2V and V_{TH-} is 1.1V. Large resistor values such as 10MΩ are used to minimize power consumption. The resistor values can be recalculated to provide the desired trip point values.

The sensor output voltage is applied to the inverting and noninverting inputs of the two comparators. Using two open-drain output comparators allows the two comparator outputs to be Wire-OR'ed together.

The respective comparator outputs are low when the sensor is less than 1.1V or greater than 2.2V. The respective comparator outputs are high when the sensor is in the range of 1.1V to 2.2V (within the "window"), as shown in Figure 35.

9.2.1.3 Application Curve

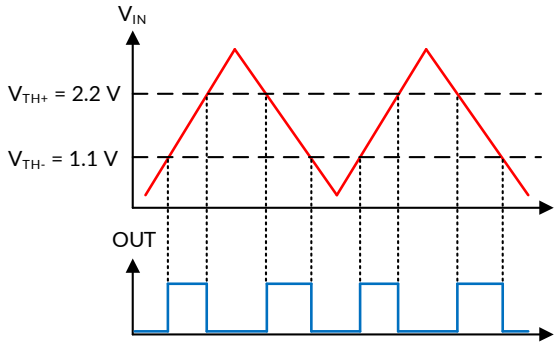


Figure 35. Window Comparator Results

9.2.2 Time Delay Generator

The circuit shown in Figure 36 provides output signals at a prescribed time interval from a time reference and automatically resets the output low when the input returns to 0V. This is useful for sequencing a "power on" signal to trigger a controlled start-up of power supplies.

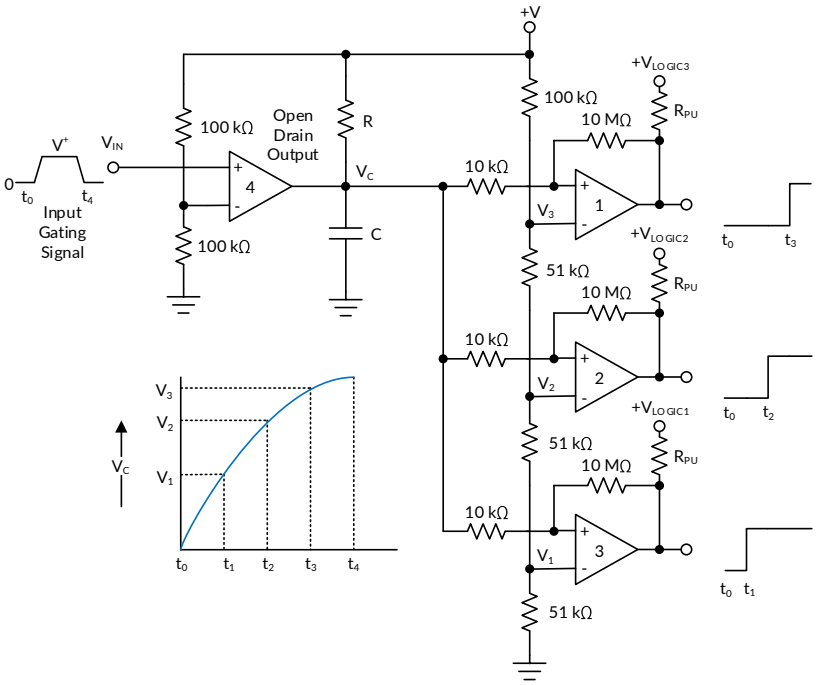


Figure 36. Time Delay Generator

Consider the case of V_{IN} = 0. The output of comparator 4 is also at ground, "shorting" the capacitor and holding the node to 0V. This implies that the outputs of comparators 1, 2, and 3 are also at 0V. When an input signal is applied, the output of open drain comparator 4 goes High-Z and C charges exponentially through R. This is indicated in the graph. The output voltages of comparators 1, 2, and 3 switch to the high state in sequence when V_C rises above the reference voltages V_1, V_2 and V_3. A small amount of hysteresis has been provided by the 10kΩ and 10MΩ resistors to insure smooth switching when the RC time constant is chosen to give long delay times. A good starting point is R = 100kΩ and C = 0.01µF to 1µF.

All outputs immediately go low when V_{IN} falls to 0V, due to the comparator output going low and immediately discharging the capacitor.

9.2.3 Logic Level Shifter

The output of the RS894X is the uncommitted drain of the output transistor. Many open-drain outputs can be tied together to provide an output OR'ing function if desired.

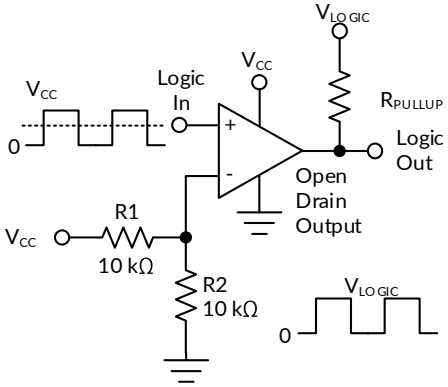


Figure 37. Universal Logic Level Shifter

The two 10kΩ resistors bias the input to half of the input logic supply level to set the threshold in the mid-point of the input logic levels. Only one shared output pull-up resistor is needed and can be connected to any pull-up voltage between 0V and 5.5V. The pullup voltage must match the driven logic input "high" level.

9.2.4 One-Shot Multivibrator

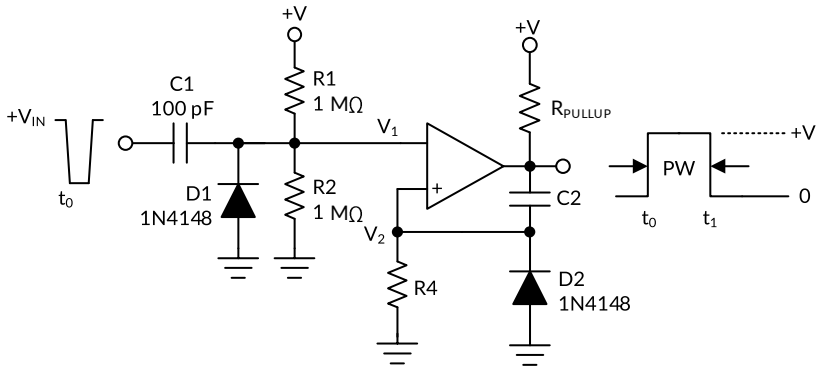


Figure 38. One-Shot Multivibrator

A monostable multivibrator has one stable state in which the output can remain indefinitely. The circuit can be triggered externally to another quasi-stable state. A monostable multivibrator can thus be used to generate a pulse of desired width.

The desired pulse width is set by adjusting the values of C_2 and R_4. The resistor divider of R_1 and R_2 can be used to determine the magnitude of the input trigger pulse. The output changes state when $V_1 < V_2$. Diode D_2 provides a rapid discharge path for capacitor C_2 to reset at the end of the pulse. The diode also prevents the non-inverting input from being driven below ground.

9.3 Power Supply Recommendations

Due to the fast output edges, proper supply bypassing is critical to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at each device with a low ESR 0.1µF ceramic bypass capacitor directly between V_{CC} pin and ground pins. Narrow, peak currents can be drawn during the output transition time. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device can be powered from either "split" supplies (V+, V- & GND), or a "single" supply (V+ and GND), with GND applied to the V- pin.

Input signals must stay within the specified input range (between V+ and V-) for either type.

Note that on "split" supplies, the output now swings "low" (V_{OL}) to V- potential and not GND.

10 LAYOUT

10.1 Layout Guidelines

For accurate comparator applications a stable power supply with minimized noise and glitches. Output rise and fall times are in the tens of nanoseconds, and must be treated as high speed logic devices. The bypass capacitor must be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the V_{CC} and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a V_{CC} or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (<100 ohms) resistor can also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations must be used when routing long distances.

10.2 Layout Example

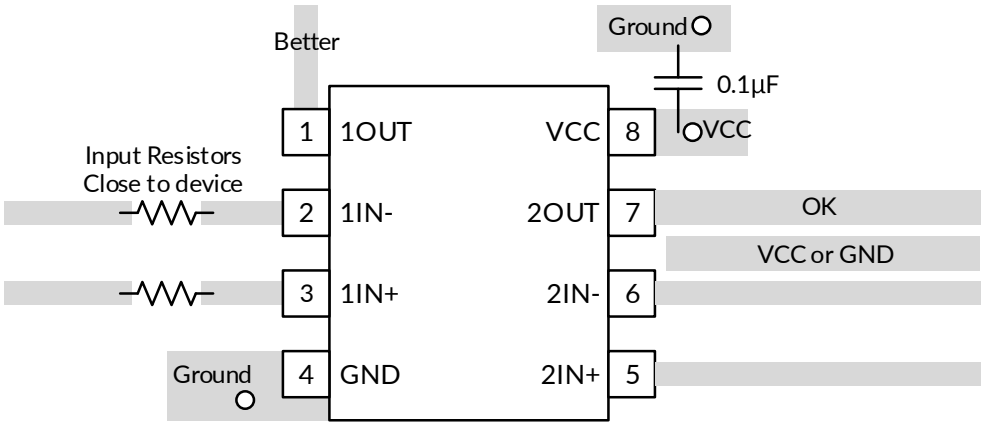
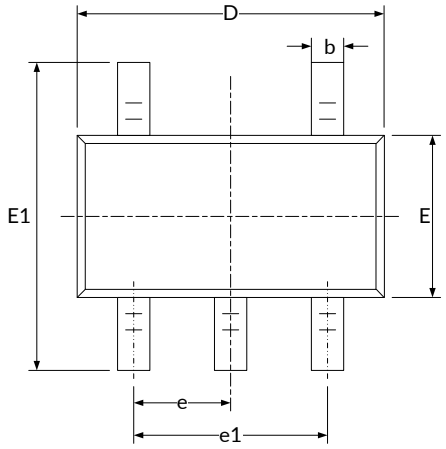
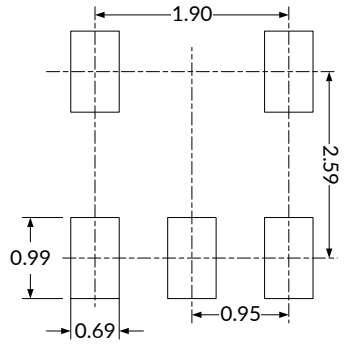


Figure 39. Dual Layout Example

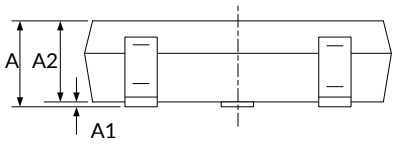
11 PACKAGE OUTLINE DIMENSIONS

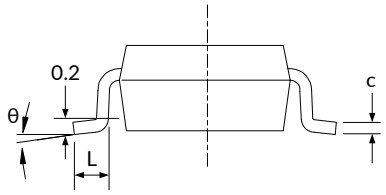
SOT23-5 (3)





RECOMMENDED LAND PATTERN (Unit: mm)



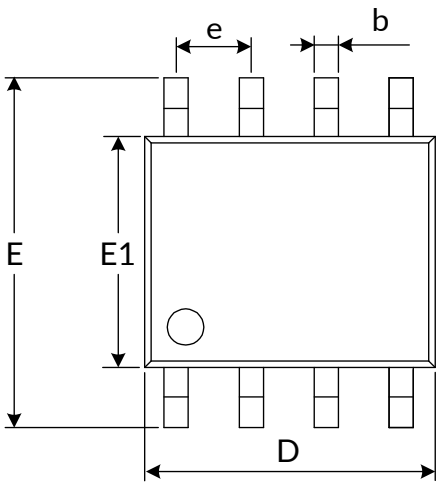


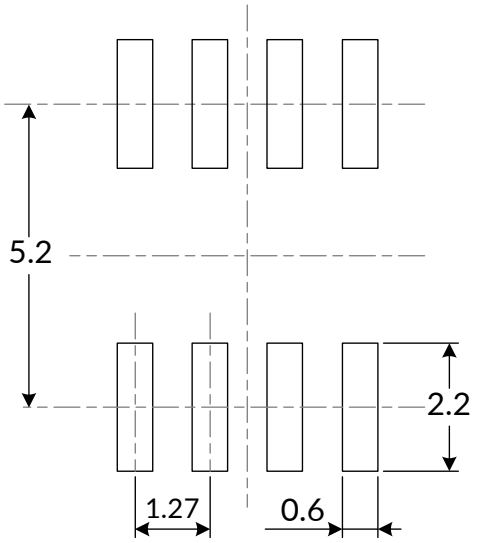
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D (1)	2.820	3.020	0.111	0.119
E (1)	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC) (2)		0.037(BSC) (2)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

NOTE:

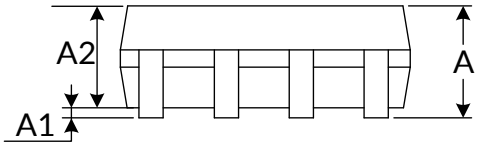
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

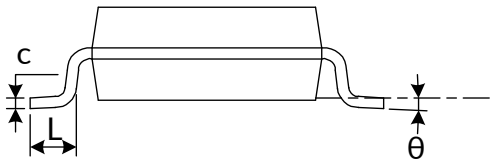
SOP8 (3)





RECOMMENDED LAND PATTERN (Unit: mm)



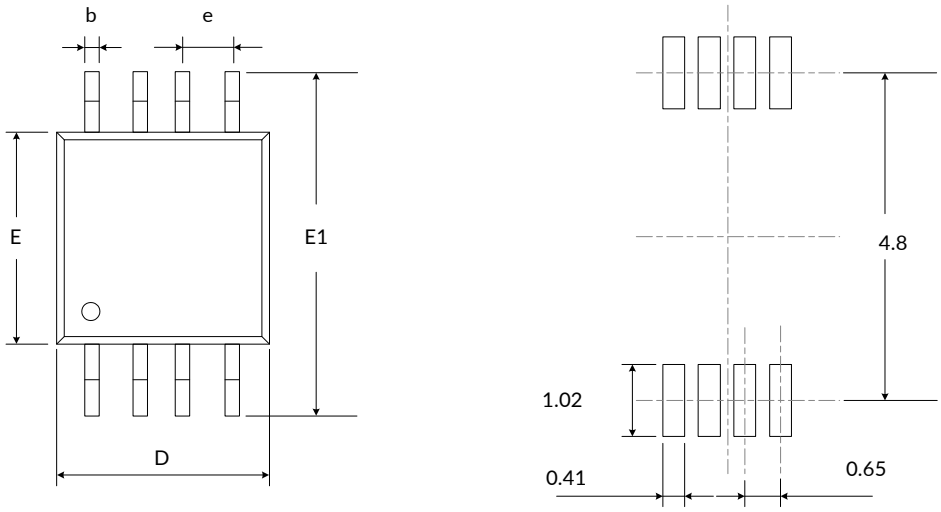


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D (1)	4.800	5.000	0.189	0.197
e	1.270(BSC) (2)		0.050(BSC) (2)	
E	5.800	6.200	0.228	0.244
E1 (1)	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

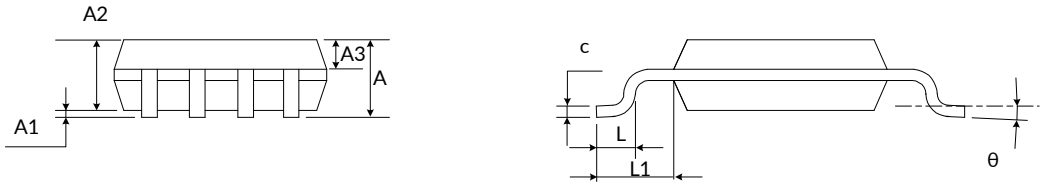
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

MSOP8 (4)



RECOMMENDED LAND PATTERN (Unit: mm)

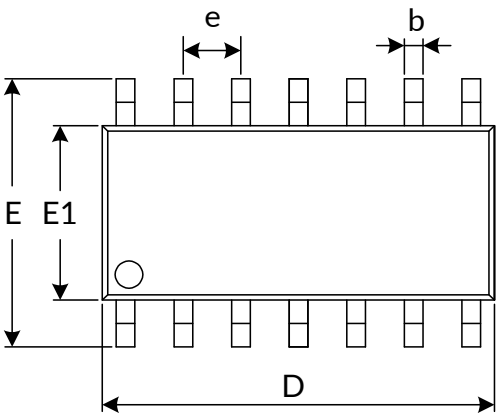


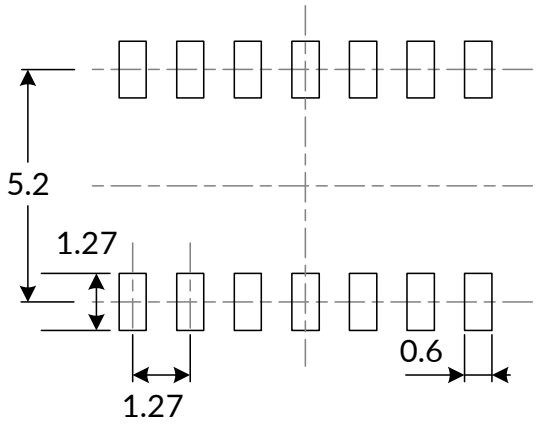
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.100		0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
A3	0.300	0.400	0.012	0.016
b	0.280	0.360	0.011	0.014
c	0.150	0.190	0.006	0.007
D (1)	2.900	3.100	0.114	0.122
e	0.650(BSC) (2)		0.026(BSC) (2)	
E (1)	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.200
L	0.400	0.700	0.016	0.027
L1	0.950(REF) (3)		0.037(REF) (3)	
θ	0°	8°	0°	8°

NOTE:

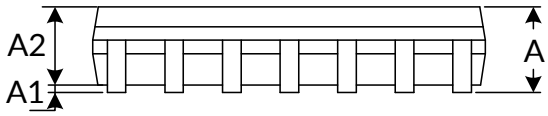
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. REF is the abbreviation for Reference.
4. This drawing is subject to change without notice.

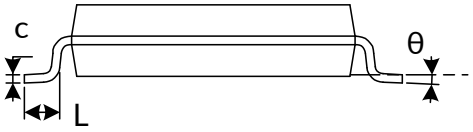
SOP14 (3)





RECOMMENDED LAND PATTERN (Unit: mm)

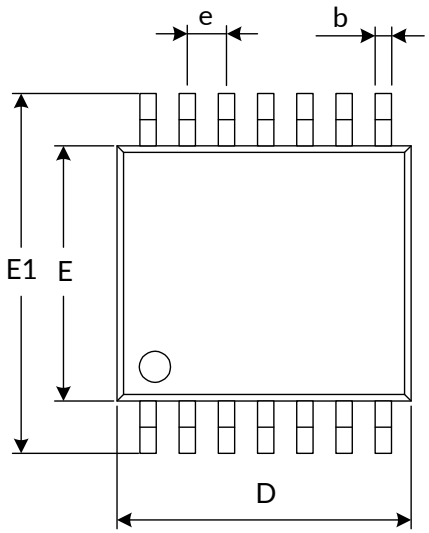


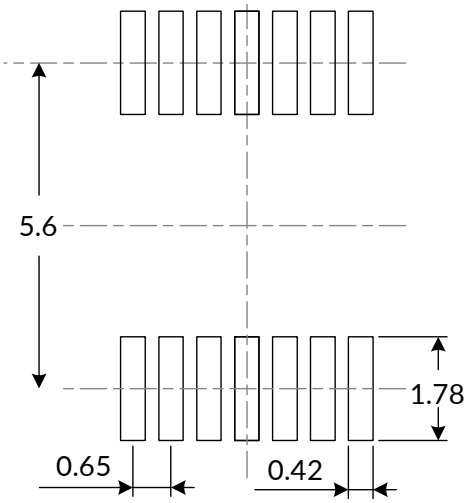


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D (1)	8.450	8.850	0.333	0.348
e	1.270(BSC) (2)		0.050(BSC) (2)	
E	5.800	6.200	0.228	0.244
E1 (1)	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

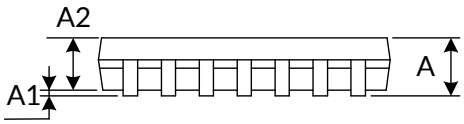
NOTE:
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

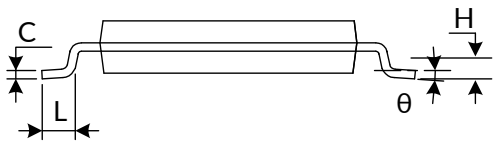
TSSOP14 (3)





RECOMMENDED LAND PATTERN (Unit: mm)





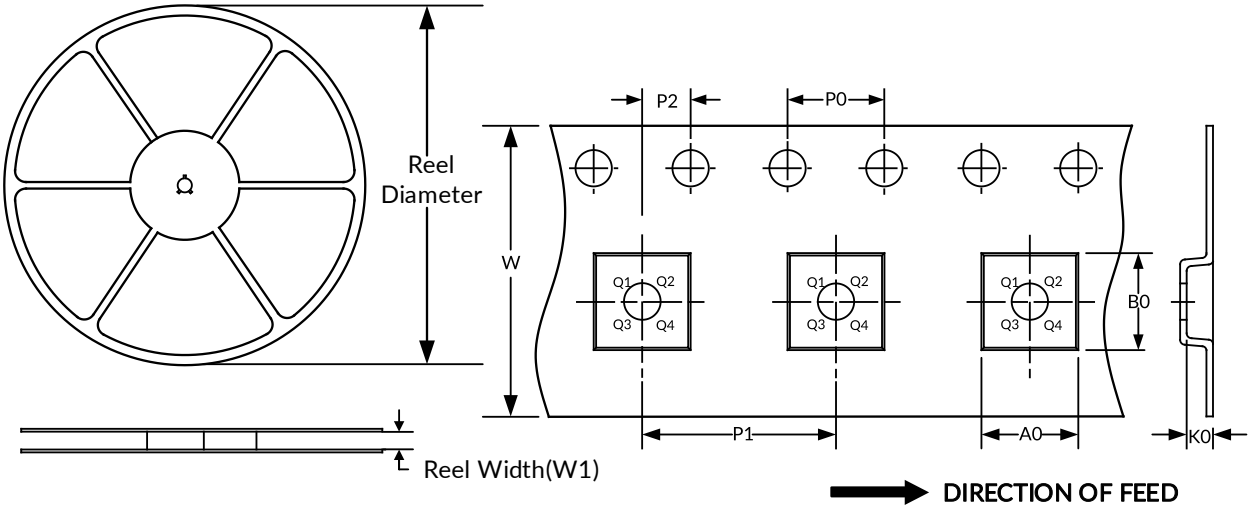
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D (1)	4.860	5.100	0.191	0.201
E (1)	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650(BSC) (2)		0.026(BSC) (2)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

NOTE:
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

12 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT23-5	7”	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
SOP8	13”	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
MSOP8	13”	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1
SOP14	13”	16.4	6.60	9.30	2.10	4.0	8.0	2.0	16.0	Q1
TSSOP14	13”	12.4	6.95	5.60	1.20	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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