# RS29548 Low-Voltage 8-Channel I$^2$C Switch with Reset

## 1 FEATURES

- **1-to-8 Bidirectional Translating Switches**
- **I$^2$C Bus and SMBus Compatible**
- **Active-Low Reset Input**
- **Three Address Pins, Allowing Up to Eight RS29548 Devices On the I$^2$C Bus**
- **Channel Selection Through an I$^2$C Bus, In Any Combination**
- **Power Up with All Switch Channels Deselected**
- **Low R$_{ON}$ Switches**
- **Allows Voltage-Level Translation Between 1.8V, 2.5V, 3.3V, and 5V Buses**
- **No Glitch On Power Up**
- **Supports Hot Insertion**
- **Low Standby Current**
- **Operating Power-Supply Voltage Range of 1.65V to 5.5V**
- **5V Tolerant Inputs**
- **0 to 400kHz Clock Frequency**

## 2 APPLICATIONS

- **Servers**
- **Routers (Telecom Switching Equipment)**
- **Factory Automation**
- **Products With I$^2$C Target Address Conflicts (Such As Multiple, Identical Temperature Sensors)**

## 3 DESCRIPTIONS

The RS29548 device has eight bidirectional translating switches that can be controlled through the I$^2$C bus. The SCL/SDA upstream pair fans out to eight downstream pairs, or channels. Any individual SCn/SDn channel or combination of channels can be selected, determined by the contents of the programmable control register. These downstream channels can be used to resolve I$^2$C target address conflicts. For example, if eight identical digital temperature sensors are needed in the application, one sensor can be connected at each channel: 0-7.

The system controller can reset the RS29548 in the event of a time-out, or other improper operation by asserting a low in the $\overline{\text{RESET}}$ input. Similarly, the power-on reset deselects all channels and initializes the I$^2$C/SMBus state machine. Asserting $\overline{\text{RESET}}$ causes the same reset and initialization to occur without powering down the part. This allows recovery if one of the downstream I$^2$C buses get stuck in a low state.

The pass gates of the switches are constructed so that the VCC pin can be used to limit the maximum high voltage, which is passed by the RS29548. Limiting the maximum high voltage allows the use of different bus voltages on each pair, so that 1.8V, 2.5V or 3.3V parts can communicate with 5V parts, without any additional protection. External pullup resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5.5V tolerant.

### Device Information [1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| RS29548 | TSSOP24 | 7.80mm×4.40mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.
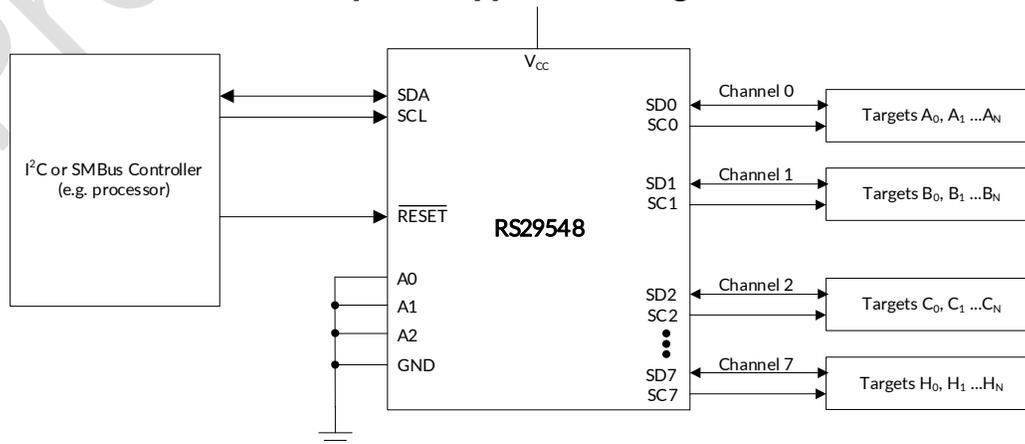
## Simplified Application Diagram

# Table of Contents

# 4 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

| Version | Change Date | Change Item |
|---------|-------------|-------------|
| A.0 | 2025/09/22 | Preliminary version completed |

## 5 PACKAGE/ORDERING INFORMATION (1)

| PRODUCT | ORDERING NUMBER | TEMPERATURE RANGE | PACKAGE LEAD | PACKAGE MARKING (2) | MSL(3) | PACKAGE OPTION |
|---|---|---|---|---|---|---|
| RS29548 | RS29548XTSS24 | -40°C ~125°C | TSSOP24 | RS29548 | MSL3 | Tape and Reel, 4000 |

NOTE:

(1)   This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2)   There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3)   RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F, Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

# 6 PIN CONFIGURATIONS AND FUNCTIONS

(TOP VIEW)

| | | | |
|---|---|---|---|
| A0 | 1 | 24 | VCC |
| A1 | 2 | 23 | SDA |
| $\overline{RESET}$ | 3 | 22 | SCL |
| SD0 | 4 | 21 | A2 |
| SC0 | 5 | 20 | SC7 |
| SD1 | 6 | 19 | SD7 |
| SC1 | 7 | 18 | SC6 |
| SD2 | 8 | 17 | SD6 |
| SC2 | 9 | 16 | SC5 |
| SD3 | 10 | 15 | SD5 |
| SC3 | 11 | 14 | SC4 |
| GND | 12 | 13 | SD4 |
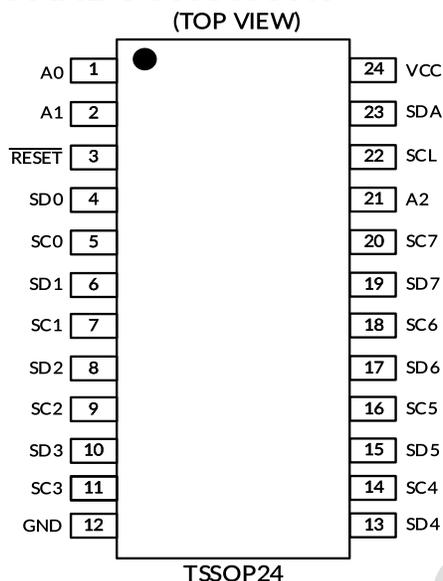
TSSOP24

## PIN DESCRIPTION

| PIN NAME | PIN TSSOP24 | TYPE [2] | DESCRIPTION |
|---|---|---|---|
| A0 | 1 | I | Address input 0. Connect directly to $V_{CC}$ or ground |
| A1 | 2 | I | Address input 1. Connect directly to $V_{CC}$ or ground |
| A2 | 21 | I | Address input 2. Connect directly to $V_{CC}$ or ground |
| GND | 12 | - | Ground |
| $\overline{RESET}$ | 3 | I | Active-low reset input. Connect to $V_{CC}$ or $V_{DPUM}$ [1] through a pull-up resistor, if not used |
| SD0 | 4 | I/O | Serial data 0. Connect to $V_{DPU0}$ [1] through a pull-up resistor |
| SC0 | 5 | I/O | Serial clock 0. Connect to $V_{DPU0}$ [1] through a pull-up resistor |
| SD1 | 6 | I/O | Serial data 1. Connect to $V_{DPU1}$ [1] through a pull-up resistor |
| SC1 | 7 | I/O | Serial clock 1. Connect to $V_{DPU1}$ [1] through a pull-up resistor |
| SD2 | 8 | I/O | Serial data 2. Connect to $V_{DPU2}$ [1] through a pull-up resistor |
| SC2 | 9 | I/O | Serial clock 2. Connect to $V_{DPU2}$ [1] through a pull-up resistor |
| SD3 | 10 | I/O | Serial data 3. Connect to $V_{DPU3}$ [1] through a pull-up resistor |
| SC3 | 11 | I/O | Serial clock 3. Connect to $V_{DPU3}$ [1] through a pull-up resistor |
| SD4 | 13 | I/O | Serial data 4. Connect to $V_{DPU4}$ [1] through a pull-up resistor |
| SC4 | 14 | I/O | Serial clock 4. Connect to $V_{DPU4}$ [1] through a pull-up resistor |
| SD5 | 15 | I/O | Serial data 5. Connect to $V_{DPU5}$ [1] through a pull-up resistor |
| SC5 | 16 | I/O | Serial clock 5. Connect to $V_{DPU5}$ [1] through a pull-up resistor |
| SD6 | 17 | I/O | Serial data 6. Connect to $V_{DPU6}$ [1] through a pull-up resistor |
| SC6 | 18 | I/O | Serial clock 6. Connect to $V_{DPU6}$ [1] through a pull-up resistor |
| SD7 | 19 | I/O | Serial data 7. Connect to $V_{DPU7}$ [1] through a pull-up resistor |
| SC7 | 20 | I/O | Serial clock 7. Connect to $V_{DPU7}$ [1] through a pull-up resistor |
| SCL | 22 | I/O | Serial clock bus. Connect to $V_{DPUM}$ [1] through a pull-up resistor |
| SDA | 23 | I/O | Serial data bus. Connect to $V_{DPUM}$ [1] through a pull-up resistor |
| VCC | 24 | Power | Supply voltage |

(1)  $V_{DPUX}$ is the pull-up reference voltage for the associated data line. $V_{DPUM}$ is the controller I$^2$C reference voltage and $V_{DPU0}$-$V_{DPU7}$ are the target channel reference voltages.

(2)  I=input, O=output, I/O=input and output.

# 7 SPECIFICATIONS

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5 | 6.5 | V |
| $V_I$ | Input voltage [2] | | −0.5 | 6.5 | V |
| $I_I$ | Input current | | -20 | 20 | mA |
| $I_O$ | Output current | | -25 | | mA |
| $I_{CC}$ | Supply current | | -100 | 100 | mA |
| $T_{stg}$ | Storage temperature | | −65 | 150 | °C |
| $\theta_{JA}$ | Package thermal impedance [3] | TSSOP24 | | 35 | °C/W |
| $T_J$ | Max Junction Temperature [4] | $V_{CC} \leq 3.6$ V | | 130 | °C |
| | | $V_{CC} \leq 5.5$ V | | 90 | |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD-51.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and $T_A$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

## 7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-Body Model (HBM), JESD22-a114 | ±4000 | V |
| | | Charged-Device Model (CDM), ANSI/ESDA/JEDEC JS-002-2022 | ±1000 | V |

**ESD SENSITIVITY CAUTION**

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted).

| PARAMETER | | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | 1.65 | | 5.5 | V |
| $V_{IH}$ | High-level input voltage | SCL, SDA | $V_{CC}$=1.65V to 2.3V | 0.75 × $V_{CC}$ | | 5.5 | V |
| | | | $V_{CC}$=2.3V to 5.5V | 0.7 × $V_{CC}$ | | 5.5 | |
| | | A2–A0, $\overline{RESET}$ | | 0.7 × $V_{CC}$ | | $V_{CC}$ | |
| $V_{IL}$ | Low-level input voltage | SCL, SDA | $V_{CC}$=1.65V to 2.3V | -0.5 | | 0.25 × $V_{CC}$ | V |
| | | | $V_{CC}$=2.3V to 5.5V | -0.5 | | 0.3 × $V_{CC}$ | |
| | | A2–A0, $\overline{RESET}$ | | -0.5 | | 0.3 × $V_{CC}$ | V |
| $T_A$ | Operating free-air temperature | | | -40 | | 125 | °C |

## 7.4 Electrical Characteristics

$V_{CC}$ = 1.65 V to 5.5 V, over recommended operating free-air temperature ranges supported by Recommended Operating Conditions (unless otherwise noted). [1] All typical values are at nominal supply voltage (1.8, 2.5, 3.3, or 5V $V_{CC}$), $T_A$ = 25°C.

| PARAMETER | | CONDITIONS | $V_{CC}$ | TEMP | MIN[2] | TYP[3] | MAX[2] | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{PORR}$ | Power-On Reset Voltage, $V_{CC}$ Rising | No load, $V_I$ = $V_{CC}$ or GND [4] | | FULL | | 1.2 | 1.6 | V |
| $V_{PORF}$ | Power-On Reset Voltage, $V_{CC}$ Falling [5] | No load, $V_I$ = $V_{CC}$ or GND [4] | | FULL | 0.8 | 1 | | |
| $V_{o(sw)}$ | Switch Output Voltage | $V_{i(sw)}$ = $V_{CC}$, $I_{SWout}$ = −100μA | 5V | +25°C | | 3.6 | | V |
| | | | 4.5V to 5.5V | FULL | 2.6 | | 4.5 | |
| | | | 3.3V | +25°C | | 1.9 | | |
| | | | 3V to 3.6V | FULL | 1.6 | | 2.8 | |
| | | | 2.5V | +25°C | | 1.5 | | |
| | | | 2.3V to 2.7V | FULL | 1.1 | | 2 | |
| | | | 1.8V | +25°C | | 1.1 | | |
| | | | 1.65V to 1.95V | FULL | 0.6 | | 1.25 | |
| $I_{OL}$ | SDA | $V_{OL}$ = 0.4V | 1.65V to 5.5V | FULL | 3 | 6 | | mA |
| | | $V_{OL}$ = 0.6V | | FULL | 6 | 9 | | |
| $I_I$ | SCL, SDA | $V_I$ = $V_{CC}$ or GND [4] | 1.65V to 5.5V | FULL | -2 | | 2 | μA |
| | SC7−SC0, SD7−SD0 | | | FULL | -2 | | 2 | |
| | A2−A0 | | | FULL | -2 | | 2 | |
| | $\overline{RESET}$ | | | FULL | -2 | | 2 | |
| $I_{CC}$ | Operating Mode | $f_{SCL}$ = 400kHz $V_I$= $V_{CC}$ or GND [4], $I_O$=0 | 5.5V | FULL | | 50 | 80 | μA |
| | | | 3.3V | FULL | | 20 | 35 | |
| | | | 1.65V | FULL | | 6 | 10 | |
| | | $f_{SCL}$ = 100kHz $V_I$= $V_{CC}$ or GND [4], $I_O$=0 | 5.5V | FULL | | 9 | 30 | |
| | | | 3.3V | FULL | | 6 | 15 | |
| | | | 1.65V | FULL | | 2 | 4 | |
| | Standby Mode | Low inputs $V_I$=GND [4], $I_O$=0 | 5.5V | FULL | | 0.2 | 2 | |
| | | | 3.6V | FULL | | 0.1 | 2 | |
| | | | 2.7V | FULL | | 0.1 | 1 | |
| | | | 1.65V | FULL | | 0.1 | 1 | |
| | | High inputs $V_I$=$V_{CC}$, $I_O$=0 | 5.5V | FULL | | 0.2 | 2 | |
| | | | 3.6V | FULL | | 0.1 | 2 | |
| | | | 2.7V | FULL | | 0.1 | 1 | |
| | | | 1.65V | FULL | | 0.1 | 1 | |
| $\Delta I_{cc}$ | Supply-Current Change SCL, SDA | SCL or SDA input at 0.6V, Other inputs at $V_{CC}$ or GND [4] | 1.65V to 5.5V | FULL | | 3 | 20 | μA |
| | | SCL or SDA input at $V_{CC}$ − 0.6V, Other inputs at $V_{CC}$ or GND [4] | | FULL | | 3 | 20 | |
| $C_i$ | A2−A0 | $V_I$=$V_{CC}$ or GND [4] | 1.65V to 5.5V | +25°C | | 4 | 5 | pF |
| | $\overline{RESET}$ | | | +25°C | | 4 | 5 | |
| | SCL | $V_I$=$V_{CC}$ or GND [4], Switch OFF | | +25°C | | 20 | 28 | |
| $C_{io(off)}$ [6] | SDA | $V_I$= $V_{CC}$ or GND [4], Switch OFF | 1.65V to 5.5V | +25°C | | 20 | 28 | pF |
| | SC7−SC0, SD7−SD0 | | | +25°C | | 5.5 | 7.5 | |

| $R_{ON}$ | Switch-On Resistance | $V_O$ = 0.4 V, $I_O$ = 10mA | 2.3V to 2.7 V | FULL | 7 | 15 | 45 | Ω |
|---|---|---|---|---|---|---|---|---|
| | | | 1.65V to 1.95V | FULL | 10 | 25 | 70 | |
| | | $V_O$ = 0.4 V, $I_O$ = 15mA | 4.5V to 5.5V | FULL | 4 | 10 | 20 | Ω |
| | | | 3V to 3.6V | FULL | 5 | 12 | 30 | |

(1) For operation between specified voltage ranges, refer to the worst-case parameter in both applicable ranges.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

(4) $\overline{RESET}$ = $V_{CC}$ (held high) when all other input voltages, $V_I$ = GND.

(5) The power-on reset circuit resets the I²C bus logic with $V_{CC}$ < $V_{PORF}$.

(6) $C_{io(ON)}$ depends on internal capacitance and external capacitance added to the SCn lines when channels(s) are ON.

## 7.5 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| **STANDARD MODE** | | | | | |
| $t_{scl}$ | I²C clock frequency | | 0 | 400 | kHz |
| $t_{sch}$ | I²C clock high time | | 0.6 | | µs |
| $t_{scl}$ | I²C clock low time | | 1.3 | | µs |
| $t_{sp}$ | I²C spike time | | | 50 | ns |
| $t_{sds}$ | I²C serial-data setup time | | 100 | | ns |
| $t_{sdh}$ | I²C serial-data hold time | | 10 [1] | | ns |
| $t_{icr}$ | I²C input rise time | | $20+0.1C_b$ [3] | 300 | ns |
| $t_{icf}$ | I²C input fall time | | $20+0.1C_b$ [3] | 300 | ns |
| $t_{ocf}$ | I²C output (SDn) fall time (10pF to 400pF bus) | | $20+0.1C_b$ [3] | 300 | ns |
| $t_{buf}$ | I²C bus free time between stop and start | | 1.3 | | µs |
| $t_{sts}$ | I²C start or repeated start condition setup | | 0.6 | | µs |
| $t_{sth}$ | I²C start or repeated start condition hold | | 0.6 | | µs |
| $t_{sps}$ | I²C stop condition setup | | 0.6 | | µs |
| $t_{vdL(Data)}$ | Valid-data time (high to low) [2] | SCL low to SDA output low valid | | 1 | µs |
| $t_{vdH(Data)}$ | Valid-data time (low to high) [2] | SCL low to SDA output high valid | | 0.6 | µs |
| $t_{vd(ack)}$ | Valid-data time of ACK condition | ACK signal from SCL low to SDA output low | | 1 | µs |
| $C_b$ | I²C bus capacitive load | | | 400 | pF |

(1) A device internally must provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH}$ min of the SCL signal), to bridge the undefined region of the falling edge of SCL.
(2) Data taken using a 1kΩ pull-up resistor and 50pF load.
(3) $C_b$ = total bus capacitance of one bus line in pF.

## 7.6 Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

| | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{W(L)}$ | Pulse duration, $\overline{RESET}$ low | 6 | | ns |
| $t_{REC(STA)}$ | Recovery time from $\overline{RESET}$ to start | 0 | | ns |

## 7.7 Switching Characteristics

over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted)

| PARAMETER | | | FROM (INPUT) | TO (OUTPUT) | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{pd}$ [1] | Propagation delay time | $R_{ON}=20Ω, C_L=15pF$ | SDA or SCL | SDn or SCn | | 0.3 | ns |
| | | $R_{ON}=20Ω, C_L=50pF$ | | | | 1 | |
| $t_{rst}$ [2] | $\overline{RESET}$ time (SDA clear) | | $\overline{RESET}$ | SDA | | 500 | ns |

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by anideal voltage source (zero output impedance).
(2) $t_{rst}$ is the propagation delay measured from the time the $\overline{RESET}$ pin is first asserted low to the time the SDA pin is asserted high, signaling a stop condition. It must be a minimum of $t_{WL}$.

## 7.8 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.
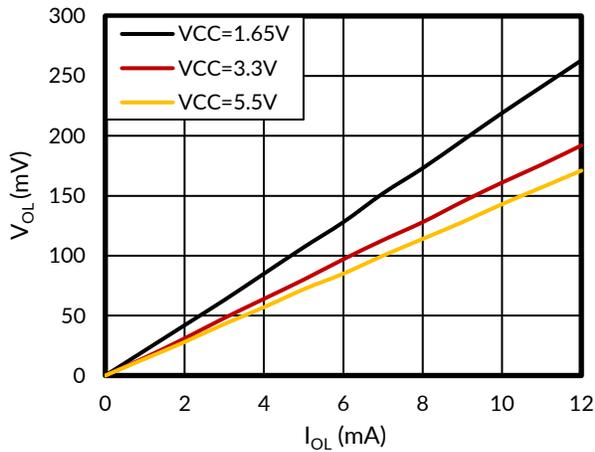


Figure 1. SDA Output Low Voltage ($V_{OL}$) vs Load Current ($I_{OL}$) at Three $V_{CC}$ Levels ($T_A$ = 25°C)
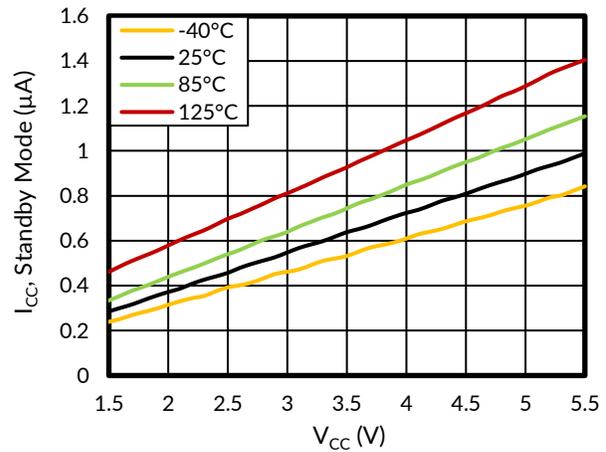


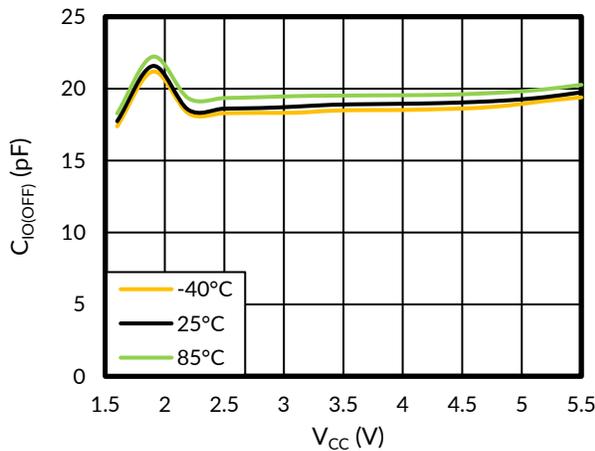Figure 2. Standby Current ($I_{CC}$) vs Supply Voltage ($V_{CC}$) at Four Temperature Points



Figure 3. Target Channel (SCn/SDn) Capacitance ($C_{io(OFF)}$) vs Supply Voltage ($V_{CC}$) at Three Temperature Points
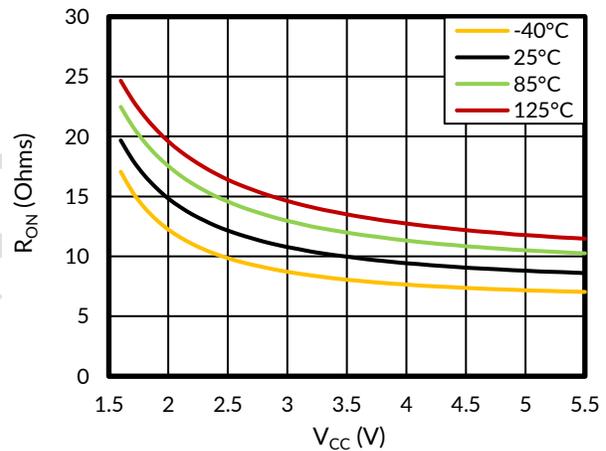


Figure 4. On-Resistance ($R_{ON}$) vs Supply Voltage ($V_{CC}$) at Four Temperature Points
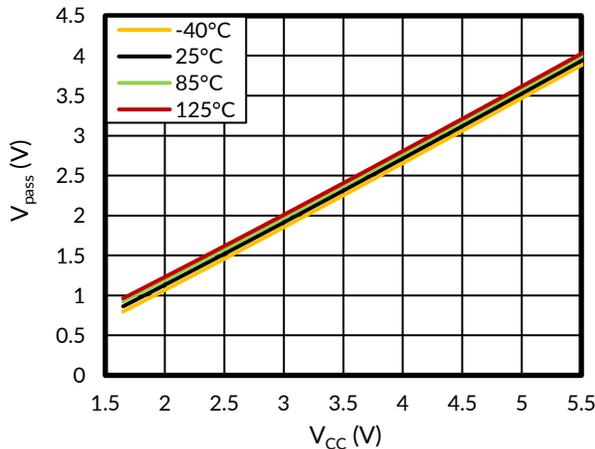


Figure 5. Pass-Gate Voltage ($V_{pass}$) vs Supply Voltage ($V_{CC}$) at Four Temperature Points
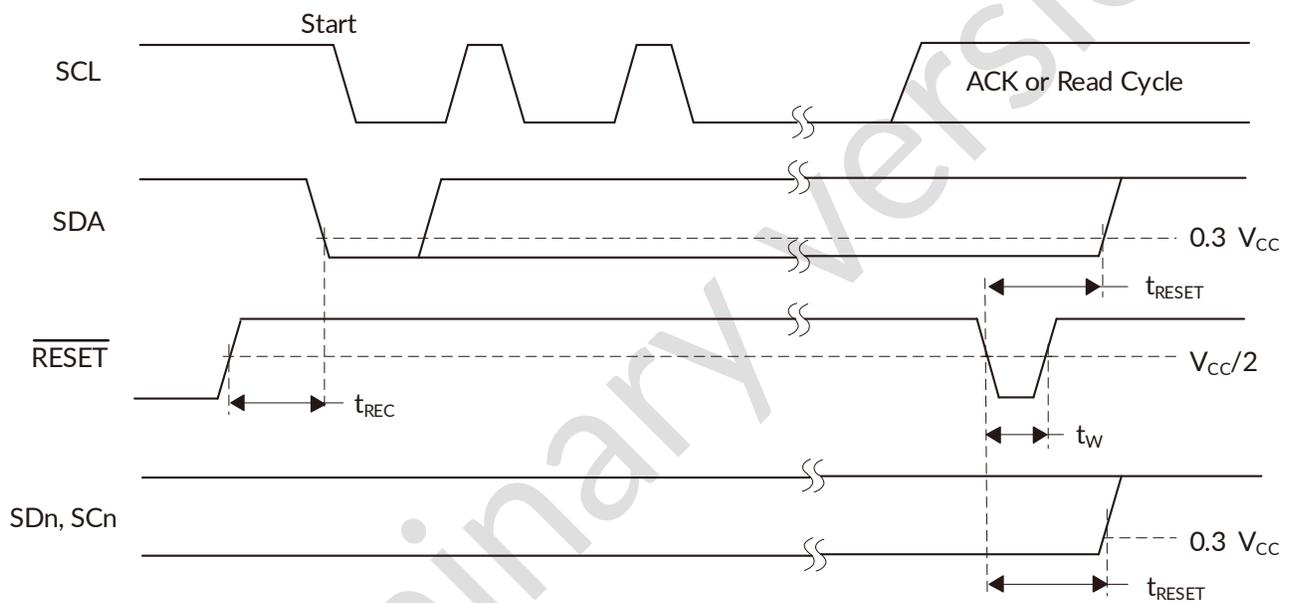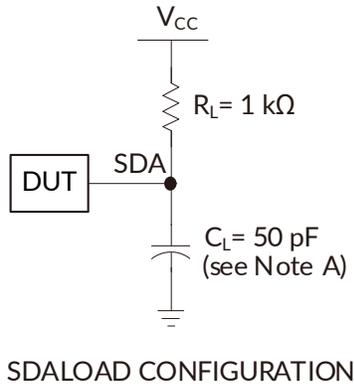
# 8 PARAMETER MEASUREMENT INFORMATION



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

| BYTE | DESCRIPTION |
|------|-------------|
| 1 | $I^2C$ address |
| 2, 3 | P-port data |

A. $C_L$ includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10MHz, $Z_O$ = 50Ω, $t_r/t_f$ ≤ 30ns.
C. Not all parameters and waveforms are applicable to all devices.

**Figure 6. I²C Load Circuit and Voltage Waveforms**

SDALOAD CONFIGURATION



A. $C_L$ includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10MHz, $Z_O$ = 50Ω, $t_r/t_f$ ≤ 30ns.
C. I/Os are configured as inputs.
D. Not all parameters and waveforms are applicable to all devices.

**Figure 7. Reset Load Circuit and Voltage Waveforms**

# 9 DETAILED DESCRIPTION

## 9.1 Overview

The RS29548 is an 8-channel, bidirectional translating I²C switch. The controller SCL/SDA signal pair is directed to eight channels of target devices, SC0/SD0-SC7/SD7. Any individual downstream channel can be selected as well as any combination of the eight channels.

The device offers an active-low $\overline{RESET}$ input which resets the state machine and allows the RS29548 to recover must one of the downstream I²C buses get stuck in a low state. The state machine of the device can also be reset by cycling the power supply, $V_{CC}$, also known as a power-on reset (POR). Both the $\overline{RESET}$ function and a POR cause all channels to be deselected.

The connections of the I²C data path are controlled by the same I²C controller device that is switched to communicate with multiple I²C targets. After the successful acknowledgment of the target address (hardware selectable by A0, A1, and A2 pins), a single 8-bit control register is written to or read from to determine the selected channels.

The RS29548 may also be used for voltage translation, allowing the use of different bus voltages on each SCn/SDn pair such that 1.8V, 2.5V, or 3.3V parts can communicate with 5V parts. This is achieved by using external pull-up resistors to pull the bus up to the desired voltage for the controller and each target channel.

## 9.2 Functional Block Diagram
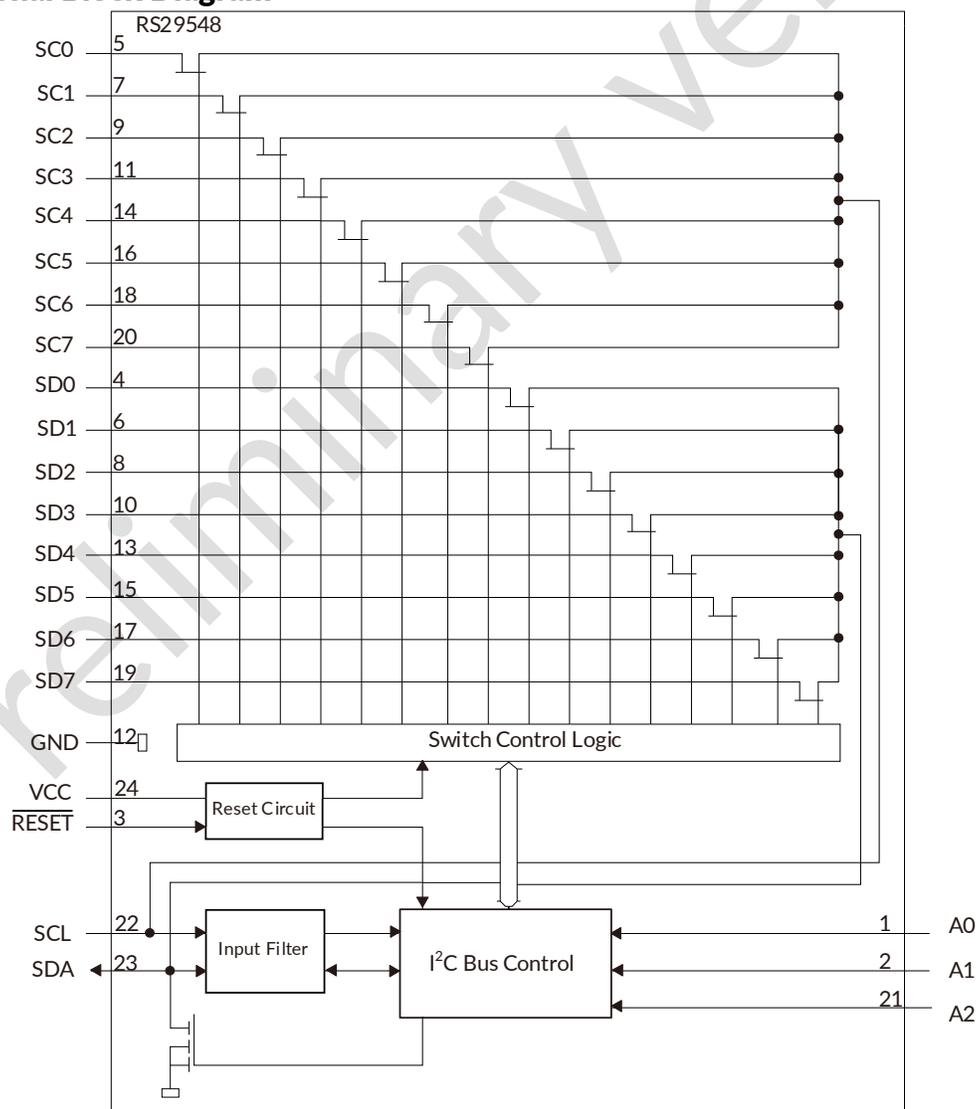
## 9.3 Feature Description

The RS29548 is an 8-channel, bidirectional translating switch for I$^2$C buses that supports Standard-Mode (100kHz) and Fast-Mode (400kHz) operation. The RS29548 features I$^2$C control using a single 8-bit control register in which each bit controls the enabling and disabling of one of the corresponding 8 switch channels for I$^2$C data flow. Depending on the application, voltage translation of the I$^2$C bus can also be achieved using the RS29548 to allow 1.8V, 2.5V, or 3.3V parts to communicate with 5V parts. Additionally, in the event that communication on the I$^2$C bus enters a fault state, the RS29548 can be reset to resume normal operation using the $\overline{RESET}$ pin feature or by a power-on reset which results from cycling power to the device.

## 9.4 Device Functional Modes

### 9.4.1 $\overline{RESET}$ Input

The $\overline{RESET}$ input is an active-low signal that may be used to recover from a bus-fault condition. When this signal is asserted low for a minimum of $t_{WL}$, the RS29548 resets its registers and I$^2$C state machine and deselects all channels. The $\overline{RESET}$ input must be connected to $V_{CC}$ through a pull-up resistor.

### 9.4.2 Power-On Reset

When power is applied to the VCC pin, an internal power-on reset holds the RS29548 in a reset condition until $V_{CC}$ has reached $V_{PORR}$. At this point, the reset condition is released, and the RS29548 registers and I$^2$C state machine are initialized to their default states, all zeroes, causing all the channels to be deselected. Thereafter, $V_{CC}$ must be lowered below $V_{PORF}$ to reset the device.

## 9.5 Programming

### 9.5.1 I$^2$C Interface

The RS29548 has a standard bidirectional I$^2$C interface that is controlled by a controller device in order to be configured or read the status of this device. Each target on the I$^2$C bus has a specific device address to differentiate between other target devices that are on the same I$^2$C bus. Many target devices require configuration upon startup to set the behavior of the device. This is typically done when the controller accesses internal register maps of the target, which have unique register addresses. A device can have one or multiple registers where data is stored, written, or read.

The physical I$^2$C interface consists of the serial clock (SCL) and serial data (SDA) lines. Both SDA and SCL lines must be connected to $V_{CC}$ through a pull-up resistor. The size of the pull-up resistor is determined by the amount of capacitance on the I$^2$C lines. Data transfer may be initiated only when the bus is idle. A bus is considered idle if both SDA and SCL lines are high after a STOP condition (See Figure 8 and Figure 9).

The following is the general procedure for a controller to access a target device:

1. If a controller wants to send data to a target:
   - Controller-transmitter sends a START condition and addresses the target-receiver.
   - Controller-transmitter sends data to target-receiver.
   - Controller-transmitter terminates the transfer with a STOP condition.

2. If a controller wants to receive or read data from a target:
   - Controller-receiver sends a START condition and addresses the target-transmitter.
   - Controller-receiver sends the requested register to read to target-transmitter.
   - Controller-receiver receives data from the target-transmitter.
   - Controller-receiver terminates the transfer with a STOP condition.
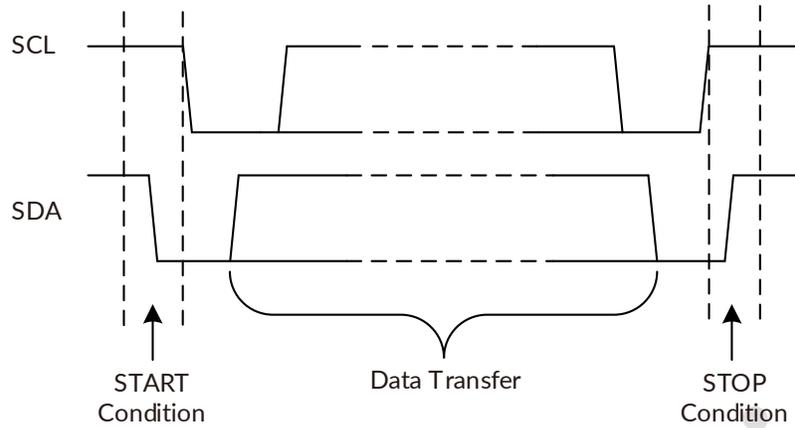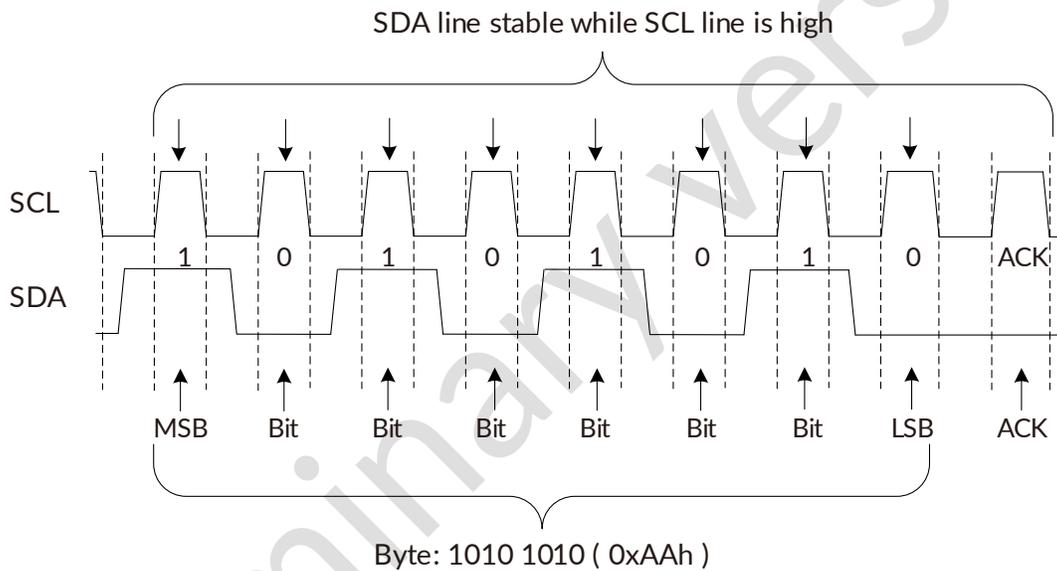
**Figure 8. Definition of Start and Stop Conditions**



Byte: 1010 1010 ( 0xAAh )

**Figure 9. Bit Transfer**

## 9.5.2 Device Address
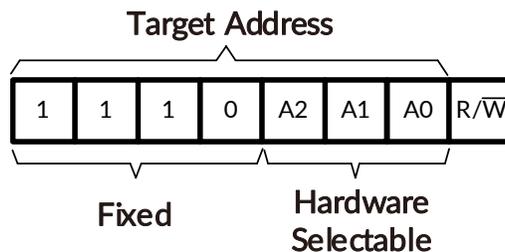Figure 10 shows the address byte of the RS29548.



**Figure 10. RS29548 Address**

The last bit of the target address defines the operation (read or write) to be performed. When it is high (1), a read is selected, while a low (0) selects a write operation.
Table 1 shows the RS29548 address reference.

## Table 1. Address Reference

| INPUTS | | | I²C BUS TARGETADDRESS |
|---|---|---|---|
| A2 | A1 | A0 | |
| L | L | L | 112 (decimal), 70 (hexadecimal) |
| L | L | H | 113 (decimal), 71 (hexadecimal) |
| L | H | L | 114 (decimal), 72 (hexadecimal) |
| L | H | H | 115 (decimal), 73 (hexadecimal) |
| H | L | L | 116 (decimal), 74 (hexadecimal) |
| H | L | H | 117 (decimal), 75 (hexadecimal) |
| H | H | L | 118 (decimal), 76 (hexadecimal) |
| H | H | H | 119 (decimal), 77 (hexadecimal) |

### 9.5.3 Bus Transactions

Data must be sent to and received from the target devices, and this is accomplished by reading from or writing to registers in the target device.

Registers are locations in the memory of the target which contain information, whether it be the configuration information or some sampled data to send back to the controller. The controller must write information to these registers in order to instruct the target device to perform a task.

While it is common to have registers in I²C targets, note that not all target devices have registers. Some devices are simple and contain only 1 register, which may be written to directly by sending the register data immediately after the target address, instead of addressing a register. The RS29548 is example of a single-register device, which is controlled via I²C commands. Since it has 1 bit to enable or disable a channel, there is only 1 register needed, and the controller merely writes the register data after the target address, skipping the register number.

### 9.5.3.1 Writes

To write on the I²C bus, the controller sends a START condition on the bus with the address of the target, as well as the last bit (the R/$\overline{W}$ bit) set to 0, which signifies a write. The target acknowledges, letting the controller know it is ready. After this, the controller starts sending the control register data to the target until the controller has sent all the data necessary (which is sometimes only a single byte), and the controller terminates the transmission with a STOP condition.

There is no limit to the number of bytes sent, but the last byte sent is what is in the register.

Figure 11 shows an example of writing a single byte to a target register.
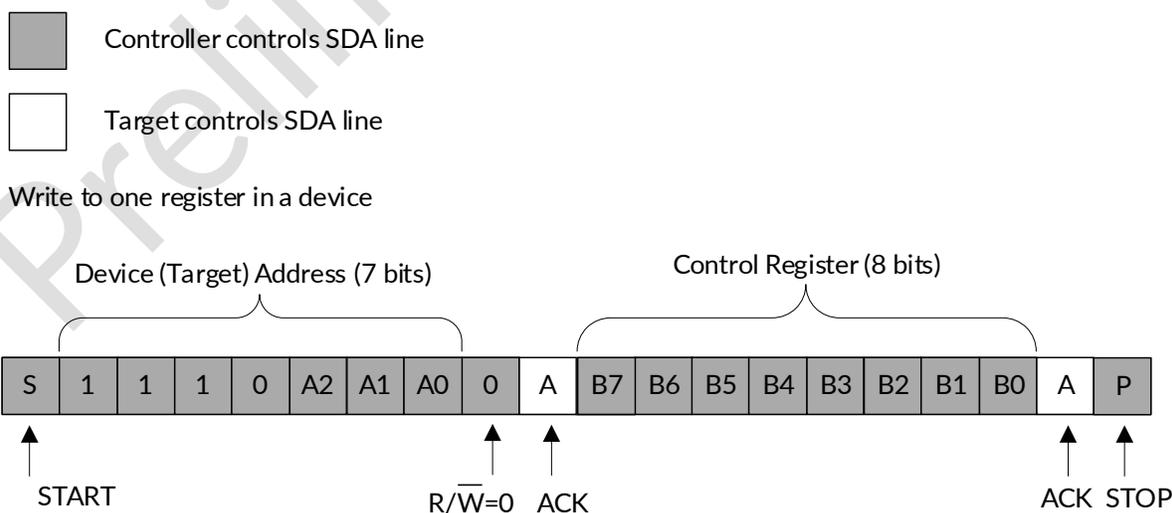


**Figure 11. Write to Register**

## 9.5.3.2 Reads

Reading from a target is very similar to writing, but the controller sends a START condition, followed by the target address with the R/$\overline{W}$ bit set to 1 (signifying a read). The target acknowledges the read request, and the controller releases the SDA bus but continues supplying the clock to the target. During this part of the transaction, the controller becomes the controller-receiver, and the target becomes the target-transmitter.

The controller continues to send out the clock pulses, but releases the SDA line so that the target can transmit data. At the end of every byte of data, the controller sends an ACK to the target, letting the target know that it is ready for more data. Once the controller has received the number of bytes it is expecting, it sends a NACK, signaling to the target to halt communications and release the bus. The controller follows this up with a STOP condition.

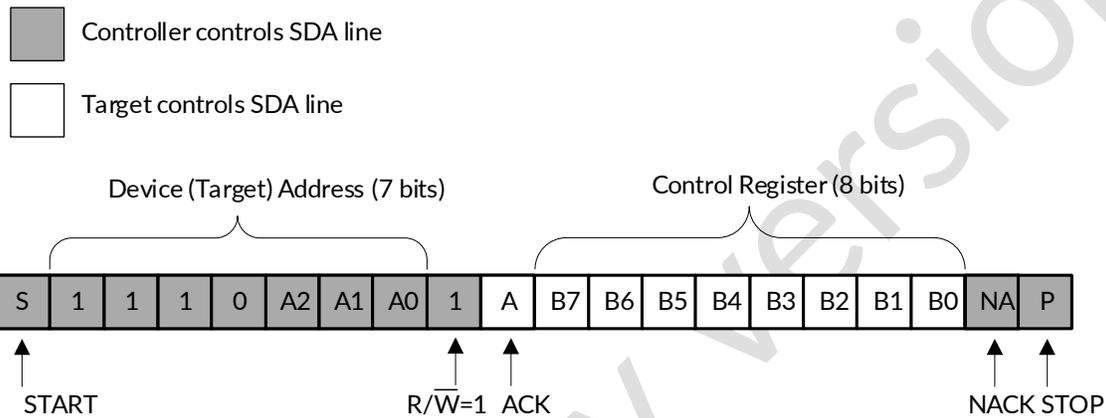Figure 12 shows an example of reading a single byte from a target register.



**Figure 12. Read from Control Register**

## 9.5.4 Control Register

Following the successful acknowledgment of the address byte, the bus controller sends a command byte that is stored in the control register in the RS29548 (see Figure 13). This register can be written and read via the I$^2$C bus. Each bit in the command byte corresponds to a SCn/SDn channel and a high (or 1) selects this channel. Multiple SCn/SDn channels may be selected at the same time. When a channel is selected, the channel becomes active after a stop condition has been placed on the I$^2$C bus. This makes sure that all SCn/SDn lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition always must occur immediately after the acknowledge cycle. If multiple bytes are received by the RS29548, it saves the last byte received.
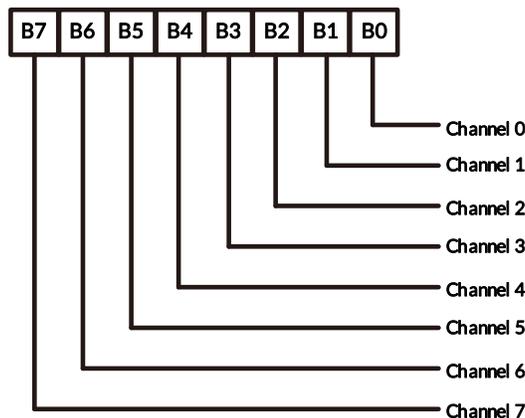


**Figure 13. Control Register**

Table 2 shows the RS29548 Command Byte Definition.

**Table 2. Command Byte Definition**

| CONTROL REGISTER BITS | | | | | | | | COMMAND |
|---|---|---|---|---|---|---|---|---|
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | |
| X | X | X | X | X | X | X | 0 | Channel 0 disabled |
| X | X | X | X | X | X | X | 1 | Channel 0 enabled |
| X | X | X | X | X | X | 0 | X | Channel 1 disabled |
| X | X | X | X | X | X | 1 | X | Channel 1 enabled |
| X | X | X | X | X | 0 | X | X | Channel 2 disabled |
| X | X | X | X | X | 1 | X | X | Channel 2 enabled |
| X | X | X | X | 0 | X | X | X | Channel 3 disabled |
| X | X | X | X | 1 | X | X | X | Channel 3 enabled |
| X | X | X | 0 | X | X | X | X | Channel 4 disabled |
| X | X | X | 1 | X | X | X | X | Channel 4 enabled |
| X | X | 0 | X | X | X | X | X | Channel 5 disabled |
| X | X | 1 | X | X | X | X | X | Channel 5 enabled |
| X | 0 | X | X | X | X | X | X | Channel 6 disabled |
| X | 1 | X | X | X | X | X | X | Channel 6 enabled |
| 0 | X | X | X | X | X | X | X | Channel 7 disabled |
| 1 | X | X | X | X | X | X | X | Channel 7 enabled |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | No channel selected, power-up/reset default state |

## 9.5.5 $\overline{\text{RESET}}$ Input

The $\overline{\text{RESET}}$ input is an active-low signal that may be used to recover from a bus-fault condition. When this signal is asserted low for a minimum of $t_{WL}$, the RS29548 resets its registers and I$^2$C state machine and deselects all channels. The $\overline{\text{RESET}}$ input must be connected to $V_{CC}$ through a pull-up resistor.

## 9.5.6 Power-On Reset

When power (from 0V) is applied to $V_{CC}$, an internal power-on reset holds the RS29548 in a reset condition until $V_{CC}$ has reached $V_{POR}$. At that point, the reset condition is released and the RS29548 registers and I$^2$C state machine initialize to their default states. After that, $V_{CC}$ must be lowered to below $V_{POR}$ and then back up to the operating voltage for a power-reset cycle.

# 10 APPLICATION AND IMPLEMENTATION

Information in the following applications sections is not part of the RUNIC component specification, and RUNIC does not warrant its accuracy or completeness. RUNIC's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

Applications of the RS29548 contain an $I^2C$ (or SMBus) controller device and up to eight $I^2C$ target devices. The downstream channels are used to resolve $I^2C$ target address conflicts. For example, if eight identical digital temperature sensors are needed in the application, one sensor can be connected at each channel: 0-7. When the temperature at a specific location is read, the appropriate channel can be enabled and all other channels switched off, the data can be retrieved, and the $I^2C$ controller can move on and read the next channel.

In an application where the $I^2C$ bus contains many additional target devices that do not result in $I^2C$ target address conflicts, these target devices can be connected to any desired channel to distribute the total bus capacitance across multiple channels. If multiple switches are enabled simultaneously, additional design requirements must be considered (see the Design Requirements section and Detailed Design Procedure section).

## 10.2 Typical Application

Figure 14 shows an application in which the RS29548 can be used.
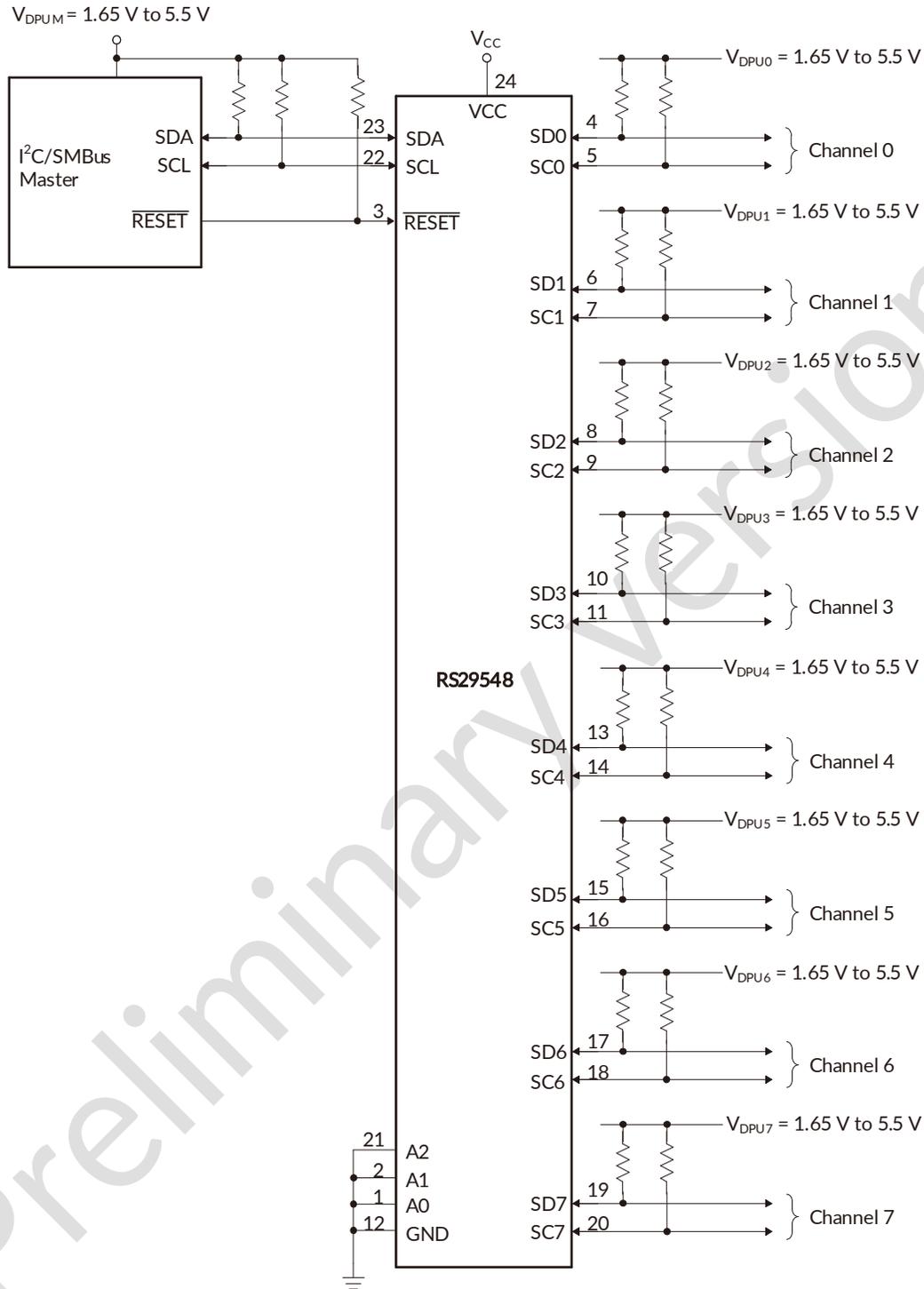
**Figure 14. Typical Application Schematic**

### 10.2.1 Design Requirements

A typical application of the RS29548 contains one or more data pull-up voltages, $V_{DPUX}$, one for the controller device ($V_{DPUM}$) and one for each of the selectable target channels ($V_{DPU0}$ – $V_{DPU7}$). In the event where the controller device and all target devices operate at the same voltage, then $V_{DPUM} = V_{DPUX} = V_{CC}$. In an application where voltage translation is necessary, additional design requirements must be considered to determine an appropriate $V_{CC}$ voltage.

The A0, A1, and A2 pins are hardware selectable to control the target address of the RS29548. These pins may be tied directly to GND or V$_{CC}$ in the application.

If multiple target channels are activated simultaneously in the application, then the total I$_{OL}$ from SCL/SDA to GND on the controller side is the sum of the currents through all pull-up resistors, R$_p$.

The pass-gate transistors of the RS29548 are constructed such that the V$_{CC}$ voltage can be used to limit the maximum voltage that is passed from one I$^2$C bus to another.

Figure 5 shows the voltage characteristics of the pass-gate transistors (note that the graph was generated using data specified in the Section 7.4 table). In order for the RS29548 to act as a voltage translator, the V$_{pass}$ voltage must be equal to or lower than the lowest bus voltage. For example, if the main bus is running at 5V and the downstream buses are 3.3V and 2.7V, V$_{pass}$ must be equal to or below 2.7V to effectively clamp the downstream bus voltages. As shown in Figure 5, V$_{pass(max)}$ is 2.7V when the RS29548 supply voltage is 4V or lower, so the RS29548 supply voltage could be set to 3.3V. Pull-up resistors then can be used to bring the bus voltages to their appropriate levels (see Figure 14).

## 10.2.2 Detailed Design Procedure

Once all the targets are assigned to the appropriate target channels and bus voltages are identified, the pull-up resistors, R$_p$, for each of the buses need to be selected appropriately. The minimum pull-up resistance is a function of V$_{DPUX}$, V$_{OL,(max)}$, and I$_{OL}$ as shown in Equation 1:

$$R_{p(min)} = \frac{V_{DPUX} - V_{OL(max)}}{I_{OL}} \qquad (1)$$

The maximum pull-up resistance is a function of the maximum rise time, t$_r$ (300ns for fast-mode operation, f$_{SCL}$ = 400kHz) and bus capacitance, C$_b$ as shown in Equation 2:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \qquad (2)$$

The maximum bus capacitance for an I$^2$C bus must not exceed 400 pF for fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the RS29548, C$_{io(OFF)}$, the capacitance of wires, connections and traces, and the capacitance of each individual target on a given channel. If multiple channels are activated simultaneously, each of the targets on all channels contribute to total bus capacitance.

## 10.3 Power Supply Recommendations

The operating power-supply voltage range of the RS29548 is 1.65V to 5.5V applied at the VCC pin. When the RS29548 is powered on for the first time or anytime, the device must be reset by cycling the power supply. The power-on reset requirements must be followed to make sure the I$^2$C bus logic is initialized properly.

## 10.3.1 Power-On Reset Requirements

In the event of a glitch or data corruption, RS29548 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

A power-on reset is shown in Figure 15.
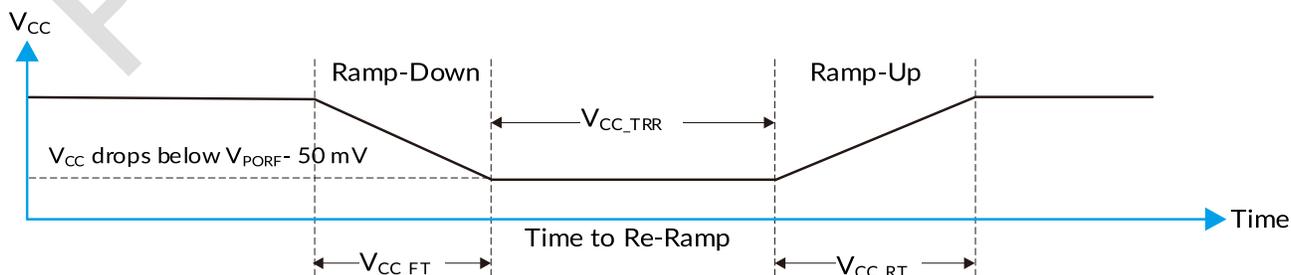


V$_{CC}$ is Lowered Below the POR Threshold, Then Ramped Back Up to V$_{CC}$

**Figure 15. Power-On Reset Waveform**

Table 3 specifies the performance of the power-on reset feature for RS29548 for both types of power-on reset.

**Table 3. Recommended Supply Sequencing and Ramp Rates [1]**

| PARAMETER | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC\_FT}$ | Fall time | See Figure 15 | 1 | 100 | ms |
| $V_{CC\_RT}$ | Rise time | See Figure 15 | 0.1 | 100 | ms |
| $V_{CC\_TRR}$ | Time to re-ramp (when $V_{CC}$ drops below $V_{PORF(min)}$ – 50mV or when $V_{CC}$ drops to GND) | See Figure 15 | 40 | | µs |
| $V_{CC\_GH}$ | Level that $V_{CC}$ can glitch down to, but not cause a functional disruption when $V_{CC\_GW}$ = 1µs | See Figure 16 | | 1.2 | V |
| $V_{CC\_GW}$ | Glitch width that does not cause a functional disruption when $V_{CC\_GH}$ = 0.5 × $V_{CC}$ | See Figure 16 | | 10 | µs |

(1) All supply sequencing and ramp rate values are measured at $T_A$ = 25°C.

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ($V_{CC\_GW}$) and height ($V_{CC\_GH}$) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 16 and Table 3 provide more information on how to measure these specifications.
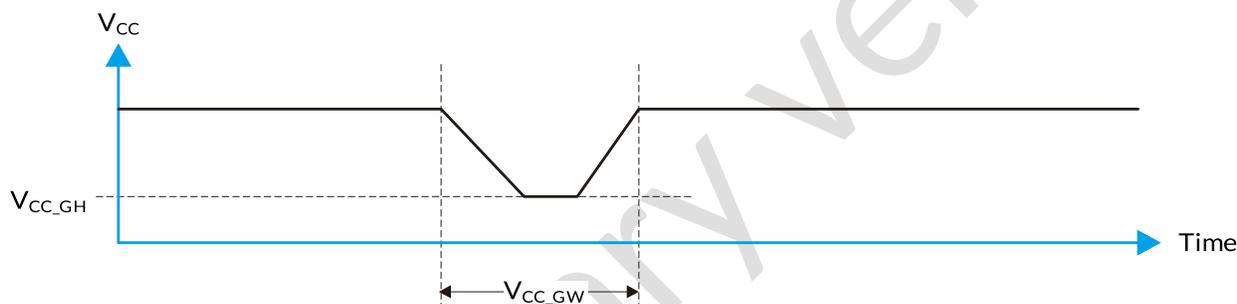


**Figure 16. Glitch Width and Glitch Height**

$V_{POR}$ is critical to the power-on reset. $V_{POR}$ is the voltage level at which the reset condition is released and all the registers and the I$^2$C/SMBus state machine are initialized to their default states. The value of $V_{POR}$ differs based on the $V_{CC}$ being lowered to or from 0. Figure 17 and Table 3 provide more details on this specification.
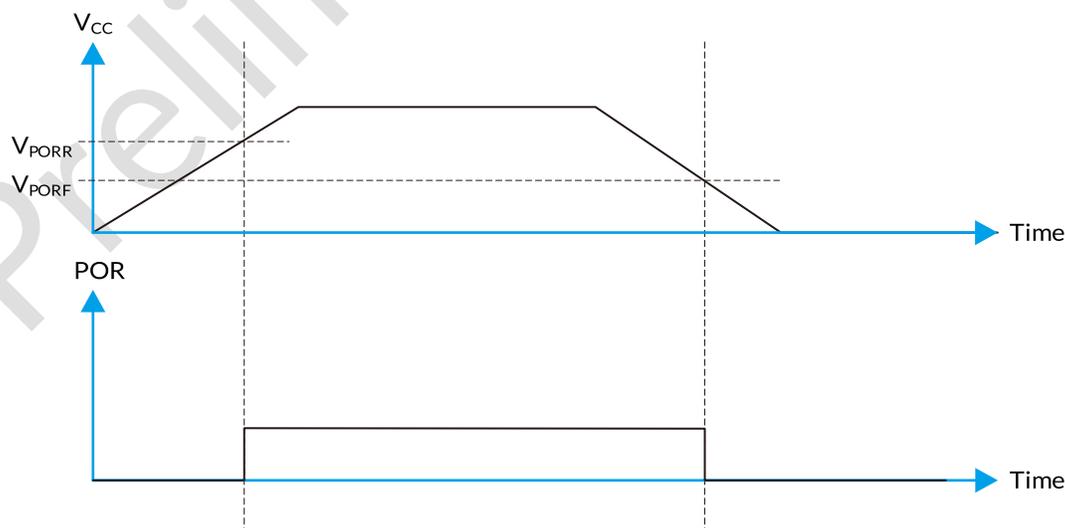


**Figure 17. $V_{POR}$**

# 11 LAYOUT

## 11.1 Layout Guidelines

For PCB layout of the RS29548, common PCB layout practices must be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for $I^2C$ signal speeds. It is common to have a dedicated ground plane on an inner layer of the board and pins that are connected to ground must have a low-impedance path to the ground plane in the form of wide polygon pours and multiple vias. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple.

In an application where voltage translation is not required, all $V_{DPUX}$ voltages and $V_{CC}$ could be at the same potential and a single copper plane could connect all of pull-up resistors to the appropriate reference voltage. In an application where voltage translation is required, $V_{DPUM}$ and $V_{DPU0}$ – $V_{DPU7}$, may all be on the same layer of the board with split planes to isolate different voltage potentials.

To reduce the total $I^2C$ bus capacitance added by PCB parasitics, data lines (SCn and SDn) must be a short as possible and the widths of the traces must also be minimized (for example, 5-10 mils depending on copper weight).
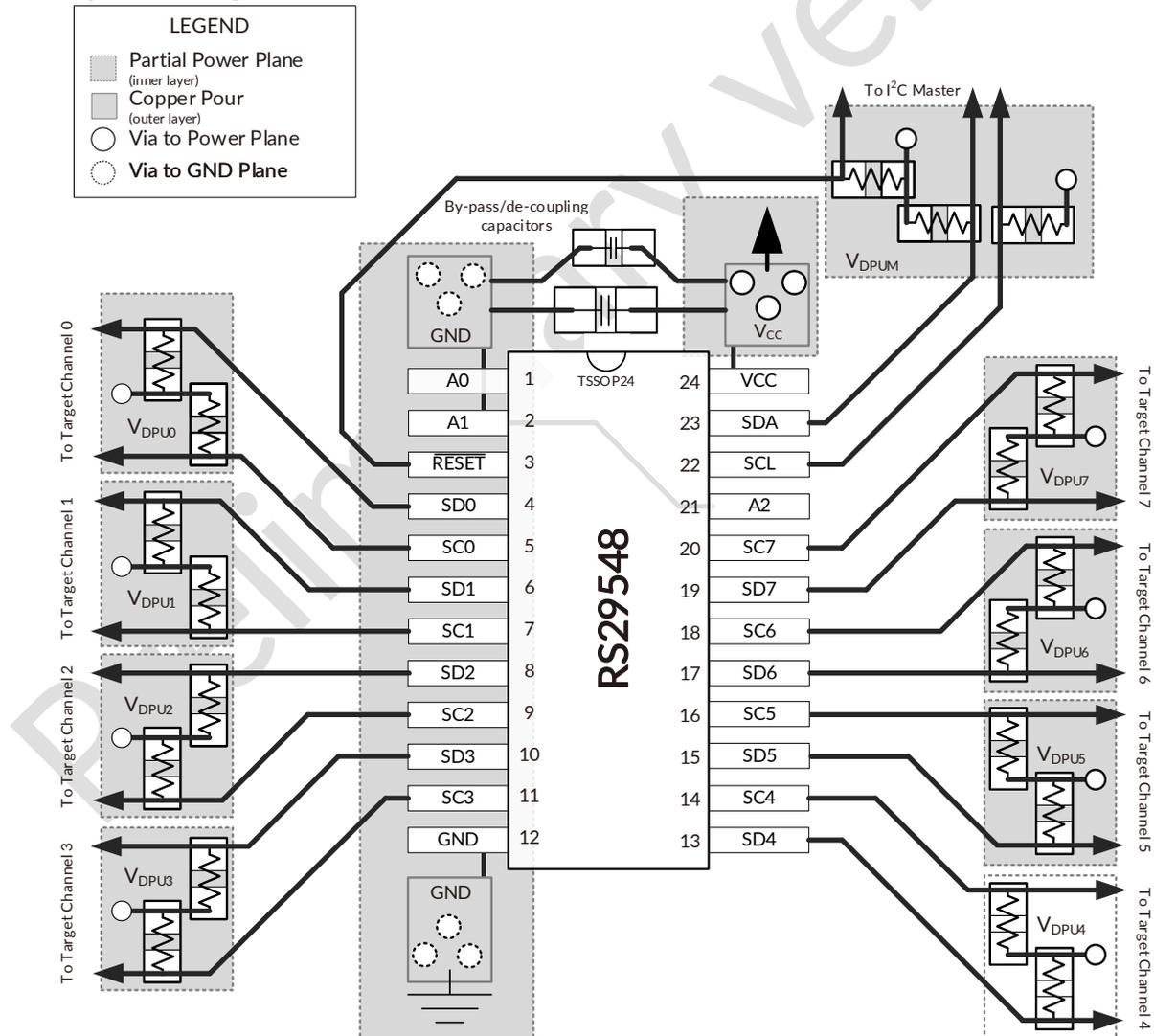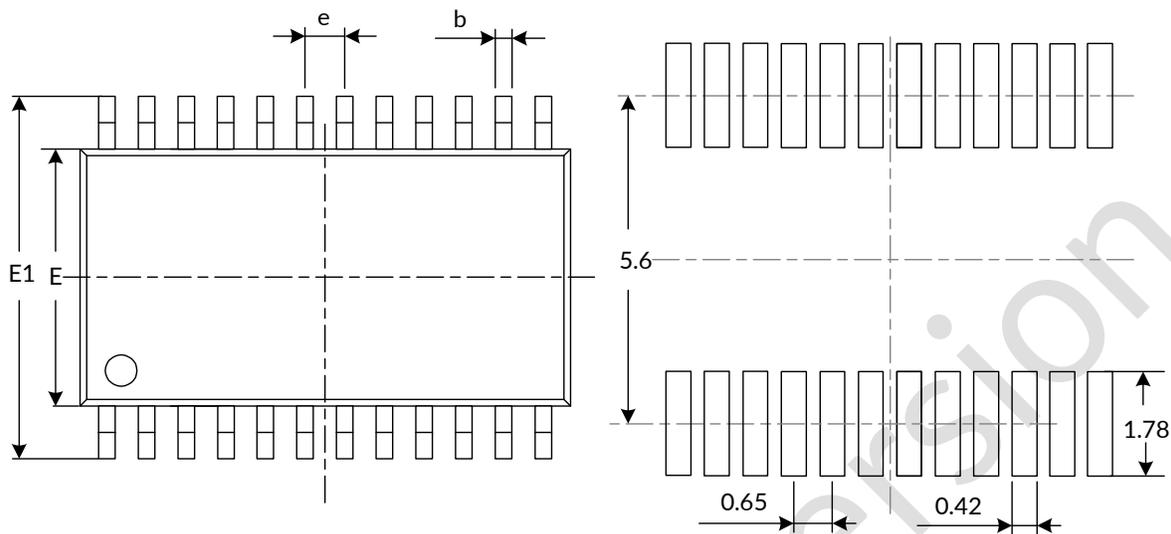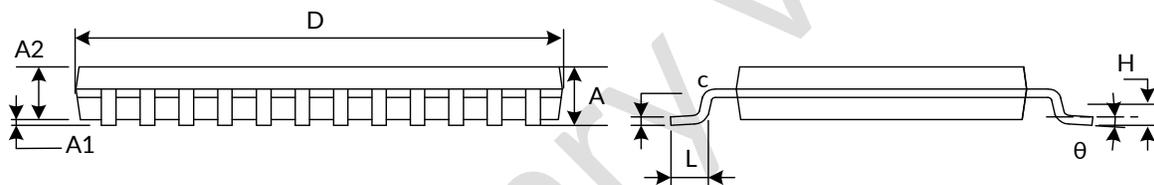
## 11.2 Layout Example



**Figure 18. Layout Schematic**

# 12 PACKAGE OUTLINE DIMENSIONS
## TSSOP24 [3]



RECOMMENDED LAND PATTERN (Unit: mm)



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A [1] | | 1.200 | | 0.047 |
| A1 | 0.050 | 0.150 | 0.002 | 0.006 |
| A2 | 0.800 | 1.050 | 0.031 | 0.041 |
| b | 0.200 | 0.290 | 0.008 | 0.011 |
| c | 0.130 | 0.170 | 0.005 | 0.007 |
| D [1] | 7.700 | 7.900 | 0.303 | 0.311 |
| E [1] | 4.300 | 4.500 | 0.169 | 0.177 |
| E1 | 6.200 | 6.600 | 0.244 | 0.260 |
| e | 0.650 (BSC) [2] | | 0.026 (BSC) [2] | |
| L | 0.450 | 0.750 | 0.018 | 0.030 |
| H | 0.250 (TYP) | | 0.010 (TYP) | |
| θ | 0° | 8° | 0° | 8° |

NOTE:
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

# 13 TAPE AND REEL INFORMATION
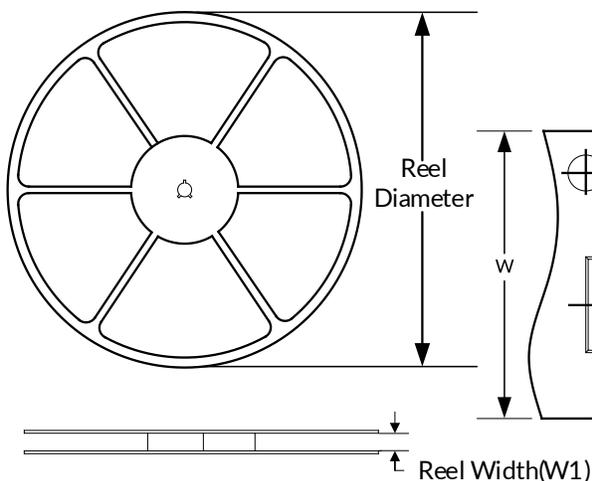
### REEL DIMENSIONS          ### TAPE DIMENSION
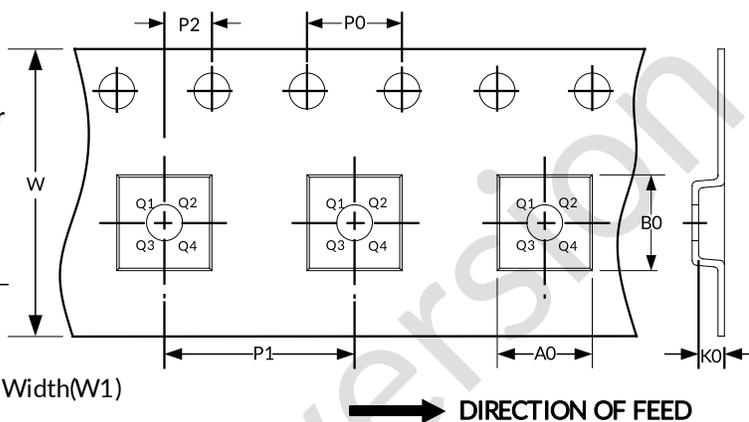


NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| TSSOP24 | 13" | 16.4 | 6.95 | 8.30 | 1.60 | 4.0 | 8.0 | 2.0 | 16.0 | Q1 |

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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