RS911xC 3.3-V and 2.5-V LVCMOS High-Performance Clock Buffer Family

1 FEATURES

- **High-Performance 1:2, 1:3, 1:4 LVCMOS Clock Buffer Family**
- **Supply Voltage: 3.3 V or 2.5 V**
- **f_{max} = 250 MHz for 3.3 V**
  f_{max} = 180 MHz for 2.5 V
- **Operating Temperature Range: –40°C to 125°C**
- **Available in TSSOP8 and DFN2X2-8 Packages**

2 APPLICATIONS

- **General-Purpose Communication, Industrial, and Consumer Applications**

3 DESCRIPTIONS

Three different fan-out variations, 1:2 to 1:4, are available. All of the devices are pin-compatible to each other for easy handling.

All family members share the same high performing characteristics such as low skew, and wide operating temperature range.

The RS911xC supports an asynchronous output enable control (1G) which switches the outputs into a low state when 1G is low.

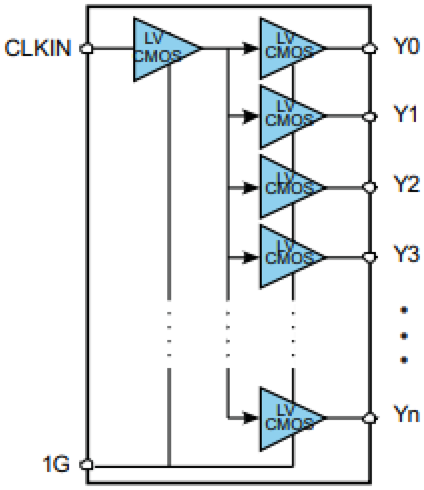
The RS911xC family operates in a 2.5-V and 3.3-V environment and are characterized for operation from –40°C to 125°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS9112C	TSSOP8	3.00 mm × 4.40 mm
RS9113C		
RS9114C		
RS9114C	DFN2X2-8	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 FUNCTIONAL BLOCK DIAGRAM



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5 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.1	2024/02/27	Initial version completed
A.2	2024/07/04	1. Added PACKAGE/ORDERING INFORMATION and TAPE AND REEL INFORMATION 2. Update PIN CONFIGURATION AND FUNCTIONS
A.3	2024/08/09	Update Recommended Operating Conditions
A.4	2025/05/16	Add $t_{sk(o)}$ PARAMETER
A.5	2025/06/26	Update $t_{sk(o)}$ PARAMETER
A.6	2025/07/10	Add $t_{sk(PP)}$ PARAMETER
A.7	2026/01/14	1. Add DFN2X2-8 package for RS9114C 2. Update T_A and t_r/ t_f PARAMETER

6 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE(°C)	PACKAGE LEAD	PACKAGE MARKING (2)	MSL (3)	PACKAGE OPTION
RS911xC	RS9112CYQ	-40°C ~125°C	TSSOP8	RS9112C	MSL3	Tape and Reel,4000
	RS9113CYQ	-40°C ~125°C	TSSOP8	RS9113C	MSL3	Tape and Reel,4000
	RS9114CYQ	-40°C ~125°C	TSSOP8	RS9114C	MSL3	Tape and Reel,4000
	RS9114CYTDE8	-40°C ~125°C	DFN2X2-8	9114C	MSL3	Tape and Reel,3000

NOTE:

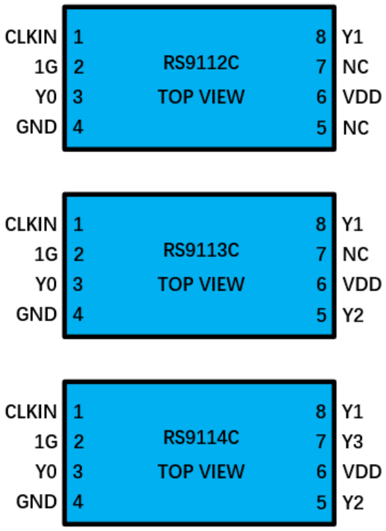
(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

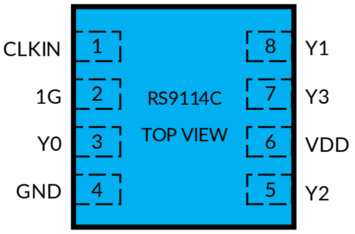
(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F, Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

7 PIN CONFIGURATION AND FUNCTIONS

Package TSSOP8 Top View



Package DFN2X2-8 Top View



Pin Functions

PIN				TYPE	DESCRIPTION
NAME	**RS9112C**	**RS9113C**	**RS9114C**		
LVCMOS CLOCK INPUT					
CLKIN	1	1	1	Input	Input Pin
CLOCK OUTPUT ENABLE					
1G	2	2	2	Input	Output Enable
LVCMOS CLOCK OUTPUT					
Y0	3	3	3	Output	LVCMOS output. Unused outputs can be left floating.
Y1	8	8	8		
Y2	—	5	5		
Y3	—	—	7		
SUPPLY VOLTAGE					
V_{DD}	6	6	6	Power	2.5-V or 3.3-Vdevice supply
GROUND					
GND	4	4	4	GND	Device ground

8 SPECIFICATIONS

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	-0.5	3.9	V
V_{IN}	Input voltage (2)	-0.5	V_{DD}+0.5	V
V_{O}	Output voltage (2)	-0.5	V_{DD}+0.5	V
I_{IN}	input current	-20	20	mA
I_{O}	Continuous output current	-50	50	mA
T_{J}	Maximum junction temperature		125	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) This value is limited to 3.9 V maximum.

8.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-Device Model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	3.3V supply	3	3.3	3.6	V
		2.5V supply	2.3	2.5	2.7	
V_{IL}	Low-level input voltage	V_{DD} = 2.3 V to 3.6 V			V_{DD}/2 – 600	mV
V_{IH}	High-level input voltage	V_{DD} = 2.3 V to 3.6 V	V_{DD}/2 + 600			mV
V_{TH}	Input threshold voltage	V_{DD} = 2.3 V to 3.6 V		V_{DD}/2		mV
t_r/ t_f	Input slew rate		1		4	V/ns
t_w	Minimum pulse width at CLKIN	V_{DD} = 3.0 V to 3.6 V	1.8			ns
		V_{DD} = 2.3 V to 2.7 V	2.75			
f_{CLK}	LVCMOS clock Input Frequency	V_{DD} = 3.0 V to 3.6 V	DC		250	MHz
		V_{DD} = 2.3 V to 2.7 V	DC		180	
T_{A}	Operating free-air temperature		-40		125	°C

8.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP [(1)]	MAX	UNIT
OVERALL PARAMETERS FOR ALL VERSIONS						
I_{DD}	Static device current	1G = V_{DD}; CLKIN = 0 V or V_{DD}; I_O = 0 mA; V_{DD} = 3.6 V		3.5	10	mA
		1G = V_{DD}; CLKIN = 0 V or V_{DD}; I_O = 0 mA; V_{DD} = 2.7 V		1.5	6	
I_{PD}	Power-down current	1G = 0 V; CLKIN = 0 V or V_{DD}; I_O = 0 mA; V_{DD} = 3.6 V or 2.7 V		34	60	µA
C_{PD}	Power dissipation capacitance per output[(2)]	V_{DD} = 3.3 V; f = 10 MHz		10.7		pF
		V_{DD} = 2.5 V; f = 10 MHz		7.4		
I_I	Input leakage current at 1G	V_I = 0 or V_{DD}, V_{DD} = 3.6 Vor2.7 V		10		µA
	Input leakage current at CLKIN	V_I = 0 or V_{DD}, V_{DD} = 3.6 V or 2.7 V		28		
R_{OUT}	Output impedance	VDD = 3.3 V		42		Ω
		VDD = 2.5 V		49		
f_{OUT}	Output frequency	VDD = 3 V to 3.6 V	DC		250	MHz
		VDD = 2.3 V to 2.7 V	DC		180	
OUTPUT PARAMETERS FOR V_{DD} = 3.3 V ± 0.3 V						
V_{OH}	High-level output voltage	V_{DD} = 3 V, I_{OH} = −0.1 mA	2.9			V
		V_{DD} = 3 V, I_{OH} = −8 mA	2.5			
		V_{DD} = 3 V, I_{OH} = −12 mA	2.2			
V_{OL}	Low-level output voltage	V_{DD} = 3 V, I_{OL} = 0.1 mA			0.1	V
		V_{DD} = 3 V, I_{OL} = 8 mA			0.5	
		V_{DD} = 3 V, I_{OL} = 12 mA			0.8	
OUTPUT PARAMETERS FOR V_{DD} =2.5 V ± 0.2 V						
V_{OH}	High-level output voltage	V_{DD} = 2.3 V, I_{OH} = −0.1 mA	2.2			V
		V_{DD} = 2.3 V, I_{OH} = −8 mA	1.7			
V_{OL}	Low-level output voltage	V_{DD} = 2.3 V, I_{OL} = 0.1 mA			0.1	V
		V_{DD} = 2.3 V, I_{OL} = 8 mA			0.5	

(1) All typical values are at respective nominal VDD. For switching characteristics, outputs are terminated to 50 Ω to $V_{DD}/2$ (see Figure 1).

(2) This is the formula for the power dissipation calculation (see and the Power Considerations section).

$P_{tot} = P_{stat} + P_{dyn} + P_{Cload}$ [W]

$P_{stat} = V_{DD} \times I_{DD}$ [W]

$P_{dyn} = C_{PD} \times V_{DD}^2 \times f$ [W]

$P_{Cload} = C_{load} \times V_{DD}^2 \times f \times n$ [W]

n = Number of switching output pins

8.5 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
OUTPUT PARAMETERS FOR V_{DD} = 3.3 V ± 0.3 V						
t_{PLH}/ t_{PHL}	Propagation delay	CLKIN toYn	0.8		2.0	ns
$t_{sk(o)}$	Output skew	Equal load of each output			50	ps
t_r/ t_f	Rise and fall time	20%–80% (V_{OH} - V_{OL})	0.3		0.8(3)	ns
					1.2	
t_{DIS}	Output disable time	1G to Yn			6	ns
t_{EN}	Output enable time	1G to Yn			6	ns
$t_{sk(p)}$	Pulse skew ; $t_{PLH(Yn)}$ – $t_{PHL(Yn)}$ (1)	To be measured with input duty cycle of 50%			180	ps
$t_{sk(pp)}$	Part-to-part skew	Under equal operating conditions for two parts			0.5	ns
t_{jitter}	Additive jitter rms(2)	12 kHz to 20 MHz, f_{OUT} = 250 MHz			100	fs
OUTPUT PARAMETERS FOR V_{DD} =2.5 V ± 0.2 V						
t_{PLH}/ t_{PHL}	Propagation delay	CLKIN to Yn	1		2.6	ns
$t_{sk(o)}$	Output skew	Equal load of each output			50	ps
t_r/ t_f	Rise and fall time	20%–80% (V_{OH} - V_{OL})	0.3		1.2(3)	ns
					1.4	
t_{DIS}	Output disable time	1G to Yn			10	ns
t_{EN}	Output enable time	1G to Yn			10	ns
$t_{sk(p)}$	Pulse skew ; $t_{PLH(Yn)}$ – $t_{PHL(Yn)}$ (1)	To be measured with input duty cycle of 50%			220	ps
$t_{sk(pp)}$	Part-to-part skew	Under equal operating conditions for two parts			1.2	ns
t_{jitter}	Additive jitter rms(2)	12 kHz to 20 MHz, f_{OUT} = 180 MHz			350	fs

(1) $t_{sk(p)}$ depends on output rise- and fall-time (t_r/t_f). The output duty-cycle can be calculated: odc = ($t_{w(OUT)}$ ± $t_{sk(p)}$)/t_{period}; $t_{w(OUT)}$ is pulse-width of output waveform and t_{period} is 1/f_{OUT}.

(2) Parameter is specified by characterization. Not tested in production.

(3) operating free-air temperature range: -40~85°C.

9 PARAMETER MEASUREMENT INFORMATION

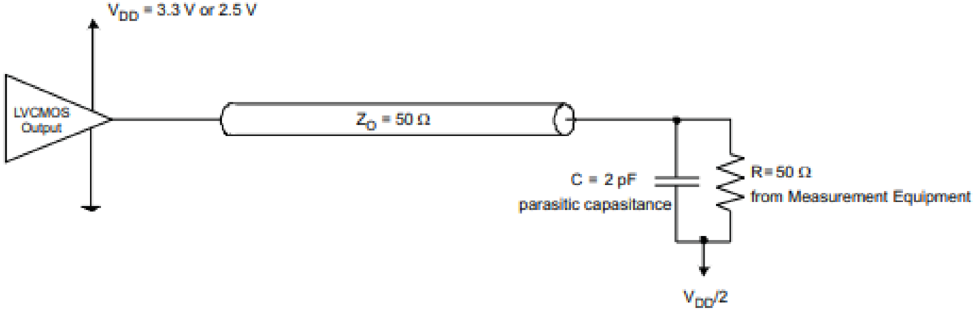


Figure 1. Test Load Circuit

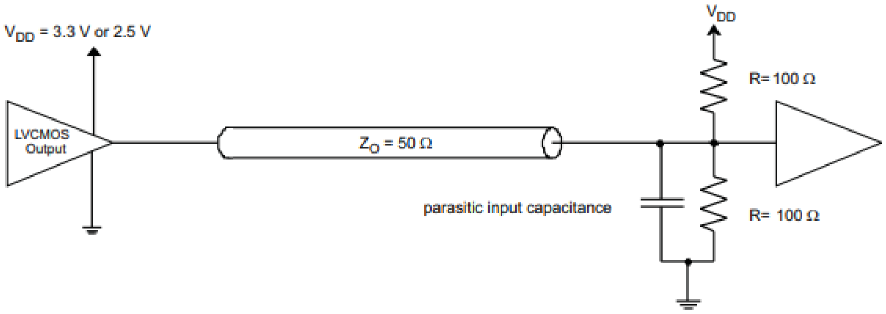


Figure 2. Application Load With 50-Ω Line Termination

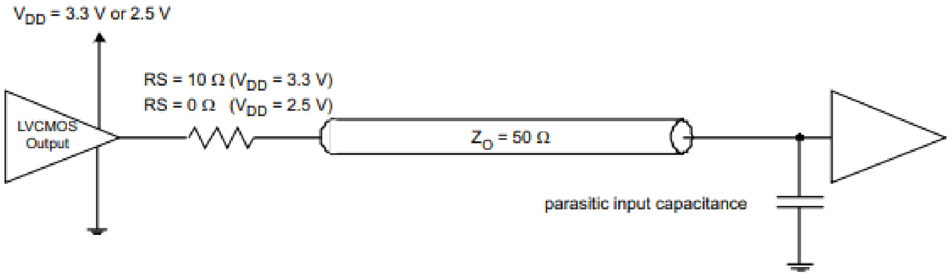


Figure 3. Application Load With Series Line Termination

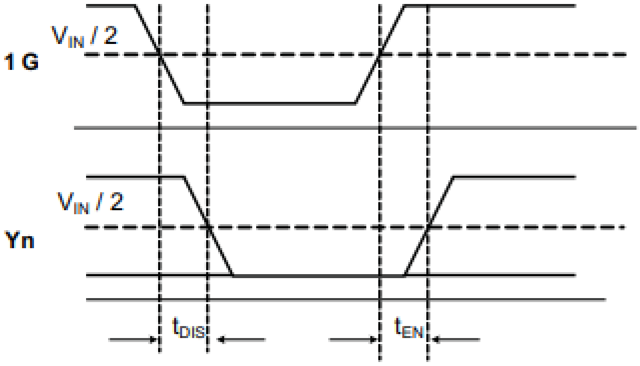


Figure 4. t_{DIS} and t_{EN} for Disable Low

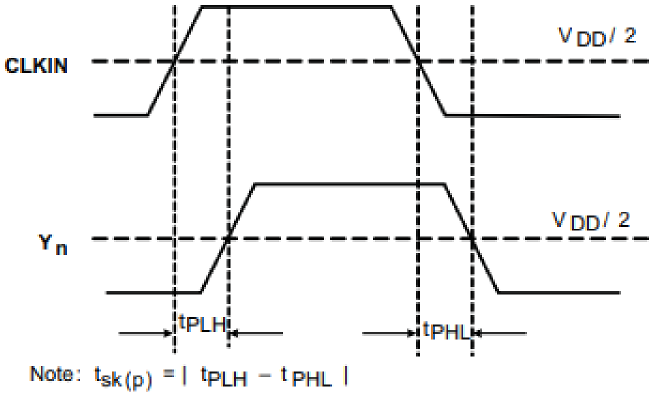


Figure 5. Pulse Skew tsk(p) and Propagation Delay t_{PLH}/t_{PHL}

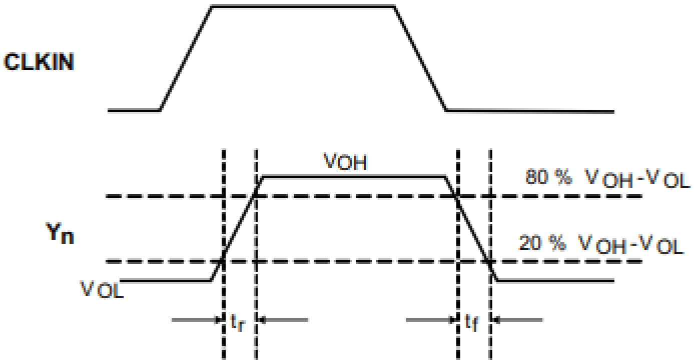


Figure 6. Rise/Fall Times t_r /t_f

10 DETAILED DESCRIPTION

10.1 Overview

The RS911xC family of devices is a low-jitter and low-skew LVCMOS fan-out buffer solution. For best signal integrity, it is important to match the characteristic impedance of the RS911xC 's output driver with that of the transmission line. Figure 2 and Figure 3 show the proper configuration per configuration for both V_{DD} = 3.3 V and V_{DD} = 2.5 V. RUNIC recommends placing the series resistor close to the driver to minimize signal reflection.

10.2 Functional Block Diagram

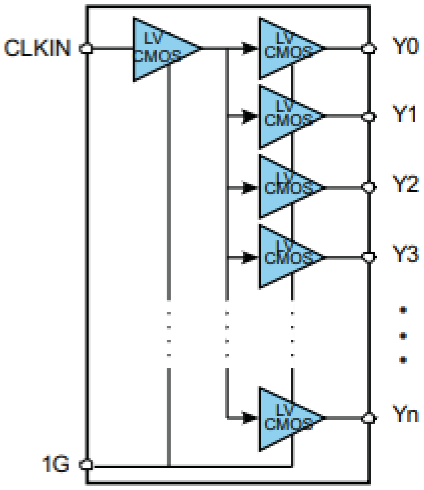


Figure 7. RS911xC functional block diagram

Table 1. Output Logic Table

INPUTS		OUTPUTS
CLKIN	**1G**	**Yn**
X	L	L
L	H	L
H	H	H

10.3 Feature Description

The outputs of the RS911xC can be disabled by driving the asynchronous output enable pin (1G) low. Unused output can be left floating to reduce overall system component cost. All supply and ground pins must be connected to V_{DD} and GND, respectively.

10.4 Device Functional Modes

The RS911xC operates from supplies between 2.5 V and 3.3 V.

11 APPLICATION AND IMPLEMENTATION

Information in the following applications sections is not part of the RUNIC component specification, and RUNIC does not warrant its accuracy or completeness. RUNIC's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The RS911xC family is a low additive jitter LVCMOS buffer solution that can operate up to 250 MHz at and 180 MHz at V_{DD} = 2.5 V. Low output skew as well as the ability for asynchronous output enable is featured to simultaneously enable or disable buffered clock outputs as necessary in the application.

11.2 Typical Application

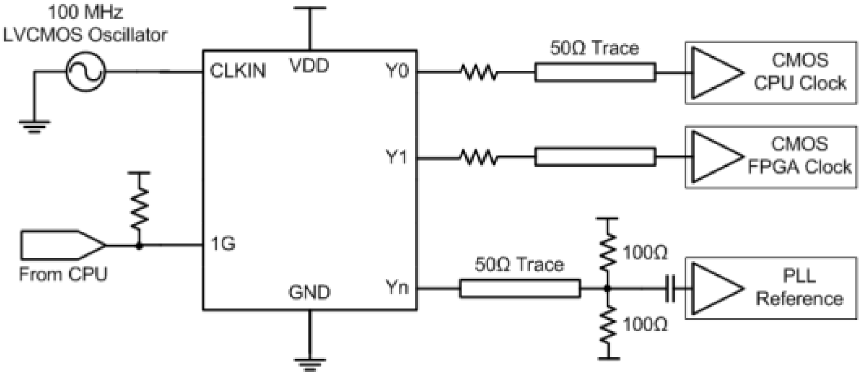


Figure 8. Example System Configuration

11.3 Design Requirements

The RS911xC shown in Figure 8 is configured to fan out a 100-MHz signal from a local LVCMOS oscillator. The CPU is configured to control the output state through 1G. The configuration example is driving three LVCMOS receivers in a backplane application with the following properties:

- The CPU clock can accept a full swing DC-coupled LVCMOS signal. A series resistor is placed near the RS911xC to closely match the characteristic impedance of the trace to minimize reflections.
- The FPGA clock is similarly DC-coupled with an appropriate series resistor placed near the RS911xC.
- The PLL in this example can accept a lower amplitude signal, so a Thevenin's equivalent termination is used. The PLL receiver features internal biasing, so AC coupling can be used when common-mode voltage is mismatched.

11.4 Detailed Design Procedure

Refer to Figure 3 and the Electrical Characteristics table to determine the appropriate series resistance needed for matching the output impedance of the RS911xC to that of the characteristic impedance of the transmission line.

Unused outputs can be left floating. See the Power Supply Recommendations section for recommended filtering techniques.

12 POWER SUPPLY RECOMMENDATIONS

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when the jitter and phase noise is critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guards the power supply system against induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed very close to the power-supply terminals and laid out with short loops to minimize inductance. RUNIC recommends adding as many high-frequency (for example, 0.1 µF) bypass capacitors, as there are supply terminals in the package. RUNIC recommends, but does not require, inserting a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock buffer; these beads prevent the switching noise from leaking into the board supply. It is imperative to choose an appropriate ferrite bead with very low DC resistance to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

Figure 9 shows this recommended power supply decoupling method.

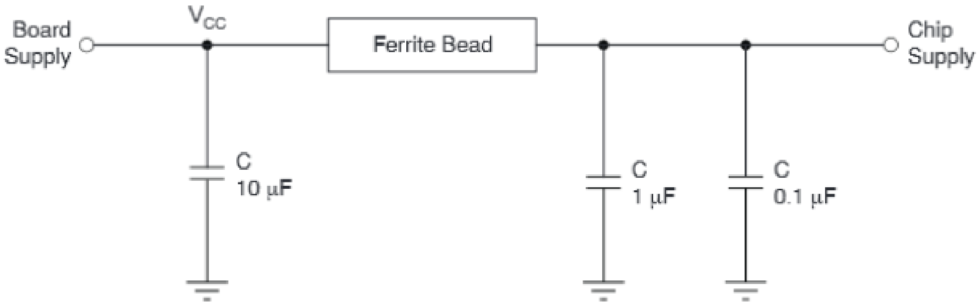


Figure 9. Power Supply Decoupling

12.1 Power Considerations

The following power consideration refers to the device-consumed power consumption only. The device power consumption is the sum of static power and dynamic power. The dynamic power usage consists of two components:

- Power used by the device as it switches states.
- Power required to charge any output load.

The output load can be capacitive only or capacitive and resistive. The following formula and the power graphs in and Figure 1 can be used to obtain the power consumption of the device:

$P_{dev} = P_{stat} + n\ (P_{dyn} + P_{Cload})$

$P_{stat} = V_{DD} \times I_{DD}\ P_{dyn} + P_{Cload}$

where:

V_{DD} = Supply voltage (3.3Vor 2.5 V)

I_{DD} = Static device current (typical 3.5 mA for V_{DD} = 3.3 V; typical 1.5 mA for V_{DD} = 2.5 V)

n = Number of switching output pins

Example for device power consumption for RS9114C: four outputs are switching, f = 120 MHz, V_{DD} = 3.3 V, and C_{load} = 2 pF per output:

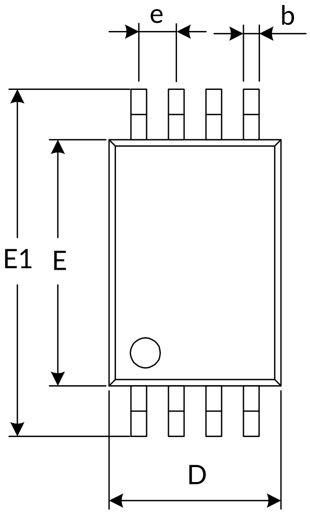
$P_{dev} = P_{stat} + n\ (P_{dyn} + P_{Cload}) = 11.55\text{ mW} + 50\text{ mW} = 61.55\text{ mW}$

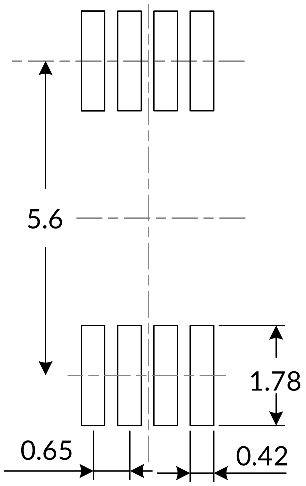
$P_{stat} = V_{DD} \times I_{DD} = 3.5\text{ mA} \times 3.3\text{ V} = 11.55\text{ mW}$

$n\ (P_{dyn} + P_{Cload}) = 4 \times 12.5\text{ mW} = 50\text{ mW}$

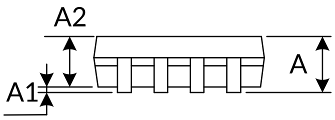
13 PACKAGE OUTLINE DIMENSIONS

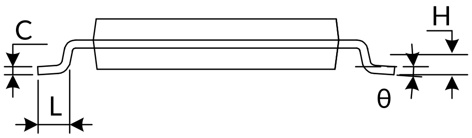
TSSOP8 (3)





RECOMMENDED LAND PATTERN (Unit: mm)



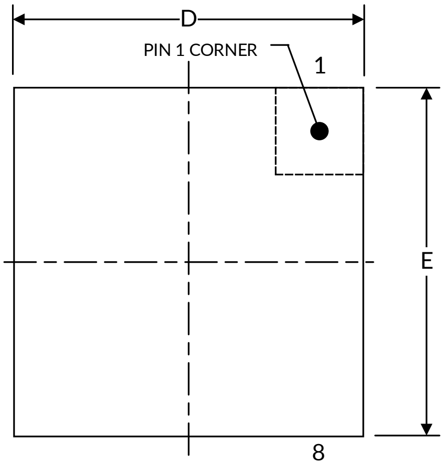


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D (1)	2.900	3.100	0.114	0.122
E (1)	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650(BSC) (2)		0.026(BSC) (2)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

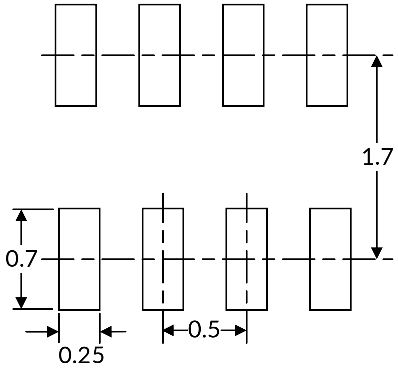
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

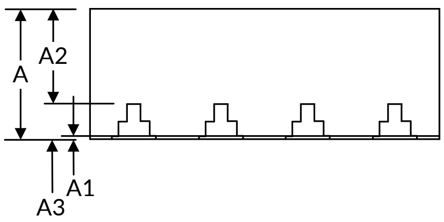
DFN2X2-8 (4)



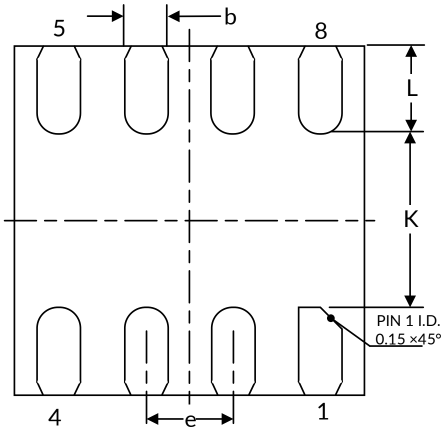
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.550 NOM		0.022 NOM	
A3	0.203 REF (2)		0.008 REF (2)	
b	0.200	0.300	0.008	0.012
D (1)	2.000 BSC (3)		0.079 BSC (3)	
E (1)	2.000 BSC (3)		0.079 BSC (3)	
e	0.500 BSC (3)		0.020 BSC (3)	
L	0.450	0.550	0.018	0.022
K	1.000 REF (2)		0.039 REF (2)	

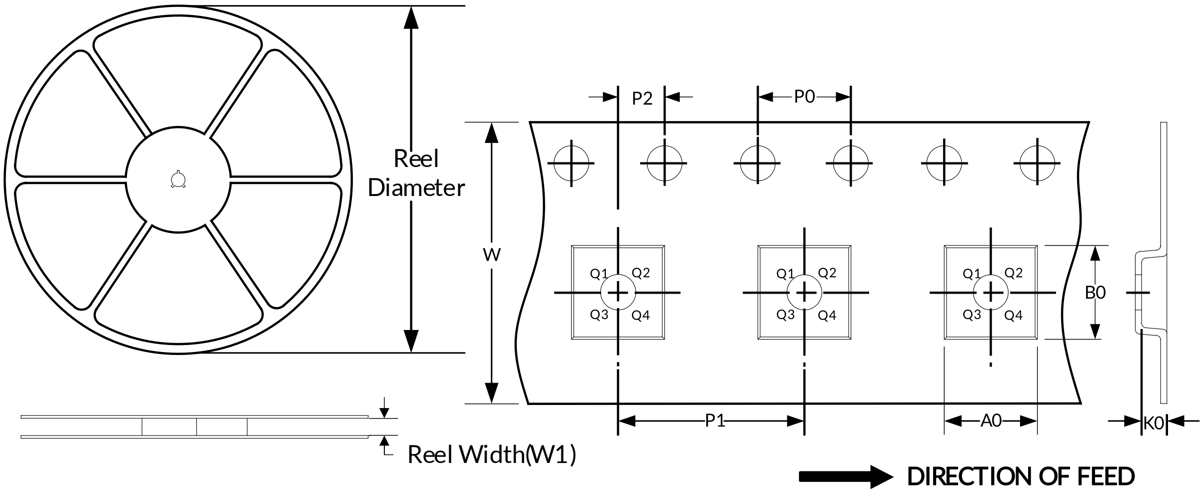
NOTE:

1. Plastic or metal protrusions of 0.075mm maximum per side are not included.
2. REF is the abbreviation for Reference.
3. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
4. This drawing is subject to change without notice.

14 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP8	13”	12.4	6.90	3.45	1.65	4.0	8.0	2.0	12.0	Q1
DFN2X2-8	7”	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q2

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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