Dual, 16Bit, 1MSPS, Simultaneous-Sampling, Analog-to-Digital Converters

1 FEATURES

- **Simultaneous Sampling of Two Channels**
- **Supports Fully-Differential Inputs**
- **Throughput: 1MSPS**
- **Excellent DC Performance:**
  - **16Bit NMC DNL, ±1.7 LSB TYP INL**
- **Excellent AC Performance:**
  - **92.5 dB SNR, –98 dB THD**
- **Dual, Programmable, and Buffered 2.5 V Internal Reference**
- **Fully-Specified Over the Extended Industrial Temperature Range: –40°C to 125°C**

2 APPLICATIONS

- **Motor Control:**
  Position Measurement Using Encoders
- **Optical Networking: EDFA Gain Control Loops**
- **Protection Relays**
- **Power Quality Measurement**
- **Three-Phase Power Controls**
- **Programmable Logic Controllers**

3 DESCRIPTIONS

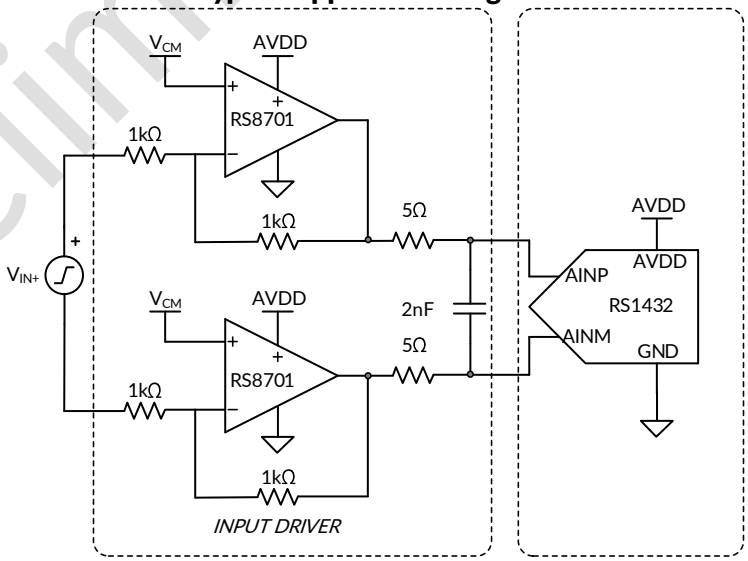
The RS1432 is a 16Bit, dual, high-speed, simultaneous-sampling, analog-to-digital converters (ADCs) that supports fully-differential Inputs. This device includes two individually programmable reference sources that can be used for system-level gain calibration. Also, it features a flexible serial interface that facilitates easy communication with a large variety of host controllers. Power consumption for a given throughput can be optimized by using the two low-power modes supported by the device. The device is fully specified over the extended industrial temperature range (–40°C to 125°C) and is available in a TSSOP16 package.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS1432	TSSOP16	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Diagram



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4 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

Version	Change Date	Change Item
A.0	2025/12/04	Preliminary version completed

5 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING (2)	MSL(3)	PACKAGE OPTION
RS1432	RS1432XTSS16	-40°C ~+125°C	TSSOP16	RS1432	MSL1	Tape and Reel, 4000

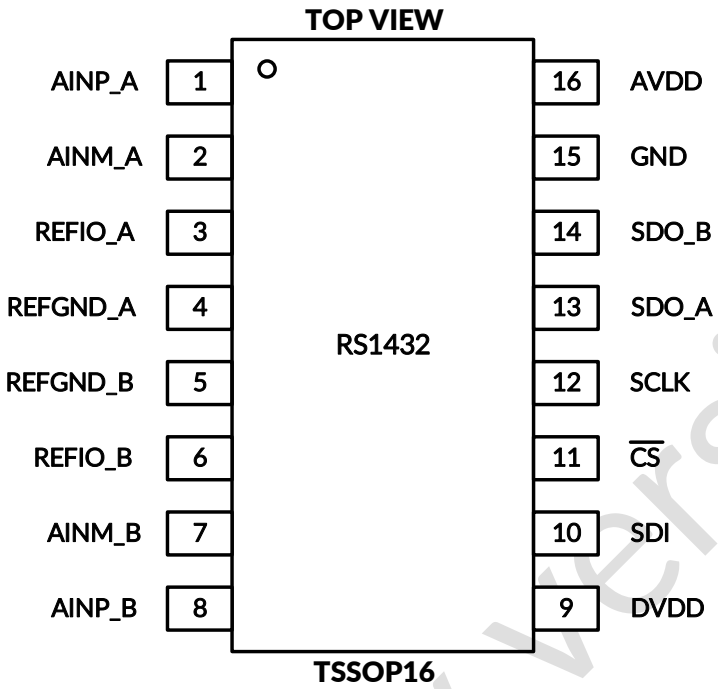
NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

6 PIN CONFIGURATION AND FUNCTIONS



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
	TSSOP16		
AINP_A	1	Analog input	Positive analog input, channel A
AINM_A	2	Analog input	Negative analog input, channel A
REFIO_A	3	Analog input/output	Reference voltage input/output, channel A
REFGND_A	4	Supply	Reference ground potential A
REFGND_B	5	Supply	Reference ground potential B
REFIO_B	6	Analog input/output	Reference voltage input/output, channel B
AINM_B	7	Analog input	Negative analog input, channel B
AINP_B	8	Analog input	Positive analog input, channel B
DVDD	9	Digital I/O supply	Digital I/O supply
SDI	10	Digital input	Data input for serial communication
$\overline{CS}$	11	Digital input	Chip-select signal; active low
SCLK	12	Digital input	Clock for serial communication
SDO_A	13	Digital output	Data output for serial communication, channel A and channel B
SDO_B	14	Digital output	Data output for serial communication, channel B
GND	15	Supply	Digital ground
AVDD	16	Supply	Supply voltage for ADC operation

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
AVDD to GND		–0.3	6	V
DVDD to GND		-0.3	AVDD + 0.3	V
Analog (AINP_x and AINM_x) voltage with respect to GND		GND – 0.3	AVDD + 0.3	V
Digital input voltage with respect to GND		GND – 0.3	DVDD + 0.3	V
Ground voltage difference |REFGND_x-GND|			0.3	V
Input current to any pin except supply pins			±10	mA
Package thermal impedance, θ_{JA} (2)	TSSOP16		135	°C/W
Maximum virtual junction temperature, T_J (3)			150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The package thermal impedance is calculated in accordance with JESD-51.

(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-Body Model (HBM), EIA/JESD22-a114	±2000	V
	Charged-Device Model (CDM), ANSI/ESDA/JEDEC JS-002-2022	±500	V

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog supply voltage		5		V
DVDD	Digital supply voltage		3.3		V

7.4 Electrical Characteristics

All minimum and maximum specifications are at T_A = –40°C to 125°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF_A} = V_{REF_B} = V_{REF} = 2.5 V (internal), and f_{DATA} = 1MSPS, 16-clock mode, unless otherwise noted.
Typical values are at T_A = 25°C, AVDD = 5 V, and DVDD = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION						
	Resolution		16			Bits
DC ACCURACY (1)						
NMC	No missing codes	16-clock mode	16			Bits
INL	Integral nonlinearity	16-clock mode		±1.7		LSB
DNL	Differential nonlinearity	16-clock mode		±0.7		LSB
E_{IO}	Input offset error			±0.5		mV
	E_{IO} match	ADC_A to ADC_B		±0.5		mV
dE_{IO}/dT	Input offset thermal drift			1		µV/°C
E_G	Gain error	Referenced to the voltage at REFIO_x		±0.01		%FS
	E_G match	ADC_A to ADC_B		±0.01		%FS
dE_G/dT	Gain error thermal drift	Referenced to the voltage at REFIO_x		1		ppm/°C
CMRR	Common-mode rejection ratio	Both ADCs, dc to 20 kHz		85		dB
AC ACCURACY (2)						
SINAD	Signal-to-noise + distortion	V_{REF} = 2.5 V, V_{REF} input range, 16-clock mode		89		dB
		V_{REF} = 2.5 V, 2 × V_{REF} input range, 16-clock mode		90		dB
		V_{REF} = 5 V (external), 16-clock mode, V_{REF} input range(external)		92		dB
SNR	Signal-to-noise ratio	V_{REF} = 2.5 V, V_{REF} input range, 16-clock mode		90		dB
		V_{REF} = 2.5 V, 2 × V_{REF} input range, 16-clock mode		91		dB
		V_{REF} = 5 V (external), 16-clock mode, V_{REF} input range(external)		92.5		dB
THD	Total harmonic distortion	V_{REF} = 2.5 V, V_{REF} input range, 16-clock mode		-98		dB
		V_{REF} = 2.5 V, 2 × V_{REF} input range, 16-clock mode		-97		dB
		V_{REF} = 5 V (external), 16-clock mode, V_{REF} input range(external)		-98		dB
SFDR	Spurious-free dynamic range	V_{REF} = 2.5 V, V_{REF} input range, 16-clock mode		100		dB
		V_{REF} = 2.5 V, 2 × V_{REF} input range, 16-clock mode		100		dB
		V_{REF} = 5 V (external), 16-clock mode, V_{REF} input range(external)		100		dB
ISOXT	ADC-to-ADC isolation	f_{IN}=2kHz, DC=V_{REF}/2		-120		dB

(1) LSB = least significant bit.
(2) All ac parameters are tested at –0.5 dBFS and a 2 kHz input frequency.

Electrical Characteristics (continued)

All minimum and maximum specifications are at T_A = –40°C to 125°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF_A} = V_{REF_B} = V_{REF} = 2.5 V (internal), and f_{DATA} = 1MSPS, 16-clock mode, unless otherwise noted.
Typical values are at T_A = 25°C, AVDD = 5 V, and DVDD = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
FSR	Full-scale input range (3) (AINP_x – AINM_x)	V_{REF} range	$-V_{REF}$		V_{REF}	V
		2 × V_{REF} range, AVDD ≥ 2 × V_{REF}	$-2 \times V_{REF}$		2 × V_{REF}	V
V_{IN}	Absolute input voltage (AINP_x and AINM_x to GND)	V_{REF} range	0		V_{REF}	V
		2 × V_{REF} range, AVDD ≥ 2 × V_{REF}	0		2 × V_{REF}	V
V_{CM}	Common-mode voltage range (AINP_x + AINM_x) / 2	V_{REF} range	(V_{REF} / 2) – 0.1	V_{REF} / 2	(V_{REF} / 2) + 0.1	V
		2 × V_{REF} range	V_{REF} – 0.1	V_{REF}	V_{REF} + 0.1	V
C_i	Input capacitance	In sample mode		40		pF
		In hold mode		4		pF
$I_{lkg(i)}$	Input leakage current			±0.1		µA
INTERNAL VOLTAGE REFERENCE						
V_{REFOUT}	Reference output voltage	REFDAC_x = 1FFh, at 25°C		2.5		V
$V_{REF\text{-}match}$	V_{REF_A} to V_{REF_B} matching	REFDAC_x = 1FFh, at 25°C		1.8		mV
	REFDAC_x resolution (4)			1.22		mV
dV_{REFOUT}/dT	Reference voltage temperature drift	REFDAC_x = 1FFh		5		ppm/°C
dV_{REFOUT}/dt	Long-term stability	1000 hours		250		ppm
R_O	Internal reference output impedance			1		Ω
I_{REFOUT}	Reference output dc current			2		mA
C_{REFOUT}	Recommended output capacitor			10		µF
t_{REFON}	Reference output settling time	For C_{REF} = 10 µF		8		ms

(3) Ideal input span, does not include gain or offset error.
(4) Refer to the Reference section for more details.

Electrical Characteristics (continued)

All minimum and maximum specifications are at T_A = –40°C to 125°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF_A} = V_{REF_B} = V_{REF} = 2.5 V (internal), and f_{DATA} = 1MSPS, 16-clock mode, unless otherwise noted.
Typical values are at T_A = 25°C, AVDD = 5 V, and DVDD = 3.3 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VOLTAGE REFERENCE INPUT							
V_{REF}	Reference voltage (input)	V_{REF} range		2.4		AVDD	V
		2 × V_{REF} range		2.4		AVDD / 2	V
I_{REF}	Average Reference input current	Per ADC			500		µA
C_{REF}	External ceramic reference capacitance				10		µF
$I_{lkg(dc)}$	DC leakage current				±0.1		µA
SAMPLING DYNAMICS							
t_A	Aperture delay				10		ns
	t_A match	ADC_A to ADC_B			50		ps
t_{AJIT}	Aperture jitter				50		ps
DIGITAL INPUTS (5)							
V_{IH}	High-level input voltage	DVDD > 2.3 V		0.7 DVDD			V
		DVDD ≤ 2.3 V		0.8 DVDD			V
V_{IL}	Low-level input voltage	DVDD > 2.3 V				0.3 DVDD	V
		DVDD ≤ 2.3 V				0.2 DVDD	V
	Input current				±10		nA
DIGITAL OUTPUTS (5)							
V_{OH}	High-level output voltage	I_{OH} = 500µA source		0.8 DVDD		DVDD	V
V_{OL}	Low-level output voltage	I_{OH} = 500µA sink		0		0.2 DVDD	V
POWER SUPPLY							
AVDD	Analog supply voltage (AVDD to GND)	±V_{REF} range	Internal reference	4.5	5	5.5	V
			External reference: V_{EXT_REF} < 4.5 V	4.5	5	5.5	V
			External reference: V_{EXT_REF} > 4.5 V	V_{EXT_REF}	5	5.5	V
		±2 × V_{REF} range	Internal reference	5	5	5.5	V
			External reference	2 × V_{REF_EXT}	5	5.5	V
DVDD	Digital supply voltage (DVDD to GND)			1.62		5.5	V

(5) Specified by design; not production tested.

Electrical Characteristics (continued)

All minimum and maximum specifications are at T_A = –40°C to 125°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF_A} = V_{REF_B} = V_{REF} = 2.5 V (internal), and f_{DATA} = 1MSPS, 16-clock mode, unless otherwise noted.
Typical values are at T_A = 25°C, AVDD = 5 V, and DVDD = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AIDD	Analog supply current	AVDD = 5 V, fastest throughput internal reference		10		mA
		AVDD = 5 V, fastest throughput external reference (6)		8.5		mA
		AVDD = 5 V, no conversion, internal reference		7		mA
		AVDD = 5 V, no conversion, external reference (6)		5.5		mA
		AVDD = 5 V, STANDBY mode, Internal Reference		2		mA
		AVDD = 5 V, STANDBY mode, external reference (6)		0.5		mA
		Power-down mode		3		µA
DIDD	Digital supply current	DVDD = 3.3 V, C_{LOAD} = 20 pF, fastest throughput		1.5		mA
		DVDD = 5 V, C_{LOAD} = 20 pF, fastest throughput		2		mA
P_D	Power dissipation (normal operation)	AVDD = 5 V, fastest throughput internal reference		50		mW

(6) With internal reference powered down, CFR.B6 = 0.

7.5 Timing Requirements: Interface Mode (1)

PARAMETER		ASSOCIATED FIGURES
t_{CLK}	CLOCK period	Figure 1, Figure 30, Figure 31, Figure 32, Figure 33
t_{ACQ}	Acquisition time	Figure 30, Figure 31, Figure 32, Figure 33
t_{CONV}	Conversion time	Figure 30, Figure 31, Figure 32, Figure 33

(1) These parameters are specific to the interface mode of operation. Refer to the Conversion Data Read section for more details.

7.6 Timing Characteristics: Serial Interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIMING REQUIREMENTS						
t_{PH_CK}	CLOCK high time		0.4		0.6	t_{CLK}
t_{PL_CK}	CLOCK low time		0.4		0.6	t_{CLK}
f_{CLK}	CLOCK frequency				$1/t_{CLK}$	MHz
t_{PH_CS}	$\overline{CS}$ high time		20	40		ns
t_{ACQ}	Acquisition time			$CLK_{CNT} \times t_{CLK} - t_{CONV}$		ns
t_{CONV}	Conversion time				640	ns
t_{SU_CSCK}	Setup time: $\overline{CS}$ falling edge to SCLK falling edge		15			ns
t_{D_CKCS}	Delay time: Last SCLK falling edge to $\overline{CS}$ rising edge		15			ns
t_{SU_CKDI}	Setup time: DIN data valid to SCLK falling edge		5			ns
t_{HT_CKDI}	Hold time: SCLK falling edge to (previous) data valid on DIN		5			ns
t_{PU_STDBY}			1			µs
t_{PU_SPD}	Power-up time from SPD mode	With internal reference	2			ms
	Power-up time from STANDBY mode	With external reference	1			µs
TIMING SPECIFICATIONS						
$t_{THROUGHPUT}$	Throughput time		1			µs
$f_{THROUGHPUT}$	Throughput				$1 / t_{THROUGHPUT}$	kSPS
t_{DV_CSDO}	Delay time: $\overline{CS}$ falling edge to data enable				20	ns
t_{DZ_CSDO}	Delay time: $\overline{CS}$ rising edge to data going to 3-state				15	ns
t_{D_CKDO}	Delay time: SCLK falling edge to next data valid				15	ns

Figure 1 shows the details of the serial interface between the device and the digital host controller.

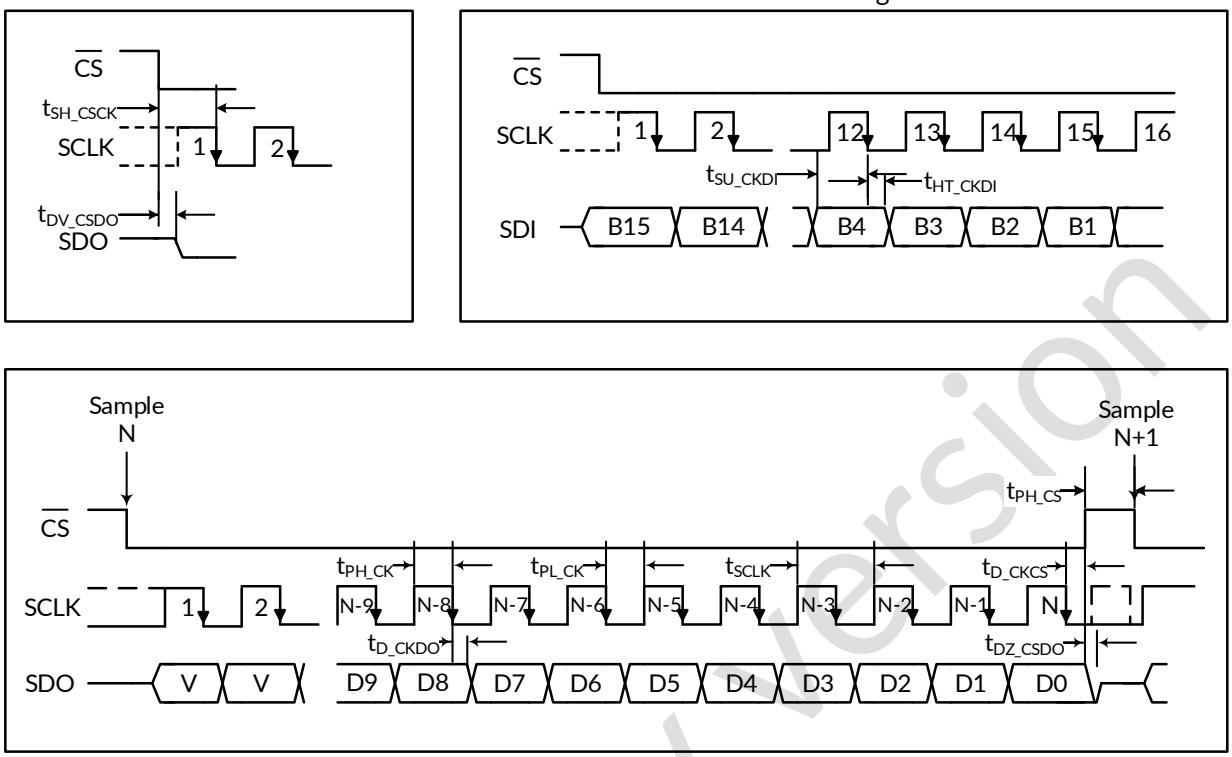


Figure 1. Serial Interface Timing Diagram

7.7 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.
At T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V (internal), and f_{DATA} = 1MSPS, 16-clock mode, unless otherwise noted.

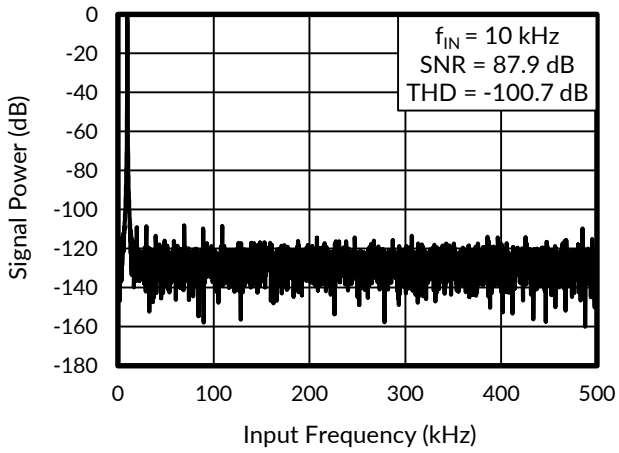


Figure 2. Typical FFT

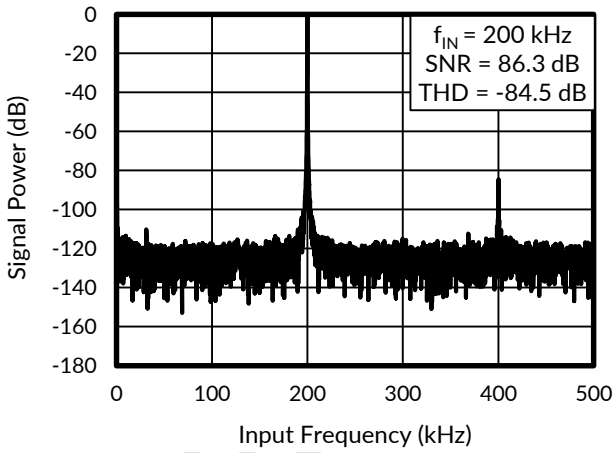


Figure 3. Typical FFT

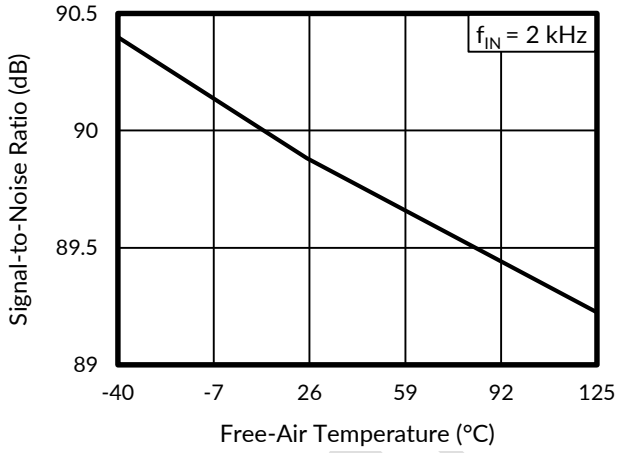


Figure 4. SNR vs Temperature

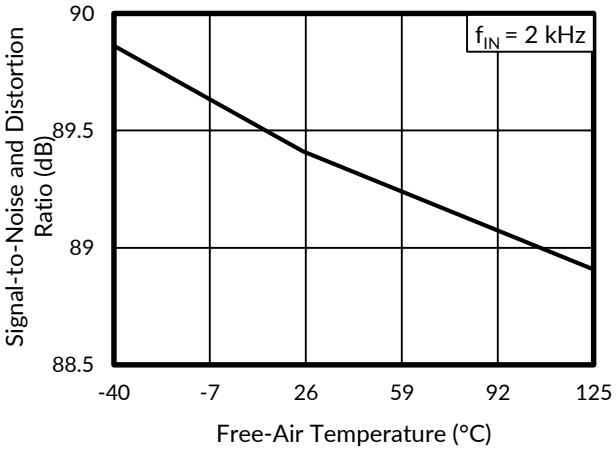


Figure 5. SINAD vs Temperature

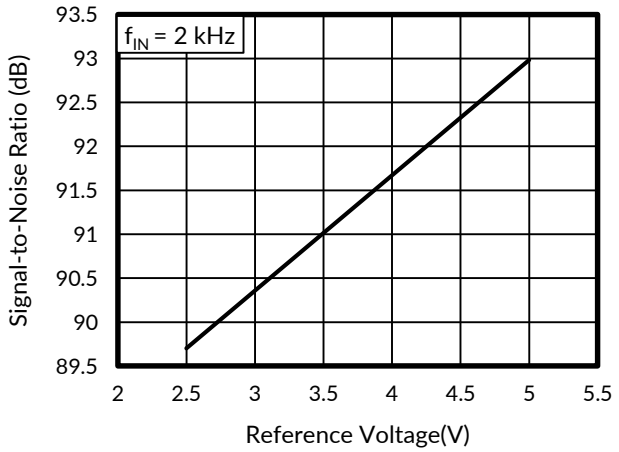


Figure 6. SNR vs Reference Voltage

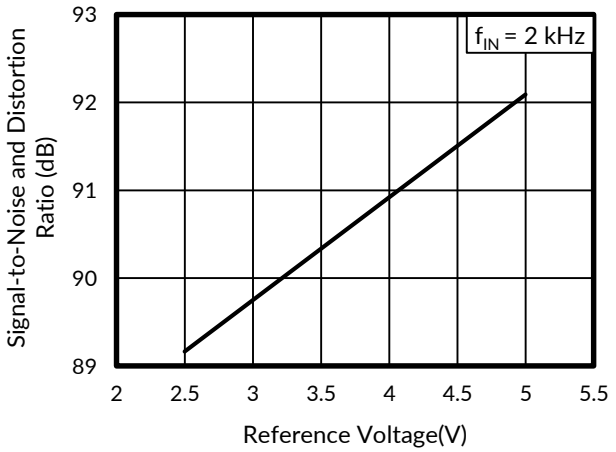


Figure 7. SINAD vs Reference Voltage

Typical Characteristics(continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V (internal), and f_{DATA} = 1MSPS, 16-clock mode, unless otherwise noted.

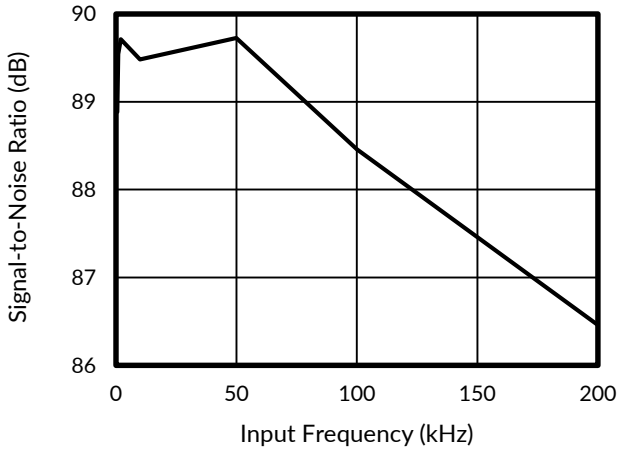


Figure 8. SNR vs Input Frequency

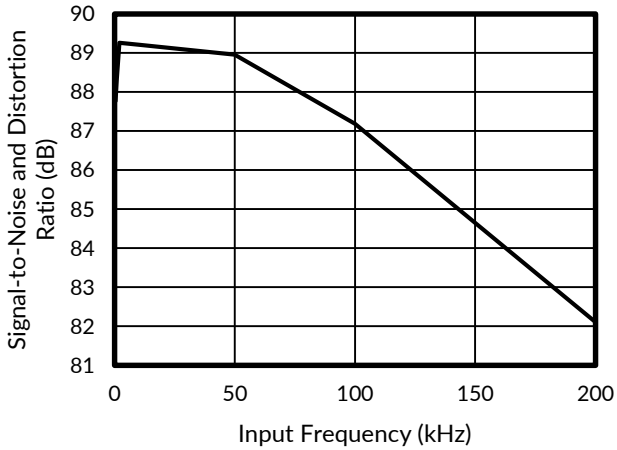


Figure 9. SINAD vs Input Frequency

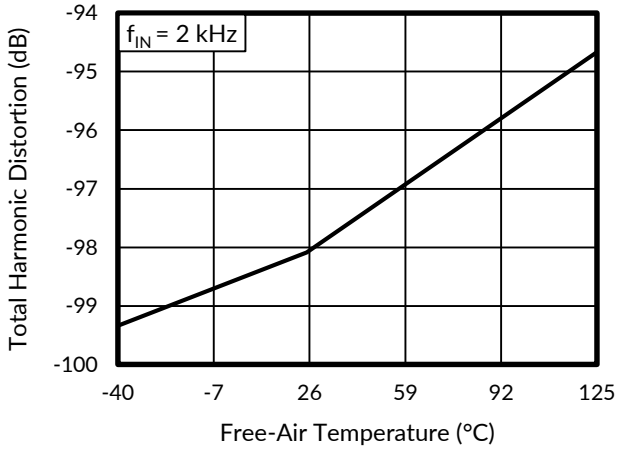


Figure 10. THD vs Temperature

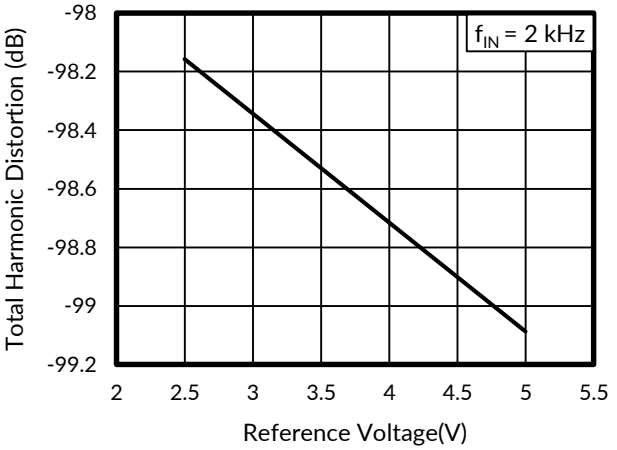


Figure 11. THD vs Reference Voltage

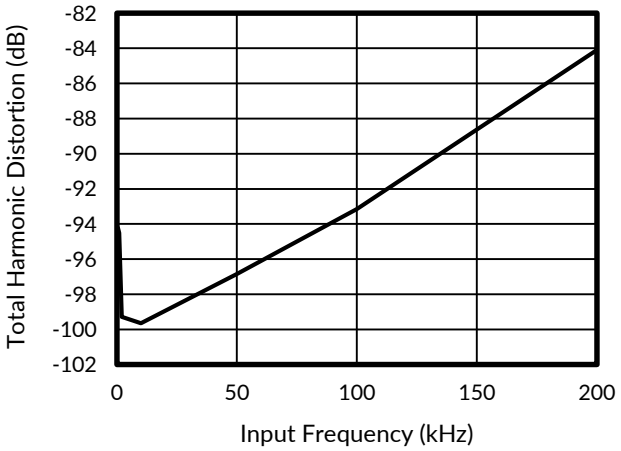


Figure 12. THD vs Input Frequency

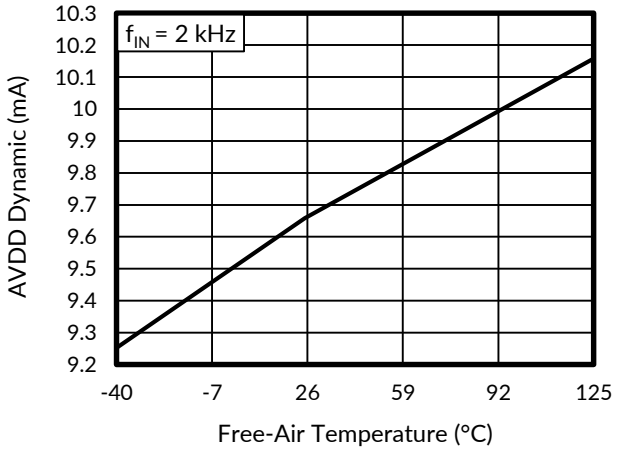


Figure 13. Analog Supply Current vs Temperature

Typical Characteristics(continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V (internal), and f_{DATA} = 1MSPS, 16-clock mode, unless otherwise noted.

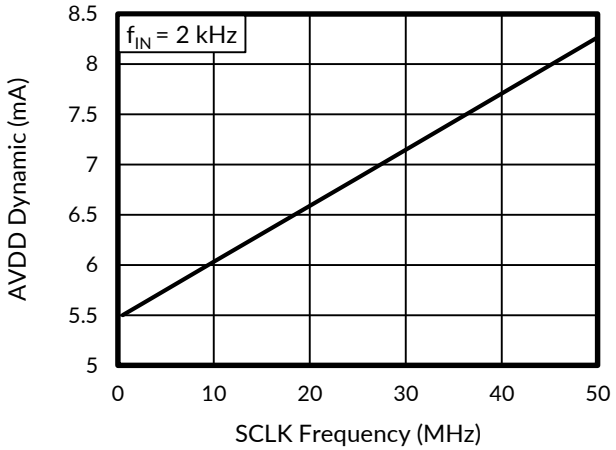


Figure 14. Analog Supply Current vs SCLK Frequency

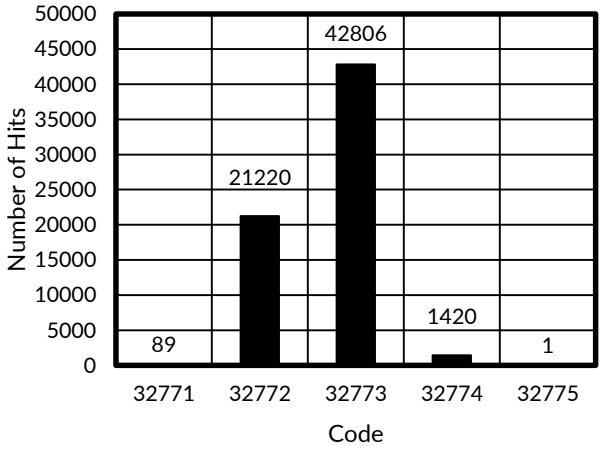


Figure 15. DC Histogram

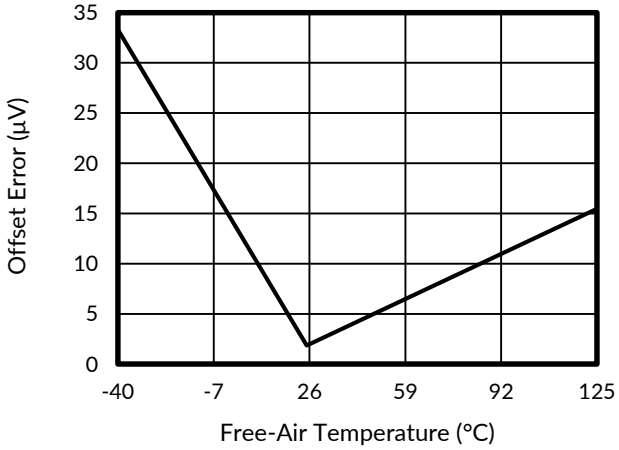


Figure 16. Offset Error vs Temperature

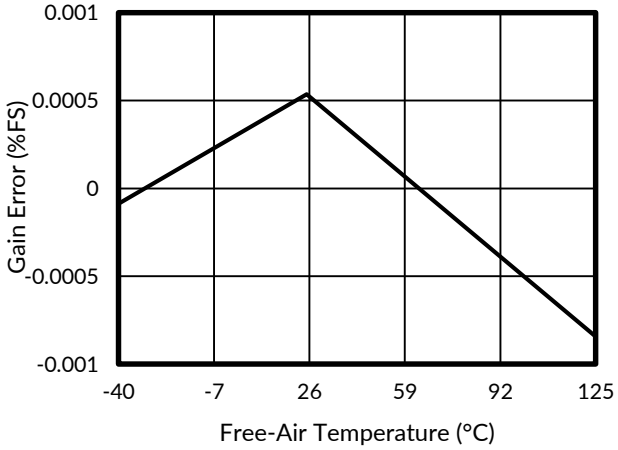


Figure 17. Gain Error vs Temperature

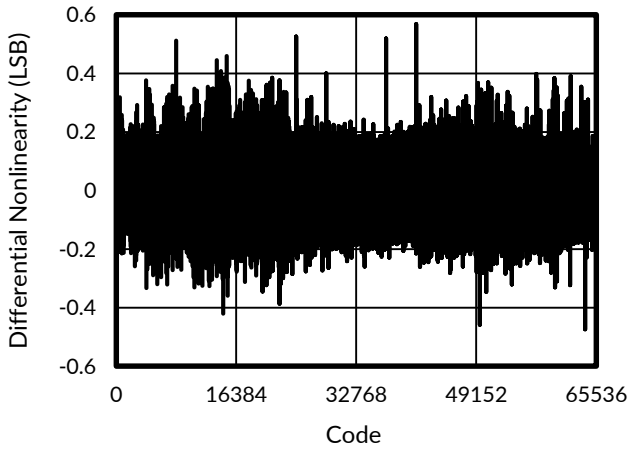


Figure 18. Typical DNL

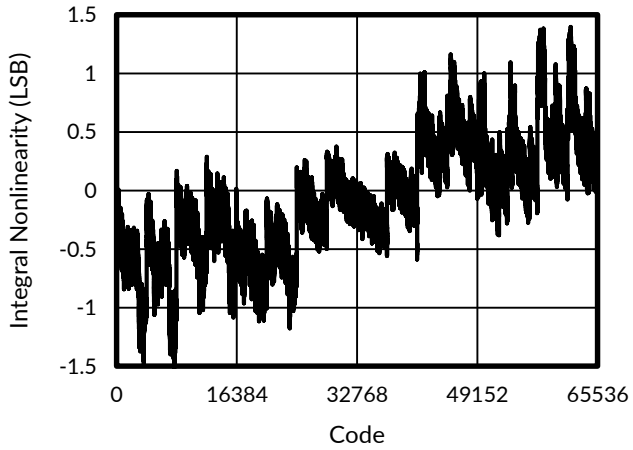


Figure 19. Typical INL

Typical Characteristics(continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V (internal), and f_{DATA} = 1MSPS, 16-clock mode, unless otherwise noted.

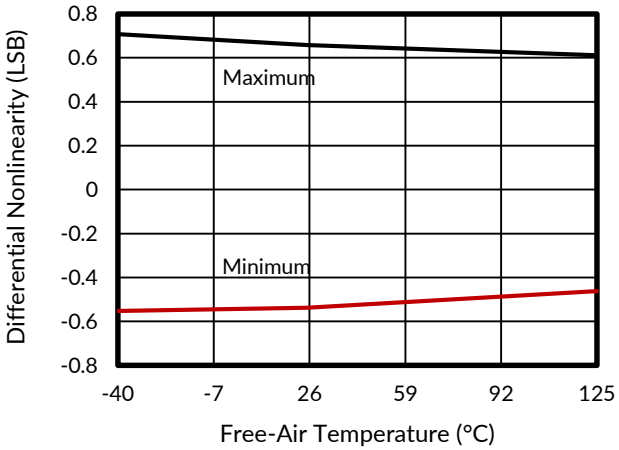


Figure 20. DNL vs Temperature

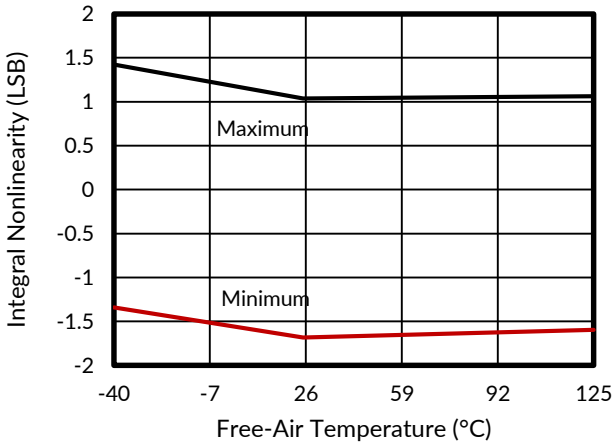


Figure 21. INL vs Temperature

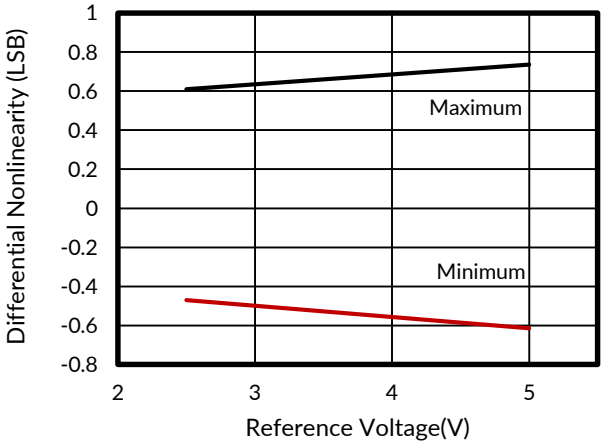


Figure 22. DNL vs Reference Voltage

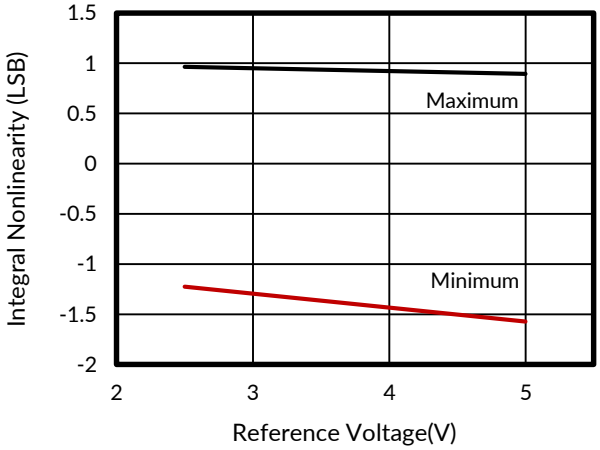


Figure 23. INL vs Reference Voltage

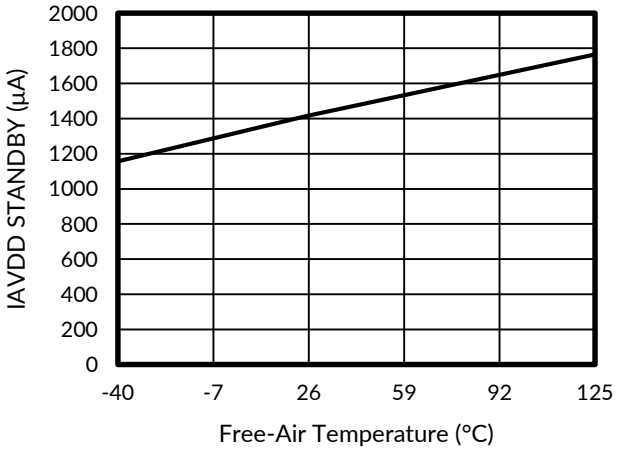


Figure 24. STANDBY Current vs Temperature

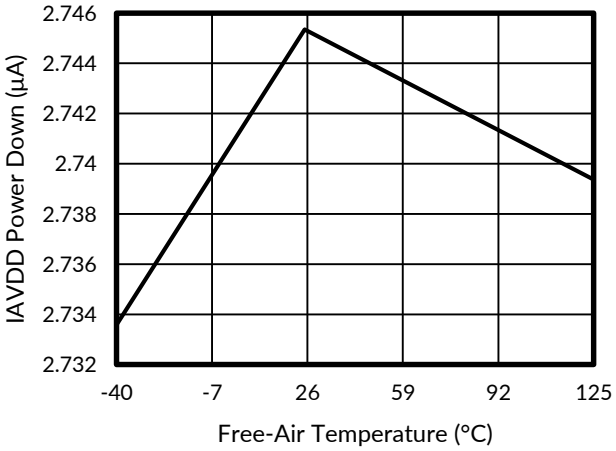


Figure 25. Power-Down Current vs Temperature

Typical Characteristics(continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V (internal), and f_{DATA} = 1MSPS, 16-clock mode, unless otherwise noted.

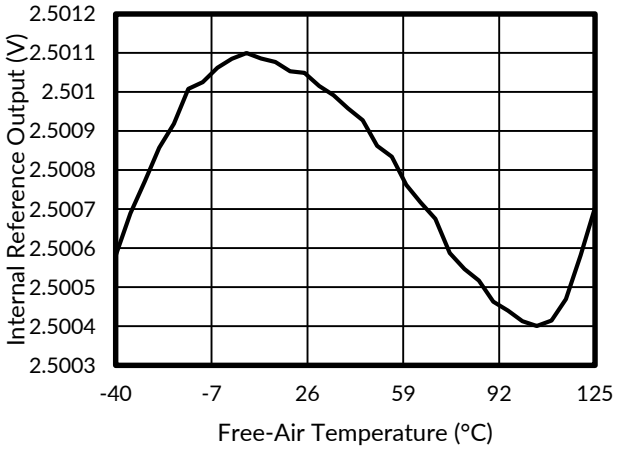


Figure 26. Internal Reference Output vs Temperature

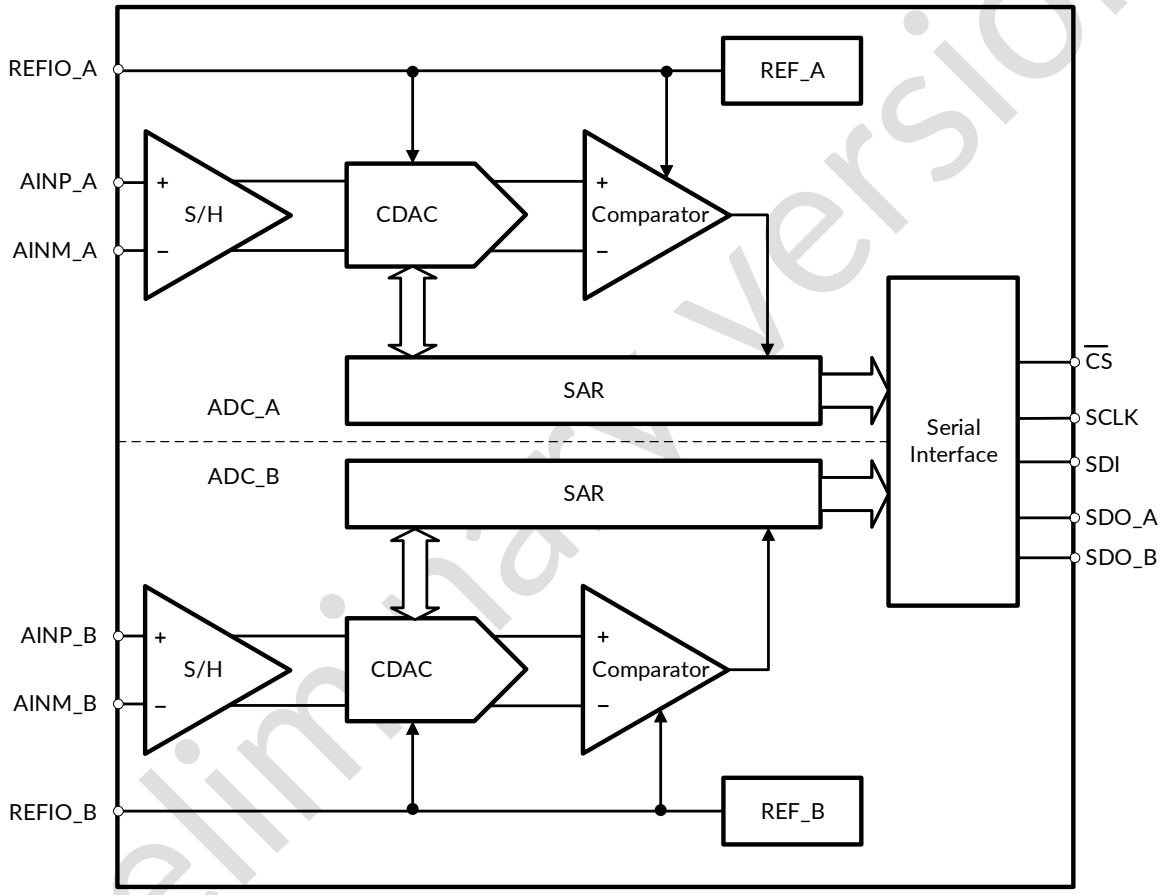
8 DETAILED DESCRIPTION

8.1 Overview

The RS1432 is a 16Bit, dual, high-speed, simultaneous-sampling, analog-to-digital converters (ADCs). The RS1432 supports fully-differential input signals. It provides a simple, serial interface for communication with the host controller and operates across a wide range of analog and digital power supplies.

This device has two independently programmable internal references to achieve system-level gain error correction. The Functional Block Diagram section provides a diagram of the device.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Reference

The device has two simultaneous sampling ADCs (ADC_A and ADC_B). ADC_A and ADC_B operate with reference voltages V_{REF_A} and V_{REF_B} present on the REFIO_A and REFIO_B pins, respectively. The REFIO_A and REFIO_B pins should be decoupled from the REFGND_A and REFGND_B pins, respectively, with 10µF decoupling capacitors.

The device supports operation with either an internal or external reference source, as shown in Figure 27. The reference voltage source is determined by setting bit 6 of the configuration register (CFR.B6). Note that this bit is common to both ADC_A and ADC_B.

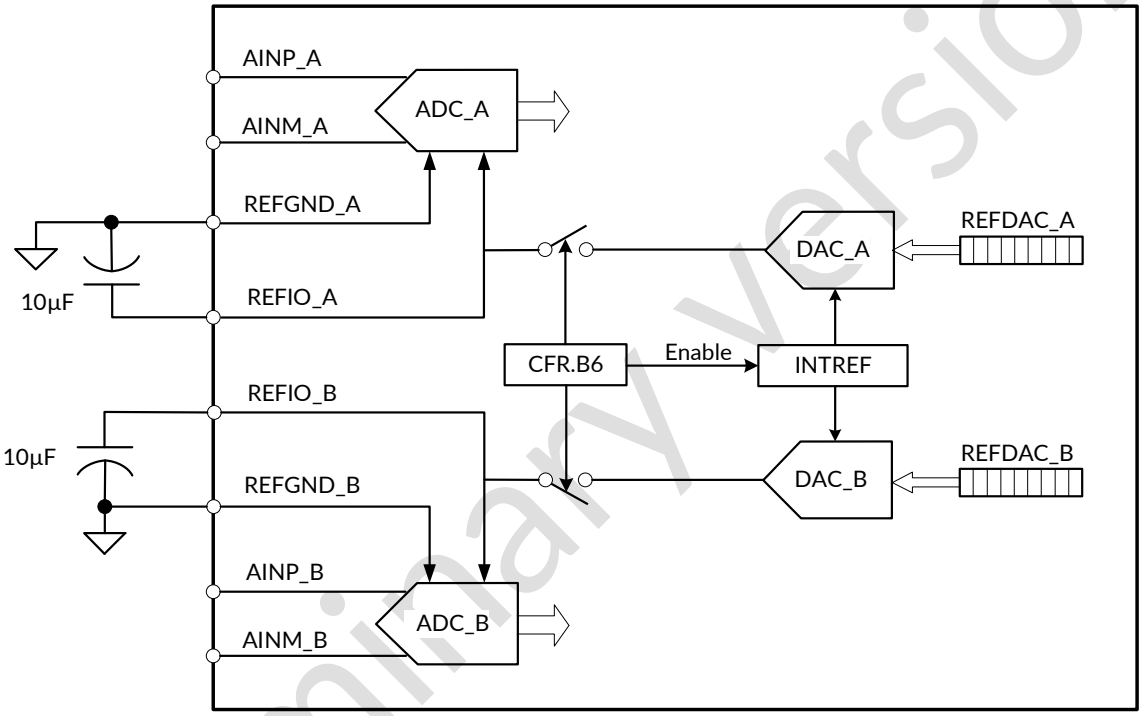


Figure 27. Reference Configurations and Connections

When CFR.B6 is 0, the device shuts down the internal reference source (INTREF), and ADC_A and ADC_B operate with external reference voltages provided by the user on the REFIO_A and REFIO_B pins, respectively.

When CFR.B6 is 1, the device operates with the internal reference source (INTREF) connected to REFIO_A and REFIO_B via DAC_A and DAC_B, respectively. In this configuration, V_{REF_A} and V_{REF_B} can be changed independently by writing to the user-programmable registers REFDAC_A and REFDAC_B, respectively. Refer to the REFDAC Registers (REFDAC_A and REFDAC_B) section for more details.

8.3.2 Analog Inputs

The RS1432 supports fully-differential analog inputs on both ADC channels. These inputs are sampled and converted simultaneously by the two ADCs, ADC_A and ADC_B. ADC_A samples and converts ($V_{AINP\_A} - V_{AINM\_A}$), and ADC_B samples and converts ($V_{AINP\_B} - V_{AINM\_B}$).

Figure 28a and Figure 28b show equivalent circuits for the ADC_A and ADC_B analog input pins, respectively. Series resistance, R_S, represents the on-state sampling switch resistance and C_{SAMPLE} is the device sampling capacitor (typically 40 pF).

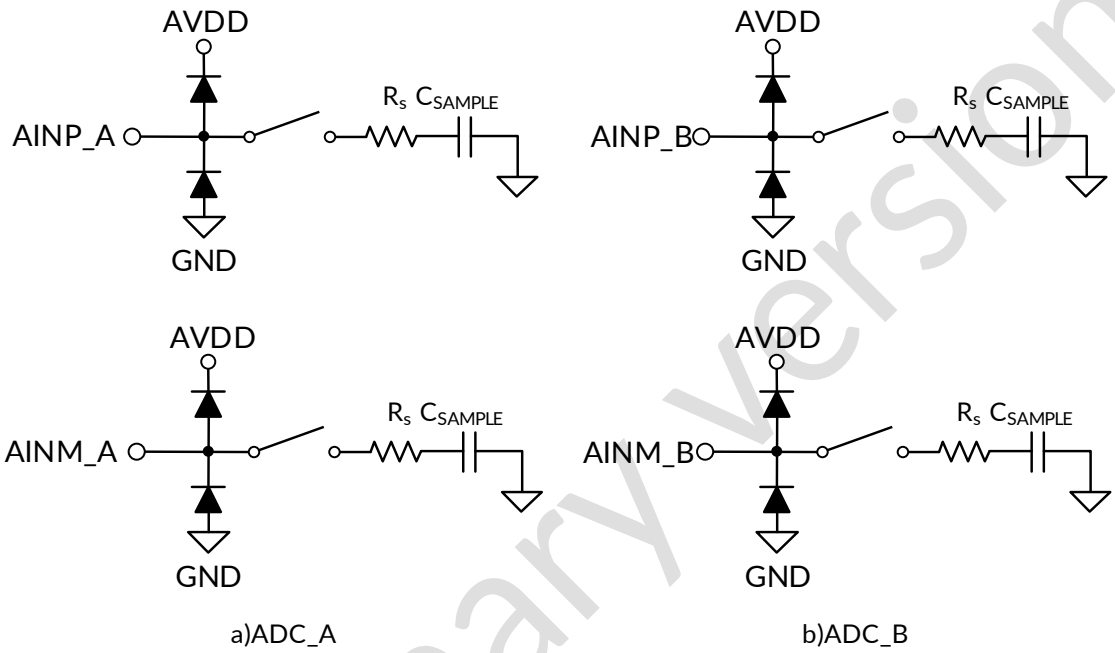


Figure 28. Equivalent Circuit for the Analog Input Pins

8.3.2.1 Analog Input: Full-Scale Range Selection

The full-scale range (FSR) supported at the analog inputs of the device is programmable via bit B9 of the configuration register (CFR.B9). This bit is common to both ADCs (ADC_A and ADC_B).

The FSR is given by Equations 1 and Equations 2:

$$\text{For CFR. B9 = 0, FSR\_ADC\_A= } \pm V_{REF\_A} \text{ and FSR\_ADC\_B= } \pm V_{REF\_B} \quad (1)$$

$$\text{For CFR.B9 = 1, FSR\_ADC\_A= } \pm 2 \times V_{REF\_A} \text{ and FSR\_ADC\_B= } \pm 2 \times V_{REF\_B} \quad (2)$$

where:

- V_{REF_A} and V_{REF_B} are the reference voltages going to ADC_A and ADC_B, respectively (as described in the Reference section).

Therefore, with the appropriate settings of the REFDAC_A and REFDAC_B registers, CFR.B7, and CFR.B9, the maximum dynamic range of the ADC can be used.

Note that while using CFR.B9 set to 1, care must be taken so that the ADC analog supply (AVDD) is as in Equation 3 and Equation 4:

$$2 \times V_{REF\_A} \le \text{AVDD} \le \text{AVDD(max)} \quad (3)$$

$$2 \times V_{REF\_B} \le \text{AVDD} \le \text{AVDD(max)} \quad (4)$$

8.3.2.2 Analog Input: Fully-Differential Configurations

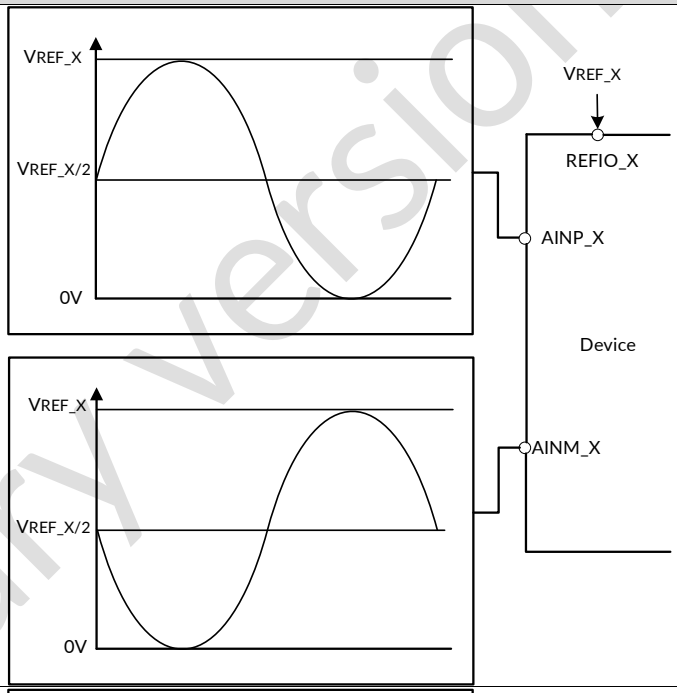
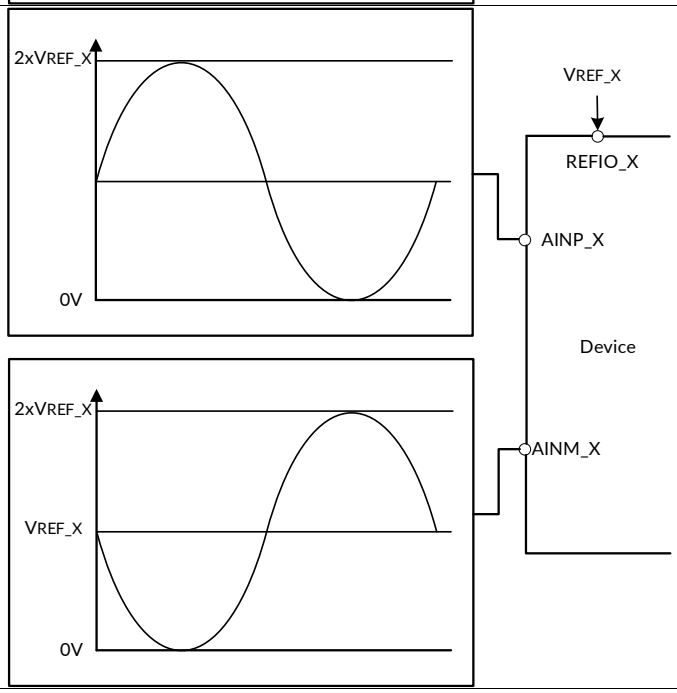
The RS1432 can support fully-differential input signals. Equation 5 and Equation 6 provide the common-mode voltage for the ADC_A and ADC_B differential inputs.

$$VCM\_A = FSR\_ADC\_A / 2 \quad (5)$$

$$VCM\_B = FSR\_ADC\_B / 2 \quad (6)$$

The various input configurations supported by the device are shown in Table 1.

Table 1. Input Configurations

INPUT RANGE SELECTION	AINM SELECTION	CONNECTION DIAGRAM
CFR.B9 = 0 (FSR_ADC_A = $\pm V_{REF\_A}$) (FSR_ADC_B = $\pm V_{REF\_B}$)	$V_{CM\_A} = \left(\frac{V_{REF\_A}}{2}\right) \pm 0.1$ V $V_{CM\_B} = \left(\frac{V_{REF\_B}}{2}\right) \pm 0.1$ V	
CFR.B9 = 1 (FSR_ADC_A = 2 x V_{REF_A}) (FSR_ADC_B = 2 x V_{REF_B})	$V_{CM\_A} = V_{REF\_A} \pm 0.1$ V $V_{CM\_B} = V_{REF\_B} \pm 0.1$ V	

8.3.3 Transfer Function

The device output is in twos compliment format. Device resolution for a fully-differential input is calculated by Equation 7:

$$1\ LSB = (2 \times FSR\_ADC\_x) / (2^N) \quad (7)$$

where:

- N = 16.
- FSR_ADC_x is the full-scale input range of the ADC (refer to the Analog Input section for more details).

Table 2 and Table 3 show the different input voltages and the corresponding output codes from the device.

Table 2. Transfer Characteristics for Straight Binary Output (CFR.B4 = 0, Default)

INPUT VOLTAGE (AINP_x – AINM_x), ±V_{REF} RANGE	INPUT VOLTAGE (AINP_x – AINM_x), ±2 × V_{REF} RANGE	INPUT VOLTAGE	OUTPUT CODE (Hex)	
			CODE	
< – V_{REF_x}	< –2 × V_{REF_x}	NFSC	NFSC	0000
0	0	0	PLC	7FFF
> V_{REF_x}	> 2 × V_{REF_x}	PFSC	PFSC	FFFF

Table 3. Transfer Characteristics for Twos Compliment Output (CFR.B4 = 1)

INPUT VOLTAGE (AINP_x – AINM_x), ±V_{REF} RANGE	INPUT VOLTAGE (AINP_x – AINM_x), ±2 × V_{REF} RANGE	INPUT VOLTAGE	OUTPUT CODE (Hex)	
			CODE	
< – V_{REF_x}	< –2 × V_{REF_x}	NFSC	NFSC	8000
–V_{REF_x} + 1 LSB	–2 × V_{REF_x} + 1 LSB	NFSR	NFSC + 1	8001
–1 LSB	–1 LSB	–1 LSB	MC	FFFF
0	0	0	PLC	0000
> V_{REF_x} – 1 LSB	> 2 × V_{REF_x} – 1 LSB	PFSR – 1 LSB	PFSC	7FFF

Figure 29 shows the ideal transfer characteristics for the device.

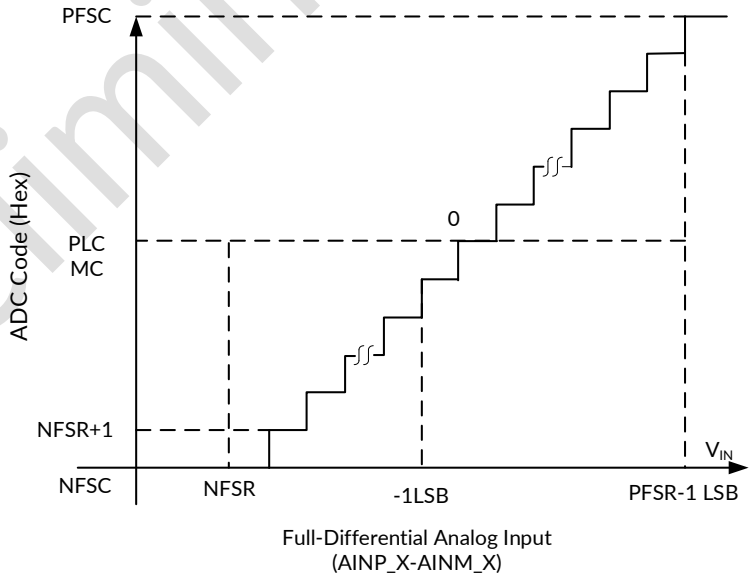


Figure 29. Ideal Transfer Characteristics for a Fully-Differential Analog Input

8.4 Device Functional Modes

The device provides three user-programmable registers: the configuration register (CFR), the REFDAC_A register, and the REFDAC_B register. These registers support write operations (refer to the Write to User-Programmable Registers section) and readback operations (refer to the Reading User-Programmable Registers section), and allow the user to customize ADC behavior for specific application requirements.

The device supports three interface modes (refer to the Conversion Data Read section), two low-power modes (refer to the Low-Power Modes section).

8.5 Register Maps and Serial Interface

8.5.1 Serial Interface

The device uses the serial clock (SCLK) for synchronizing data transfers in and out of the device.

The $\overline{CS}$ signal defines one conversion and serial transfer frame. A frame starts with a $\overline{CS}$ falling edge and ends with a $\overline{CS}$ rising edge. Between the start and end of the frame, a minimum of N SCLK falling edges must be provided to validate the read or write operation. As shown in Table 4, N depends upon the interface mode used to read the conversion result. When N SCLK falling edges are provided, the write operation attempted in the frame is validated and the internal user-programmable registers are updated on the subsequent $\overline{CS}$ rising edge. This $\overline{CS}$ rising edge also ends the frame.

Table 4. SCLK Falling Edges for a Valid Write Operation

INTERFACE MODE	MINIMUM SCLK FALLING EDGES REQUIRED TO VALIDATE WRITE OPERATION N
32-CLK, dual-SDO mode (default). See the 32-CLK, Dual-SDO Mode section.	32
32-CLK, single-SDO mode. See the 32-CLK, Single-SDO Mode section.	48
16-CLK, dual-SDO mode. See the 16-CLK, Dual-SDO Mode section.	16

8.5.2 Write to User Programmable Registers

The device features three user-programmable registers: the configuration register (CFR), the REFDAC_A register, and the REFDAC_B register. These registers can be written with the device SDI pin. The first 16 bits of data on SDI are latched into the device on the first 16 SCLK falling edges. However, the new configuration takes effect only when the read or write operation is validated. If these registers are not required to update, SDI must remain low during the respective frames.

The first four SDI data bits (B[15:12]) determine what operation is performed (that is, either a read or write operation or no operation), which register address the operation uses, and the function of the next 12 SDI data bits (B[11:0]). Table 5 lists the various combinations supported for B[15:12].

Table 5. Data Write Operation

B15	B14	B13	B12	OPERATION	FUNCTION OF BITS B[11:0]
0	0	0	0	No operation is performed	These bits are ignored
0	0	0	1	REFDAC_A read	000h; see the Reading User-Programmable Registers section
0	0	1	0	REFDAC_B read	000h; see the Reading User-Programmable Registers section
0	0	1	1	CFR read	000h; see the Reading User-Programmable Registers section
1	0	0	0	CFR write	See the Configuration Register (CFR) section
1	0	0	1	REFDAC_A write	See the REFDAC_A section
1	0	1	0	REFDAC_B write	See the REFDAC_B section
1	0	1	1	No operation is performed	These bits are ignored
X	1	X	X	No operation is performed	These bits are ignored

8.5.2.1 Configuration Register (CFR)

The device operation configuration is controlled by the configuration register (CFR) status. Data written into the CFR in a valid frame (F) determine the device configuration for frame (F+1). The bit functions are outlined in Table 6. On power-up, all bits in the CFR default to 0.

Table 6. CFR Bit Functions

15	14	13	12	11	10	9	8
WRITE/READ	0	ADDR1	ADDR0	RD_CLK_ MODE	RD_DATA_ LINES	INPUT_ RANGE	0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	REF_SEL	STANDBY	RD_DATA_ FORMAT	0	0	0	SOFT_RESET

Table 7. Configuration Register (CFR) Field Descriptions

Bit	Field	Type	Reset	Description
15	WRITE/READ	W	0h	These bits select the user-programmable register. 1000 = Select this combination to write to the CFR register and to enable bits 11:0
14	0	R/W	0h	
13	ADDR1	R/W	0h	
12	ADDR0	R/W	0h	
11	RD_CLK_MODE	R/W	0h	This bit provides clock mode selection for the serial interface. 0 = Select 32-CLK mode (default) 1 = Select 16-CLK mode
10	RD_DATA_LINES	R/W	0h	This bit provides data line selection for the serial interface. 0 = Use SDO_A to output ADC_A data and SDO_B to output of ADC_B data (default) 1 = Use only SDO_A to output of ADC_A data followed by ADC_B data
9	INPUT_RANGE	R/W	0h	This bit selects the maximum input range for the ADC as a function of the reference voltage provided to the ADC. See the Analog Inputs section for more details. 0 = FSR equals V_{REF} 1 = FSR equals 2 × V_{REF}
8	0	R/W	0h	This bit must be set to 0 (default).
7	0	R/W	0h	This bit must be set to 0 (default).
6	REF_SEL	R/W	0h	This bit selects the ADC reference voltage source. Refer to the Reference section for more details. 0 = Use external reference (default) 1 = Use internal reference
5	STANDBY	W	0h	This bit is used by the device to enter or exit STANDBY mode. Refer to the STANDBY Mode section for more details.
4	RD_DATA_FORMAT	R/W	0h	This bit selects the output data format. 0 = Output is in straight binary format (default) 1 = Output is in twos compliment format
3:1	0	R/W	0h	These bits must be set to 0 (default).
0	SOFT_RESET	R/W	0h	This bit selects the soft reset function. 0 = no reset action (default) 1 = soft reset, all registers reset to 0 (default)

8.5.2.2 REFDAC Registers (REFDAC_A and REFDAC_B)

The REFDAC registers, bit functions, and resolution information are described in this section.

Table 8. REFDAC_X Bit Functions

15	14	13	12	11	10	9	8
WRITE/READ	0	ADDR1	ADDR0	D8	D7	D6	D5
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
D4	D3	D2	D1	D0	0	0	0

Table 9. REFDAC Registers Field Descriptions

Bit	Field	Type	Reset	Description
15	WRITE/READ	W	0h	These bits select the configurable register address. 1001 = Select this combination to write to the REFDAC_A register 1010 = Select this combination to write to the REFDAC_B register
14	0	R/W	0h	
13	ADDR1	R/W	0h	
12	ADDR0	R/W	0h	
11:3	D[8:0]	R/W	0h	Data to program the individual DAC output voltage. Note: These bits are valid only for bits 15:12 = 1001 or bits 15:12 = 1010. Table 10 shows the relationship between the REFDAC_x programmed value and the DAC_x output voltage.
2:0	0	R/W	0h	This bit must be set to 0 (default)

Table 10. REFDAC Settings

REFDAC_x VALUE (Bits 11:3 in Hex)	B[2:0]	Typical DAC_x OUPTUT VOLTAGE (V) (1)
1FF	000	2.5000
1FE	000	2.4989
1FD	000	2.4978
—	—	—
1D7	000	2.45
—	—	—
1AE	000	2.40
—	—	—
186	000	2.35
—	—	—
15D	000	2.30
—	—	—
134	000	2.25
—	—	—
10C	000	2.20
—	—	—
0E3	000	2.15
—	—	—
0BA	000	2.10
—	—	—
091	000	2.05
—	—	—
069	000	2.00
—	—	—
000 (default)	000	1.87

(1) Actual output voltage may vary by a few millivolts from the specified value. To obtain the desired output voltage, start with the specified register setting and then experiment with five codes on either side of this setting.

8.5.3 Data Read Operation

The device supports two types of read operations: reading user-programmable registers and reading conversion results.

8.5.3.1 Reading User-Programmable Registers

The device supports a readback option for all user-programmable registers: CFR, REFDAC_A, and REFDAC_B. Figure 30 shows a detailed timing diagram for this operation.

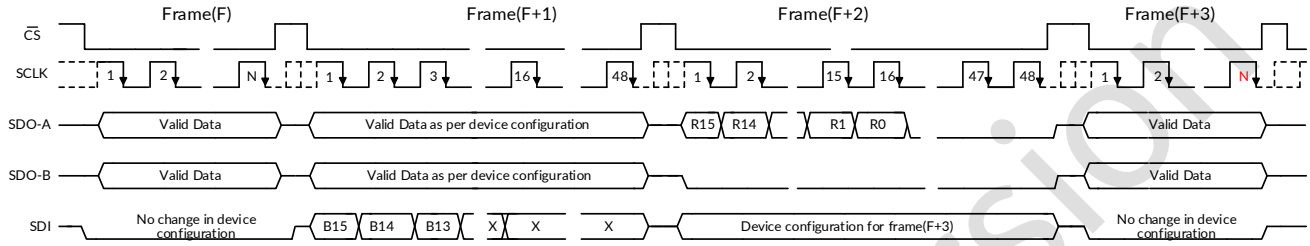


Figure 30. Register Readback Timing

To readback the user-programmable register settings, the appropriate control word should be transmitted to the device during frame (F+1), as shown in Table 11. Frame (F+1) must have at least 48 SCLK falling edges.

Table 11. Control Word to Readback User-Programmable Registers

USER-PROGRAMMABLE REGISTER	CONTROL WORD TO BE PROGRAMMED IN FRAME (F+1)	
	B[15:12] (Binary)	B[11:0] (Hex)
CFR	0011b	000h
REFDAC_A	0001b	000h
REFDAC_B	0010b	000h

Frame (F+2) must have at least 48 SCLK falling edges. During frame (F+2), SDO_A outputs the contents of the selected user-programmable register on the first 16 SCLK falling edges (as shown in Table 12) and then outputs 0s for any subsequent SCLK falling edges. The SDO_B pin outputs 0s for all the SCLK falling edges.

Table 12. Register Data Read Back

USER-PROGRAMMABLE REGISTER	DATA READ ON SDO-A IN FRAME (F+2)									
	R15	R14	R13	R12	R11	—	R3	R2	R1	R0
CFR	0	0	1	1	CFG.B11	—	CFG.B3	CFG.B2	CFG.B1	CFG.B0
REFDAC_A	0	0	0	1	REFDAC_A.D8	—	REFDAC_A.D0	0	0	0
REFDAC_B	0	0	1	0	REFDAC_B.D8	—	REFDAC_B.D0	0	0	0

Register settings programmed during frame (F+2) determine the device configuration in frame (F+3).

8.5.3.2 Conversion Data Read

The device provides three different interface modes to the user for reading the conversion result. These modes offer flexible hardware connections and firmware programming. Table 13 shows how to select one of the three interface modes.

Table 13. Interface Mode Selection

CFR.B11	CFR.B10	INTERFACE MODE	MINIMUM SCLK FALLING EDGES REQUIRED TO VALIDATE WRITE OPERATION N
0	0	32-CLK, dual-SDO mode (default)	32
0	1	32-CLK, single-SDO mode	48
1	X	16-CLK, dual-SDO mode	16

In the 32-CLK interface modes, the device uses an internal clock to convert the sampled analog signal. The conversion is completed during the first 16 periods of SCLK and the conversion result can be read on the subsequent SCLK falling edges.

In addition to the 32-CLK interface modes, the RS1432 also support the 16-CLK interface modes. By using the 16-CLK interface modes, the same throughput can be achieved at much lower SCLK speeds.
The following sections detail the various interface modes supported by the device.

8.5.3.2.1 32-CLK, Dual-SDO Mode (CFR.B11 = 0, CFR.B10 = 0, Default)

The 32-CLK dual-SDO mode is the default mode supported by the devices. This mode can also be selected by writing CFR.B11 = 0 and CFR.B10 = 0.

In this mode, the SDO_A pin outputs the ADC_A conversion result and the SDO_B pin outputs the ADC_B conversion result. Figure 31 shows a detailed timing diagram for this mode.

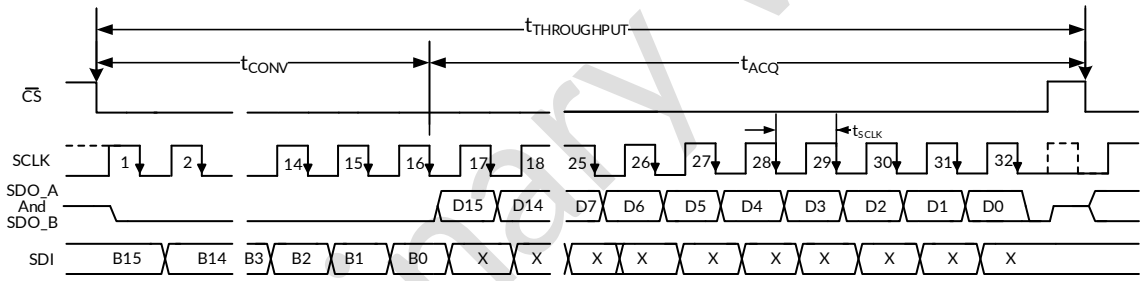


Figure 31. 32-CLK, Dual-SDO Mode Timing Diagram

A $\overline{CS}$ falling edge brings the serial data bus out of 3-state and also outputs a 0 on the SDO_A and SDO_B pins. The device converts the sampled analog input during the conversion time (t_{CONV}). SDO_A and SDO_B read 0 during this period. After completing the conversion process, the sample-and-hold circuit returns to sample mode. The device outputs the MSBs of ADC_A and ADC_B on SDO_A and SDO_B pins, respectively, on the 16th SCLK falling edge. The subsequent SCLK falling edges are used to shift out the rest of the bits of the conversion result, as shown in Table 14.

Table 14. Data Launch Edge

PINS	LAUNCH EDGE												
	$\overline{CS}$	SCLK											$\overline{CS}$
	↓	↓1	–	↓15	↓16	–	↓27	↓28	↓29	↓30	↓31	↓32 ...	↑
SDO-A	0	0	–	0	D15_A	–	D4_A	D3_A	D2_A	D1_A	D0_A	0 ...	Hi-Z
SDO-B	0	0	–	0	D15_B	–	D4_B	D3_B	D2_B	D1_B	D0_B	0 ...	Hi-Z

In this mode, at least 32 SCLK falling edges must be provided to validate the read data or write configuration frame. A $\overline{CS}$ rising edge ends the frame and puts the serial bus into 3-state.

Refer to Table 15 for timing specifications specific to this serial interface mode.

Table 15. 32-CLK, Dual-SDO Interface Specific Timing

PARAMETER		MIN	TYP	MAX	UNIT
TIMING REQUIREMENTS					
t_{CLK}	CLOCK period	20			ns
t_{ACQ}	Acquisition time		33 × t_{CLK} - t_{CONV}		ns
TIMING SPECIFICATIONS					
t_{CONV}	Conversion time			640	ns

8.5.3.2.2 32-CLK, Single-SDO Mode (CFR.B11 = 0, CFR.B10 = 1)

The 32-CLK, single-SDO mode provides the option of using only one SDO pin (SDO_A) to read conversion results from both ADCs (ADC_A and ADC_B). SDO_B remains in 3-state and can be treated as a no connect (NC) pin.

This mode can be selected by writing CFR.B11 = 0 and CFR.B10 = 1. Figure 33 shows a detailed timing diagram for this mode.

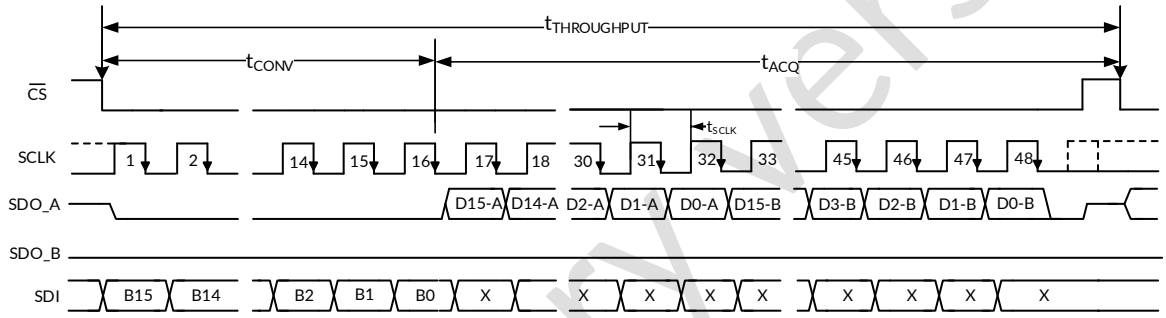


Figure 33. 32-CLK, Single-SDO Mode Timing Diagram

A $\overline{CS}$ falling edge brings the serial data bus out of 3-state and also outputs a 0 on the SDO_A pin. The device converts the sampled analog input during the conversion time (t_{CONV}). SDO_A reads 0 during this period. After competing the conversion process, the sample-and-hold circuit goes back into sample mode. The device outputs the MSB of ADC_A on the SDO_A pin on the 16th SCLK falling edge. The subsequent SCLK falling edges are used to shift out the conversion result of ADC_A followed by the conversion result of ADC_B on the SDO_A pin, as shown in Table 16.

Table 16. Data Launch Edge

PIN	LAUNCH EDGE																			
	$\overline{CS}$	SCLK																		$\overline{CS}$
	↓	↓1	–	↓15	↓16	–	↓27	↓28	↓29	↓30	↓31	↓32	–	↓43	↓44	↓45	↓46	↓47	↓48 ...	↑
SDO-A	0	0	–	0	D15_A	–	D4_A	D3_A	D2_A	D1_A	D0_A	D15_B	–	D4_B	D3_B	D2_B	D1_B	D0_B	0 ...	Hi-Z

In this mode, at least 48 SCLK falling edges must be given to validate the read data or write configuration frame. A $\overline{CS}$ rising edge ends the frame and puts the serial bus into 3-state.

Refer to Table 17 for timing specifications specific to this serial interface mode.

Table 17. 32-CLK, Single-SDO Interface Specific Timing

PARAMETER		MIN	TYP	MAX	UNIT
TIMING REQUIREMENTS					
t_{CLK}	CLOCK period	20			ns
t_{ACQ}	Acquisition time		49 × t_{CLK} - t_{CONV}		ns
TIMING SPECIFICATIONS					
t_{CONV}	Conversion time			640	ns

8.5.3.2.3 16-CLK, Dual-SDO Mode (CFR.B11 = 1, CFR.B10 = 0)

The 16-CLK, dual-SDO mode is designed to support maximum throughput at lower SCLK frequencies.

For the RS1432, this interface mode can be selected by setting CFR.B11 = 1 and CFR.B10 = 0. In this mode, the SDO_A pin outputs the ADC_A conversion result, and SDO_B outputs the ADC_B result. Figure 34 shows a detailed timing diagram for this mode.

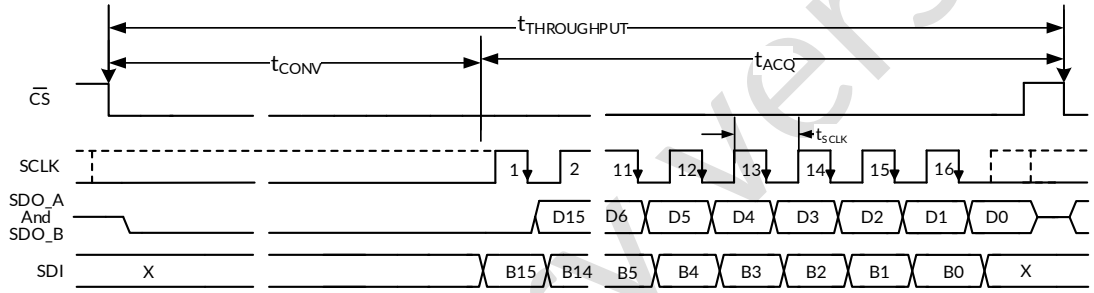


Figure 34. 16-CLK, Dual-SDO Mode Timing Diagram

A $\overline{CS}$ falling edge brings the serial data bus out of 3-state and also outputs a 0 on the SDO_A and SDO_B pins. The subsequent SCLK falling edges are used for conversion and for data transfer using the serial interface, as shown in Table 18.

The sample-and-hold circuit goes back into sample mode as soon as the conversion process is over.

Table 18. Data Launch Edge

PINS	LAUNCH EDGE								
	$\overline{CS}$	SCLK							$\overline{CS}$
	↓	↓1	↓2	–	↓13	↓14	↓15	↓16 ...	↑
SDO-A	0	D15_A	D14_A	–	D3_A	D2_A	D1_A	D0_A ...	Hi-Z
SDO-B	0	D15_B	D14_B	–	D3_B	D2_B	D1_B	D0_B ...	Hi-Z

In this mode, at least 16 SCLK falling edges must be given to validate the read data or write configuration frame. A $\overline{CS}$ rising edge ends the frame and puts the serial bus into 3-state.

Refer to Table 19 for timing specifications specific to this serial interface mode.

Table 19. 16-CLK, Dual-SDO Interface Specific Timing

PARAMETER		MIN	TYP	MAX	UNIT
TIMING REQUIREMENTS					
t_{CLK}	CLOCK period	20			ns
t_{ACQ}	Acquisition time		17 × t_{CLK}		ns
TIMING SPECIFICATIONS					
t_{CONV}	Conversion time			640	ns

8.5.4 Low-Power Modes

In normal mode of operation, all internal circuits of the device are always powered up and the device is always ready to commence a new conversion. This mode enables the device to support the rated throughput. The device also supports two low-power modes to optimize the power consumption at lower throughputs: STANDBY mode and software power-down (SPD) mode.

8.5.4.1 STANDBY Mode

The device supports a STANDBY mode of operation where some of the internal circuits of the device are powered down. However, if bit 6 in configuration register is set to 1 (CFR.B6 = 1), then the internal reference is not powered down and the contents of the REFDAC_A and REFDAC_B registers are retained to enable faster power-up to a normal mode of operation.

As shown in Figure 35, a valid write operation in frame (F) to program the configuration register with B5 set to 1 (CFR.B5 = 1) places the device into a STANDBY mode of operation on the following $\overline{CS}$ rising edge. While in STANDBY mode, SDO_A and SDO_B output all 1s when $\overline{CS}$ is low and remain in 3-state when $\overline{CS}$ is high. To remain in STANDBY mode, SDI must remain low in the subsequent frames.

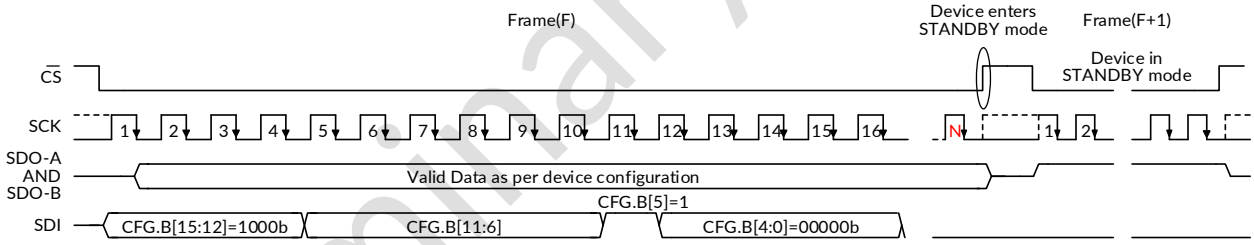
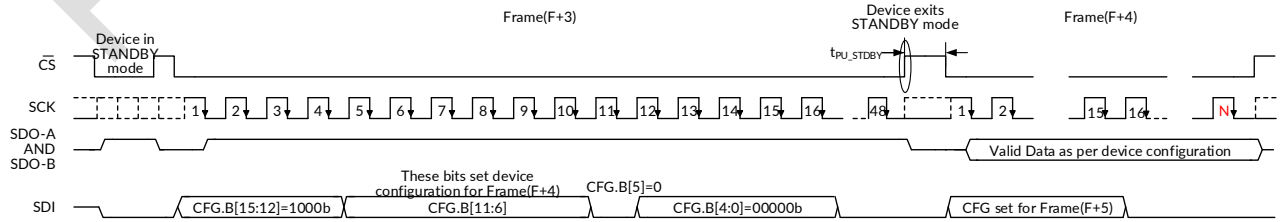


Figure 35. Enter STANDBY Mode

As shown in Figure 36, a valid write operation in frame (F+3) by writing the configuration register with B5 set to 0 (CFR.B5 = 0) brings the device out of STANDBY mode on the following $\overline{CS}$ rising edge. Frame (F+3) must have at least 48 SCLK falling edges.

After exiting the STANDBY mode, a delay of t_{PU_STDBY} must elapse for the internal circuits to fully power-up and resume normal operation in frame (F+4). Device configuration for frame (F+4) is determined by the status of the CFR.B[11:6] bits programmed during frame (F+3).



Note that N is a function of the device configuration, as described in Table 4.

Figure 36. Exit STANDBY Mode

Refer to the Timing Characteristics: Serial Interface for timing specifications for this operating mode.

8.5.4.2 Software Power-Down (SPD) Mode

In software power-down (SPD) mode, all internal circuits (including the internal references) are powered down. However, the contents of the REFDAC_A and REFDAC_B registers are retained.

As shown in Figure 37, to enter SPD mode, the device must be selected (by bringing $\overline{CS}$ low) and SDI must be kept high for a minimum of 48 SCLK cycles during frame (F). The device goes to SPD on the $\overline{CS}$ rising edge following frame (F). While in SPD mode, SDO_A and SDO_B go to 3-state irrespective of the status of the $\overline{CS}$ signal.

To remain in SPD mode, SDI must remain high in subsequent frames.

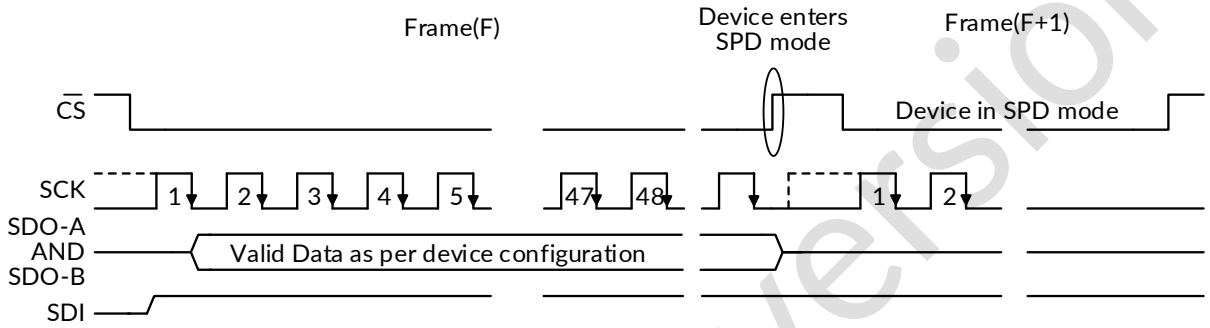
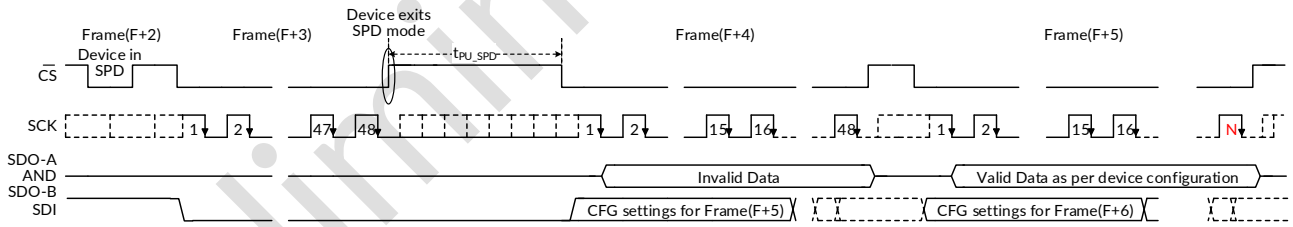


Figure 37. Enter SPD Mode

As shown in Figure 38, to exit SPD mode, the device must be selected (by bringing $\overline{CS}$ low) and SDI must be kept low for a minimum of 48 SCLK cycles during frame (F+3). The device starts powering-up on a $\overline{CS}$ rising edge following frame (F+3). After frame (F+3), a delay of t_{PU_SPD} must elapse before programming the configuration register.

A valid write operation in frame (F+4) sets the device configuration for frame (F+5). Frame (F+4) must have at least 48 SCLK falling edges. The output data in frame (F+4) should be discarded.



Note that N is a function of the device configuration, as described in Table 4.

Figure 38. Exit SPD Mode

Refer to the Timing Characteristics: Serial Interface for timing specifications for this operating mode.

9 APPLICATION AND IMPLEMENTATION

Information in the following applications sections is not part of the RUNIC component specification, and RUNIC does not warrant its accuracy or completeness. RUNIC's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The two primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR), analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section details some general principles for designing these circuits, and some application circuits designed using these devices.

The device supports operation with either an internal or external reference source. Refer to the Reference section for details about the decoupling requirements.

The reference source to the ADC must provide low-drift and very accurate dc voltage and support the dynamic charge requirements without affecting the noise and linearity performance of the device. The output broadband noise (typically in the order of a few 100 μV_{RMS}) of the reference source must be appropriately filtered by using a low-pass filter with a cutoff frequency of a few hundred hertz. After band-limiting the noise from the reference source, the next important step is to design a reference buffer that can drive the dynamic load posed by the reference input of the ADC. At the start of each conversion, the reference buffer must regulate the voltage of the reference pin within 1 LSB of the intended value. This condition necessitates the use of a large filter capacitor at the reference pin of the ADC. The amplifier selected to drive the reference input pin must be stable while driving this large capacitor and should have low output impedance, low offset, and temperature drift specifications. To reduce the dynamic current requirements and crosstalk between the channels, a separate reference buffer is recommended for driving the reference input of each ADC channel.

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and a fly-wheel RC filter. The amplifier is used for signal conditioning of the input voltage and its low output impedance provides a buffer between the signal source and the switched capacitor inputs of the ADC. The RC filter helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC and functions as an antialiasing filter to band-limit the wideband noise contributed by the front-end circuit. Careful design of the front-end circuit is critical to meet the linearity and noise performance of a high-precision ADC.

9.1.1 Input Amplifier Selection

Selection criteria for the input amplifiers is highly dependent on the input signal type and the performance goals of the data acquisition system. Some key amplifier specifications to consider while selecting an appropriate amplifier to drive the inputs of the ADC are:

- Small-signal bandwidth. Select the small-signal bandwidth of the input amplifiers to be as high as possible after meeting the power budget of the system. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive the low cutoff frequency RC filter at the ADC inputs. Higher bandwidth also minimizes the harmonic distortion at higher input frequencies. In order to maintain the overall stability of the input driver circuit, the amplifier bandwidth should be selected as described in Equation 8:

$$\text{Unity-Gain Bandwidth} \geq 4 \times \left(\frac{1}{2\pi \times (R_{FLT}+R_{FLT}) * C_{FLT}} \right) \quad (8)$$

- Noise. Noise contribution of the front-end amplifiers should be as low as possible to prevent any degradation in SNR performance of the system. As a rule of thumb, to ensure that the noise performance of the data acquisition system is not limited by the front-end circuit, the total noise contribution from the front-end circuit should be kept below 20% of the input-referred noise of the ADC. Noise from the input driver circuit is band-limited by designing a low cutoff frequency RC filter and is calculated by Equation 9:

$$N_G \times \sqrt{2} \times \sqrt{\left(\frac{V_{1/f\_AMP\_PP}}{6.6}\right)^2 + e_{n\_RMS}^2 \times \frac{\pi}{2} \times f_{-3dB}} \le \frac{1}{5} \times \frac{V_{REF}}{\sqrt{2}} \times 10^{-\left(\frac{SNR(dB)}{20}\right)} \quad (9)$$

where:

- V_{1/f_AMP_PP} is the peak-to-peak flicker noise in µV.
- e_{n_RMS} is the amplifier broadband noise density in nV/√Hz.
- f_{-3dB} is the 3dB bandwidth of the RC filter.
- NG is the noise gain of the front-end circuit, which is equal to 1 in a buffer configuration.

- Distortion. Both the ADC and the input driver introduce nonlinearity in a data acquisition block. As a rule of thumb, to ensure that the distortion performance of the data acquisition system is not limited by the front-end circuit, the distortion of the input driver should be at least 10dB lower than the distortion of the ADC, as shown in 10:

$$THD_{AMP} \le THD_{ADC} - 10\ (dB) \quad (10)$$

- Settling Time. For dc signals with fast transients that are common in a multiplexed application, the input signal must settle to the desired accuracy at the inputs of the ADC during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC.

9.1.2 Antialiasing Filter

Converting analog-to-digital signals requires sampling an input signal at a constant rate. Any higher frequency content in the input signal beyond half the sampling frequency is digitized and folded back into the low-frequency spectrum. This process is called aliasing. Therefore, an analog, antialiasing filter must be used to remove the harmonic content from the input signal before being sampled by the ADC. An antialiasing filter is designed as a low-pass, RC filter, for which the 3 dB bandwidth is optimized based on specific application requirements. For dc signals with fast transients (including multiplexed input signals), a high-bandwidth filter is designed to allow accurately settling the signal at the ADC inputs during the small acquisition time window. For ac signals, the filter bandwidth should be kept low to band-limit the noise fed into the ADC input, thereby increasing the signal-to- noise ratio (SNR) of the system.

A filter capacitor, C_{FLT}, connected across the ADC inputs (as shown in Figure 39), filters the noise from the front-end drive circuitry, reduces the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. As a rule of thumb, the value of this capacitor should be at least 10 times the specified value of the ADC sampling capacitance. For these devices, the input sampling capacitance is equal to 40 pF. Thus, the value of CFLT should be greater than 400 pF. The capacitor should be a COG or NPO type because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.

Note that driving capacitive loads can degrade the phase margin of the input amplifiers, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors (R_{FLT}) are used at the output of the amplifiers. A higher value of R_{FLT} is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability and distortion of the design. RS recommends limiting the value of R_{FLT} to a maximum of 22 Ω in order to avoid any significant degradation in linearity performance. The tolerance of the selected resistors can be chosen as 1% because the use of a differential capacitor at the input balances the effects resulting from any resistor mismatch.

$$f_{-dB} = \frac{1}{2\pi \times (R_{FLT} + R_{FLT}) \times C_{FLT}}$$

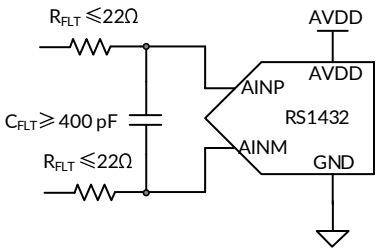


Figure 39. Antialiasing Filter

The input amplifier bandwidth should be much higher than the cutoff frequency of the antialiasing filter. If an amplifier has less than a 40° phase margin with 22 Ω resistors, using a different amplifier with higher bandwidth or reducing the filter cutoff frequency with a larger differential capacitor is advisable.

9.2 Typical Applications

9.2.1 DAQ Circuit to Achieve Maximum SINAD for a Input Signal at Full Throughput

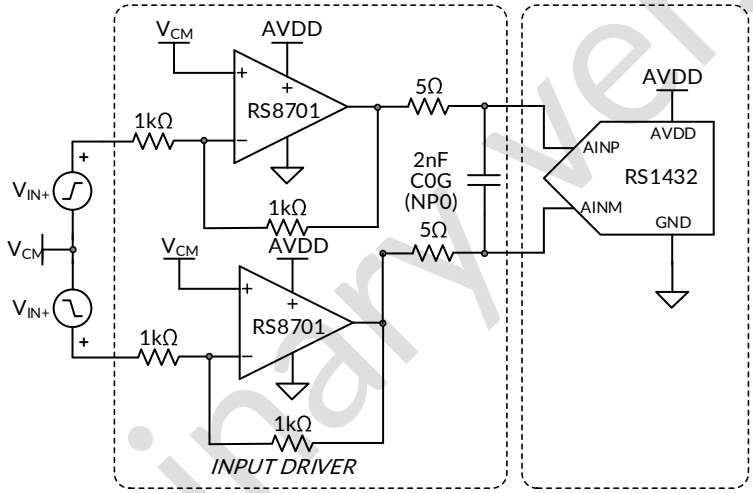
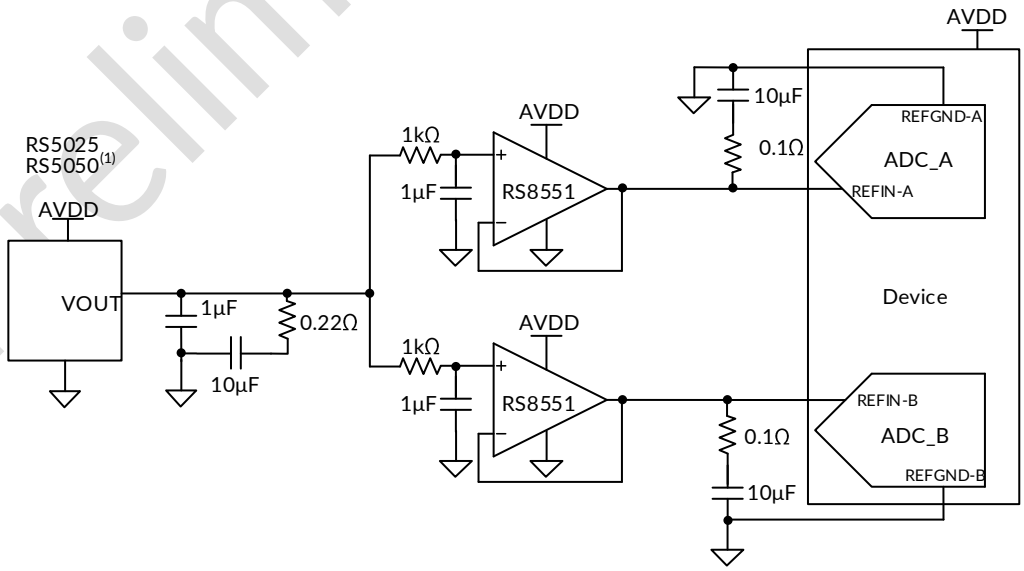


Figure 40. DAQ Circuit: Maximum SINAD for a Input Signal at Full Throughput



(1) When using the RS5050, AVDD must be set to 5.5 V.

Figure 41. Reference Drive Circuit

9.2.1.1 Detailed Design Procedure

Best practices require that the distortion generated by the input driver be at least 10 dB lower than the ADC's distortion. By employing an amplifier in an inverting gain configuration, distortion caused by common-mode signal variations can be eliminated, as this configuration establishes a fixed common-mode level for the circuit. This structure also eliminates the requirement for the amplifier input to achieve rail-to-rail swing. When using the low-power RS8701XF as the input driver, its extremely low distortion and high bandwidth characteristics deliver excellent AC performance.

Additionally, the components of the anti-aliasing filter are optimally designed to suppress noise from the front-end circuit without introducing additional distortion to the input signal. The application circuit shown in Figure 40 is optimized for a input signal, achieving the lowest distortion and noise when the RS1432 operates at its full throughput rate in the default 32-clock cycle, dual SDO interface mode. The input signal is first processed by a high-bandwidth, low-distortion amplifier configured for inverting gain, along with a low-pass RC filter, before being fed into the device.

The 16-clock cycle interface mode is also supported, which allows the rated throughput to be achieved at a lower serial clock frequency. The application circuit shown in Figure 40 is optimized for a input signal, achieving the lowest distortion and noise when the RS1432 operates at its full throughput rate in the 16-clock cycle, dual SDO interface mode. Similarly, the input signal must be processed by a high-bandwidth, low-distortion inverting amplifier circuit and a low-pass RC filter.

Figure 41 shows the reference driver circuit when using an external voltage reference. The reference voltage is generated by the high-precision, low-noise RS50xx, whose output broadband noise is deeply filtered by a low-pass filter with a cutoff frequency of 160 Hz. A 1 μF decoupling capacitor is selected for each reference pin. The RS8551XF, with its low output impedance, low noise, and fast settling characteristics, is an ideal choice for driving this highly capacitive load.

9.2.1.2 Application Curves

To minimize external components and maximize the ADC's dynamic range, the device is configured to operate using an internal reference (CFR.B6 = 1) with a 2 × V_{REF_x} input full-scale range (CFR.B9 = 1).

Figure 42, Figure 44 shows the corresponding FFT plots and test results obtained under full throughput operation with a 32-CLK interface, using the circuit configuration shown in Figure 40.

Figure 43, Figure 45 shows the corresponding FFT plots and test results obtained under full throughput operation with a 16-CLK interface, using the circuit configuration shown in Figure 40.

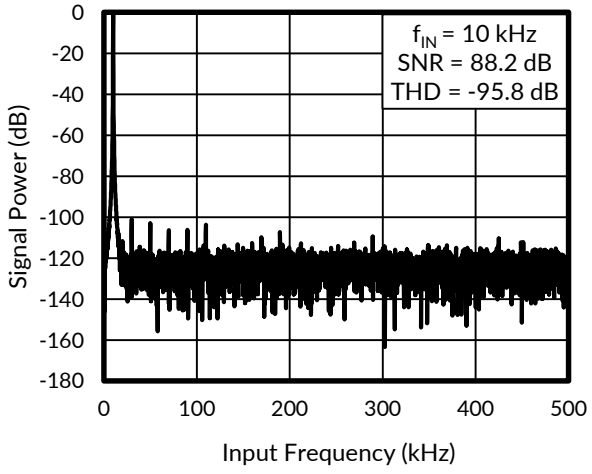


Figure 42. 32-CLK Interface Mode

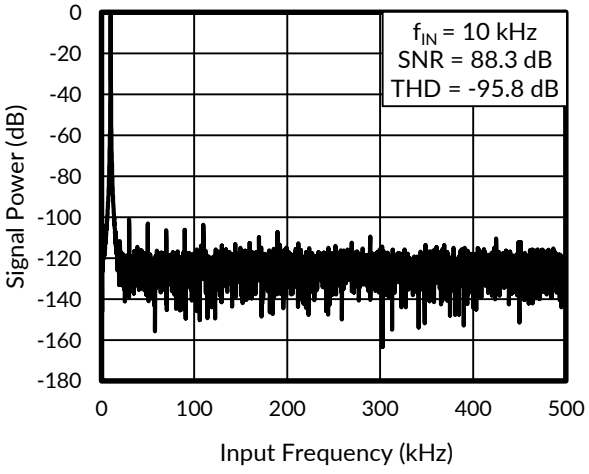


Figure 43. 16-CLK Interface Mode

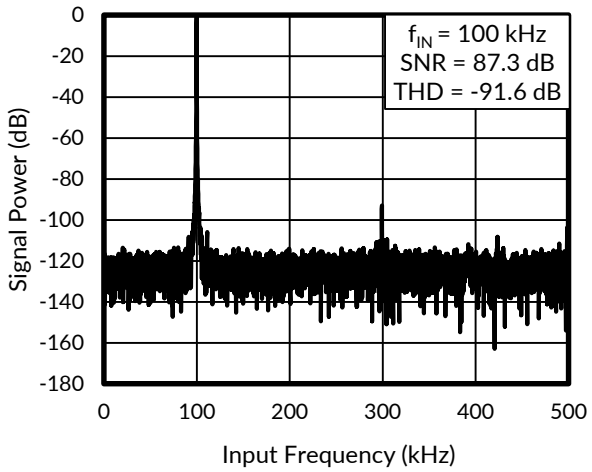


Figure 44. 32-CLK Interface Mode

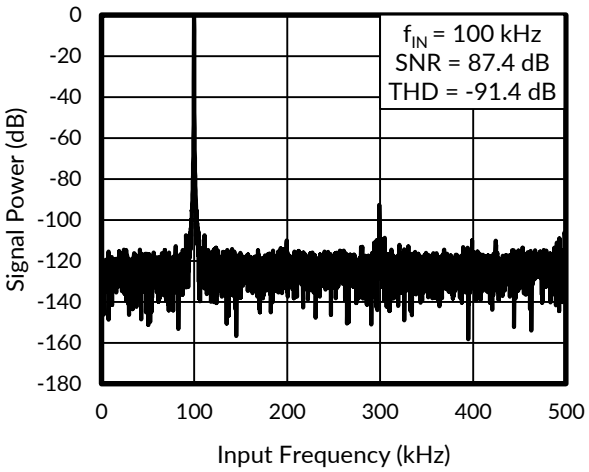


Figure 45. 16-CLK Interface Mode

10 POWER-SUPPLY RECOMMENDATIONS

The devices have two separate power supplies: AVDD and DVDD. The device operates on AVDD; DVDD is used for the interface circuits. AVDD and DVDD can be independently set to any value within the permissible ranges.

When using the device with 2 × V_{REF} input range (CFR.B9 = 1), the AVDD supply voltage value defines the permissible voltage swing on the analog input pins. To avoid saturation of output codes, and to use the full dynamic range on the analog input pins, AVDD must be set as shown in Equation 11, Equation 12, and Equation 13:

$$AVDD \geq 2 \times V_{REF\_A} \quad (11)$$

$$AVDD \geq 2 \times V_{REF\_B} \quad (12)$$

$$4.75\ V \leq AVDD \leq 5.25\ V \quad (13)$$

Decouple the AVDD and DVDD pins with the GND pin using individual 10 µF decoupling capacitors, as shown in Figure 46.

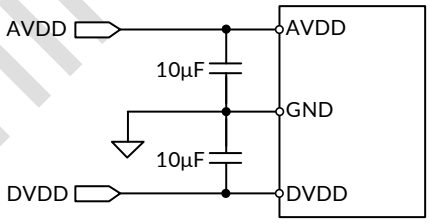


Figure 46. Power-Supply Decoupling

11 LAYOUT

11.1 Layout Guidelines

Figure 47 shows a board layout example for the RS1432 with the TSSOP package. Use a ground plane underneath the device and partition the PCB into analog and digital sections. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources. As shown in Figure 47, the analog input and reference signals are routed on the left side of the board and the digital connections are routed on the right side of the device.

The power supply to the device must be clean and well-decoupled. Place 10 µF ceramic bypass capacitors close to the analog (AVDD) and digital (DVDD) power supply pins, and avoid placing vias between the power pins and the bypass capacitors. All ground pins should be connected to the ground plane via short, low-impedance paths.

The REFIO-A and REFIO-B reference inputs and outputs are bypassed with 10 µF, X7R grade, 0805 size, 16V rated ceramic capacitors (C_{REF-x}). Place the reference bypass capacitors as close as possible to the reference REFIO-x pins and connect the bypass capacitors using short, low-inductance connections. Avoid placing vias between the REFIO-x pins and the bypass capacitors. Small 0.1 Ω to 0.2 Ω resistors (R_{REF-x}) are used in series with the reference bypass capacitors to improve stability.

The fly-wheel RC filters are placed immediately next to the input pins. Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes. Figure 47 shows C_{IN-A} and C_{IN-B} filter capacitors placed across the analog input pins of the device.

11.2 Layout Example

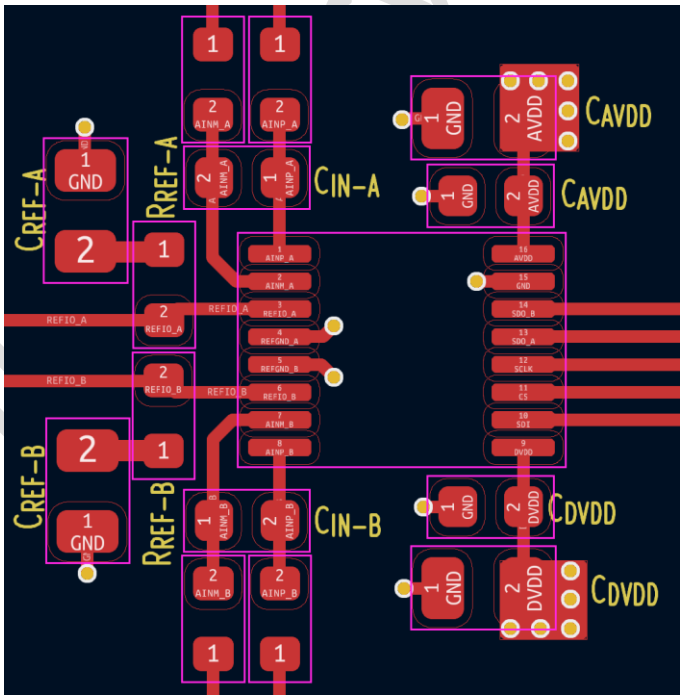
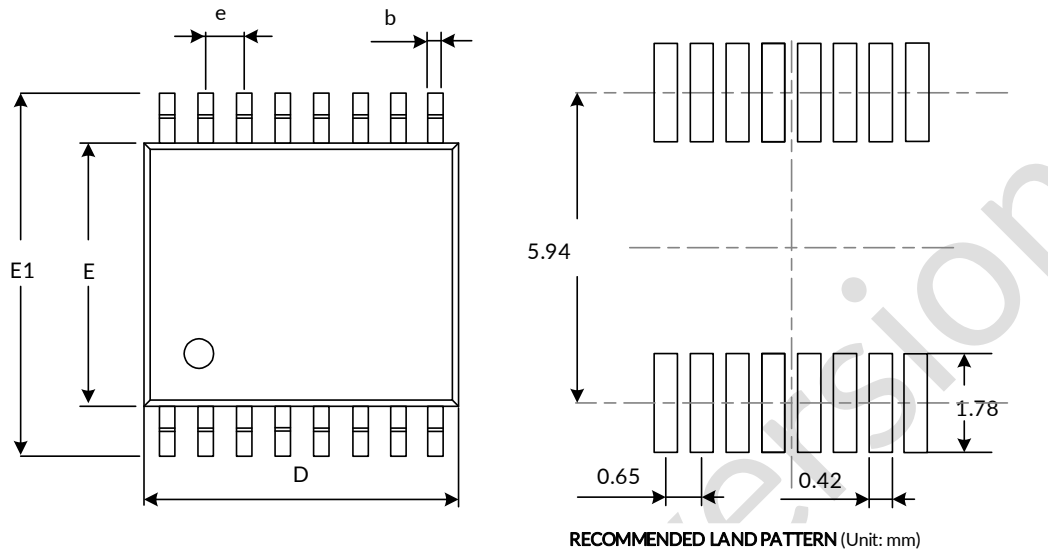


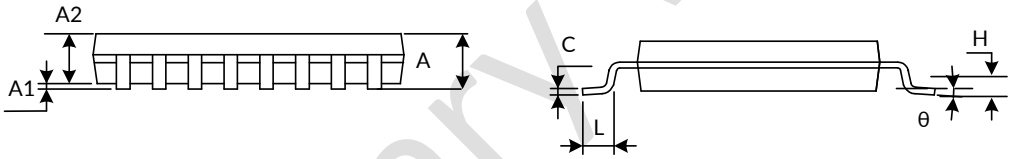
Figure 47. Recommended Layout

12 PACKAGE OUTLINE DIMENSIONS

TSSOP16 (3)



RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D (1)	4.860	5.100	0.191	0.201
E (1)	4.300	4.500	0.169	0.177
E1	6.200	6.600	0.244	0.260
e	0.650 (BSC) (2)		0.026 (BSC) (2)	
L	0.500	0.700	0.020	0.028
H	0.250 TYP		0.010 TYP	
θ	1°	7°	1°	7°

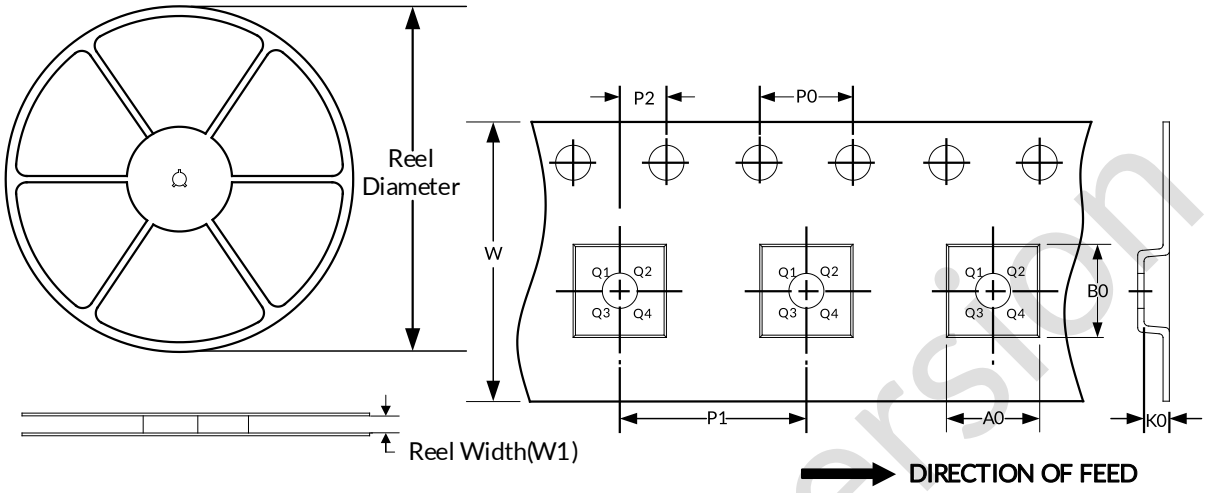
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

13 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP16	13”	12.4	6.90	5.60	1.20	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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