300mA, Low Power Consumption, High Voltage CMOS LDO Regulator

1 FEATURES

- **RS3015-Q1 AEC-Q100 Qualification is Ongoing**
- **Input Voltage Range: 3 V to 45 V**
- **Output Voltage Range:**
  - Fixed Option: 2.5V, 3.3V and 5.0V
- **Very low I_Q: 3μA (TYP)**
- **Up to 300mA Load Current**
- **Low Dropout Voltage**
- **Low Temperature Coefficient**
- **Current Limit Protection**
- **Over Temperature Protection**
- **Output Voltage Accuracy: ±1%**
- **SOT23-5, SOT-223, EMSOP8 and DFN2X2-6 Packages**

2 APPLICATIONS

- **Smart Power Network Equipment**
- **Portable Power Tools**
- **BMS Systems**
- **Motor Control System/Industrial Control System**
- **Power Meter/Instrument**
- **White Goods**
- **Vehicle-Mounted System**
- **Battery-Powered Equipment**
- **Automotive Head Unit**
- **Security Equipment**
- **Communication Equipment**

3 DESCRIPTIONS

The RS3015-Q1 series is a Low Dropout Linear Regulator designed by CMOS technology. Which can provide 300 mA output current. The device allows input voltage as high as 45 V. It is very suitable for multi-cell battery systems, bus voltage power supply systems, Vehicle battery power supply system and other high DC voltage systems. Wide input voltage can make it well withstand the impact of surge voltage and ensure the stability of output voltage.

The RS3015-Q1 series only consume 3μA (typical), Which is particularly important in battery power system, can reduce the standby power consumption of the whole system.

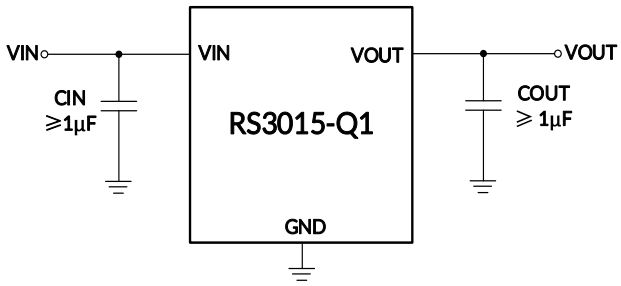
The RS3015-Q1 is available in Green SOT23-5, SOT-223, EMSOP8 and DFN2X2-6 variety of packages, for the different application's requirements.

Device Information (1)

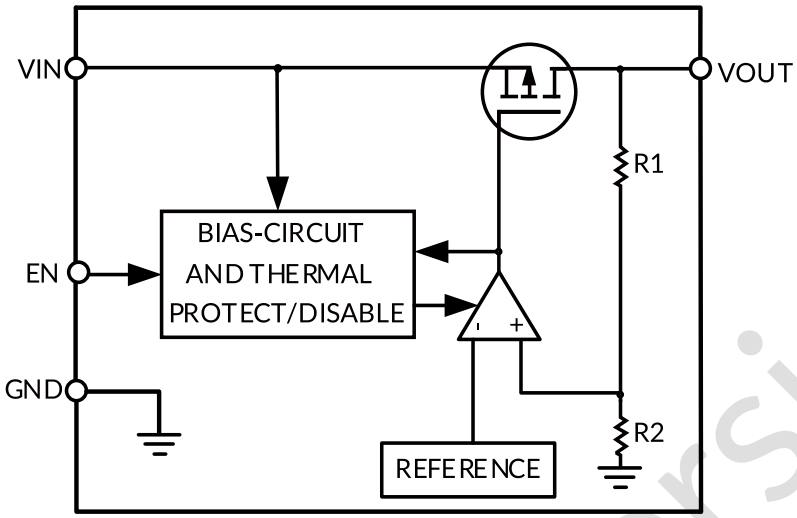
PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS3015-Q1	SOT23-5	1.60mm×2.92mm
	SOT-223	3.50mm×7.00mm
	EMSOP8	3.00mm×3.00mm
	DFN2X2-6	2.00mm×2.00mm

(1) For all available packages, see the orderable addendum at the next page of the data sheet.

4 TYPICAL APPLICATION SCHEMATIC



5 FUNCTIONAL BLOCK DIAGRAM



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6 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2025/08/25	Preliminary version completed
A.0.1	2025/12/25	1. Update Electrical Characteristics 2. Add DFN2X2-6 and EMSOP8 packages 3. Delete SOT23-3, SOT89-3 and SOT89-3L packages

7 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	Lead finish/Ball material (2)	MSL Peak Temp (3)	PACKAGE MARKING (4)	PACKAGE OPTION
RS3015-2.5-Q1	RS3015-2.5XF5-Q1	-40°C ~125°C	SOT23-5	TBD	TBD	SF25	Tape and Reel, 3000
	RS3015-2.5XD3-Q1	-40°C ~125°C	SOT-223	TBD	TBD	SF25	Tape and Reel, 2500
	RS3015-2.5XEM-Q1	-40°C ~125°C	EMSOP8	TBD	TBD	SF25	Tape and Reel, 4000
	RS3015-2.5XTDE6-Q1	-40°C ~125°C	DFN2X2-6	TBD	TBD	SF25	Tape and Reel, 3000
RS3015-3.3-Q1	RS3015-3.3XF5-Q1	-40°C ~125°C	SOT23-5	TBD	TBD	SF33	Tape and Reel, 3000
	RS3015-3.3XD3-Q1	-40°C ~125°C	SOT-223	TBD	TBD	SF33	Tape and Reel, 2500
	RS3015-3.3XEM-Q1	-40°C ~125°C	EMSOP8	TBD	TBD	SF33	Tape and Reel, 4000
	RS3015-3.3XTDE6-Q1	-40°C ~125°C	DFN2X2-6	TBD	TBD	SF33	Tape and Reel, 3000
RS3015-5.0-Q1	RS3015-5.0XF5-Q1	-40°C ~125°C	SOT23-5	TBD	TBD	SF50	Tape and Reel, 3000
	RS3015-5.0XD3-Q1	-40°C ~125°C	SOT-223	TBD	TBD	SF50	Tape and Reel, 2500
	RS3015-5.0XEM-Q1	-40°C ~125°C	EMSOP8	TBD	TBD	SF50	Tape and Reel, 4000
	RS3015-5.0XTDE6-Q1	-40°C ~125°C	DFN2X2-6	TBD	TBD	SF50	Tape and Reel, 3000

NOTE:

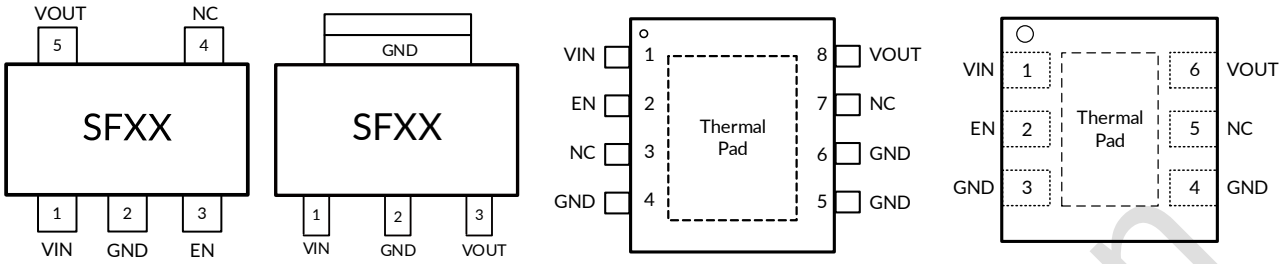
(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) Lead finish/Ball material. Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

(4) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

8 PIN CONFIGURATION AND FUNCTIONS (TOP VIEW)



NOTE: XX indicate Output Voltage, xx indicate Date Code
For example: SF33(V_{OUT}=3.3V)

PIN DESCRIPTION

NAME	PIN				FUNCTION
	SOT23-5	SOT-223	EMSOP8	DFN2X2-6	
GND	2	2	4, 5, 6	3, 4	Ground
VOUT	5	3	8	6	Regulated output voltage. Connect a minimum 1μF low-ESR capacitor to this pin.
VIN	1	1	1	1	Input voltage supply. Must be closely decoupled to GND with a 1μF or greater capacitor.
EN	3	/	2	2	Enable input. A low voltage (< V_{IL}) on this pin turns the regulator off. A high voltage (> V_{IH}) on this pin enables the regulator output. The EN pin can be connected to the VIN pin if not used. Do not leave floating.
NC	4	/	3, 7	5	No internal connection
-	/	/	Thermal pad	Thermal pad	Connect the thermal pad to a large-area GND plane for improved thermal performance.

9 SPECIFICATIONS

9.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

			MIN	MAX	UNIT
V_{IN}	Input voltage		-0.3	55	V
V_{EN}	V_{EN} voltage range		-0.3	V_{IN}	V
V_{OUT}	V_{OUT} voltage range		-0.3	7	V
T_J	PN Junction temperature (3)		-40	150	°C
P_D	Continuous power dissipation (4)		Internally limited		W
θ_{JA}	Package thermal impedance (5)	SOT23-5		160	°C/W
		SOT-223		100	
		DFN2X2-6		TBD	
		EMSOP8		TBD	
θ_{JC}	Junction-to-case (top) thermal resistance	SOT23-5		95	°C/W
		SOT-223		70	
		DFN2X2-6		TBD	
		EMSOP8		TBD	
T_{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to the GND pin.

(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

(4) Internal thermal shutdown circuitry protects the device from permanent damage. The actual chip output current is subject to the input-output voltage difference, ambient temperature and PCB heat dissipation design.

(5) The package thermal impedance is calculated in accordance with JESD-51.

9.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), per AEC Q100-002 (1)	TBD	V
		Charged-Device Model (CDM), per AEC Q100-011	TBD	V
		Latch-Up (LU), per AEC Q100-004	TBD	mA

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input Voltage Range on VIN	3	45	V
V_{EN}	Input Voltage Range on EN	0	V_{IN}	V
I_{OUT}	Output Current Range on IOUT	0	300	mA
C_{OUT}	Output Capacitor Range	1	10	μF
T_A	Operating Ambient Temperature Range	-40	125	°C
T_J	PN Junction Temperature	-40	150	°C

9.4 Electrical Characteristics

Over operating temperature range (−40°C ≤ T_A ≤ 125°C), V_{IN} = V_{OUT}nom + 2V [1], C_{IN} =C_{OUT} = 1μF, V_{OUT}=3.3V, unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER	SYMBOL	CONDITIONS		MIN[2]	TYP[3]	MAX[2]	UNIT
POWER SUPPLY AND CURRENTS							
Input Voltage [1]	V_{IN}			3		45	V
Under Voltage Lockout	UVLO	VIN rising		2.05	2.55	2.95	V
Hysteresis	V_{HYS}	VIN falling		75	125	200	mV
Quiescent Current	I_Q	V_{EN} = 1.7V, I_{OUT} = 0mA			3	12	μA
Shutdown Current	I_{SD}	V_{EN} = 0V				1	μA
OUTPUT VOLTAGE							
Output Voltage Range	V_{OUT}			2.5		5.0	V
DC Output Accuracy [1]	ΔV_{OUT}	T_J = 25°C, I_{OUT} = 1mA		-1		1	%
Line Regulation [1]	$\Delta V_{OUT(\Delta VIN)}$	V_{IN} = V_{OUT} + 2V to 45V, I_{OUT} = 1mA			2	4.5	mV
Load Regulation [1]	$\Delta V_{OUT(\Delta IOUT)}$	V_{IN} =V_{OUT} + 2V, I_{OUT} = 1mA to 300mA			20	40	mV
Maximum output current [4]	I_{OUTMAX}			300			mA
DROPOUT VOLTAGE							
Dropout Voltage [5]	V_{DO}	I_{OUT} = 300mA	V_{OUT} = 2.5V		TBD		mV
			V_{OUT} = 3.3V		1150	2100	
			V_{OUT} = 5.0V		1030	2100	
POWER SUPPLY REJECTION RATIO AND NOISE							
Power Supply Rejection Ratio [6]	PSRR	V_{OUT} = 3.3V, I_{OUT} = 10mA	f = 100Hz		60		dB
			f = 217Hz		60		dB
			f = 1KHz		58		dB
			f = 10KHz		53		dB
			f = 100KHz		45		dB
Output Noise Voltage [6]	V_N	BW = 10Hz ~ 100KHz, V_{OUT} = 3.3V, I_{OUT} = 300mA			120		μV_{RMS}
ENABLE AND STARTUP TIME							
EN Input Logic High Voltage	V_{IH}	V_{IN} = 3V to 45V, EN rising		1.7			V
EN Input Logic Low Voltage	V_{IL}	V_{IN} = 3V to 45V, EN falling				0.4	V
EN Input leakage current	I_{EN}	V_{IN} = 45, V_{EN} = 0V			0.01	0.1	μA
		V_{IN} = 45, V_{EN} = 45V			1.5	3	μA
PROTECTIONS							
Over Current Limit	I_{LMT}	V_{IN} = 14V, V_{OUT} = 0.9*V_{OUT}nom		350	550		mA
Thermal shutdown threshold [6]	T_{TSD}				165		°C
Thermal shutdown hysteresis [6]	T_{HYS}				20		°C

NOTE:

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 3V, whichever is greater.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

(4) Maximum output current is affected by the PCB layout, size of metal trace, the thermal conduction path between metal layers, ambient temperature and the other environment factors of system. Attention should be paid to the dropout voltage when V_{IN} < V_{OUT} + V_{DROP}.

(5) V_{DROP} FT test method: test the V_{OUT} voltage at V_{SET} +$V_{DROPMAX}$ with output current.

(6) Guaranteed by design and characterization, not a FT item.

9.5 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

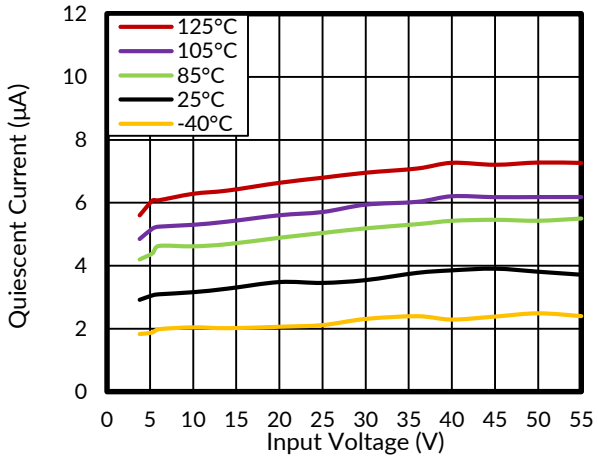


Figure 1. Quiescent Current vs Input Voltage

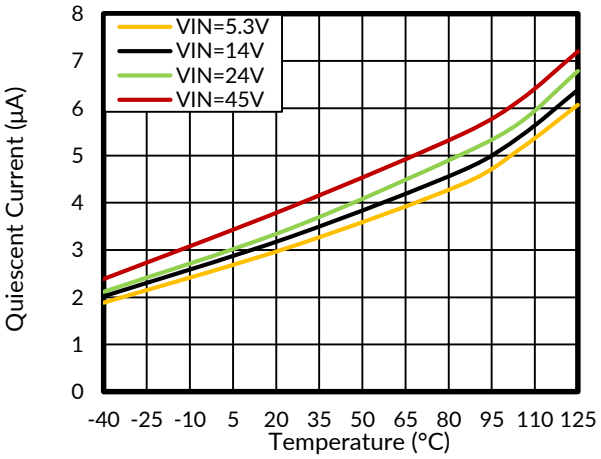


Figure 2. Quiescent Current vs Temperature

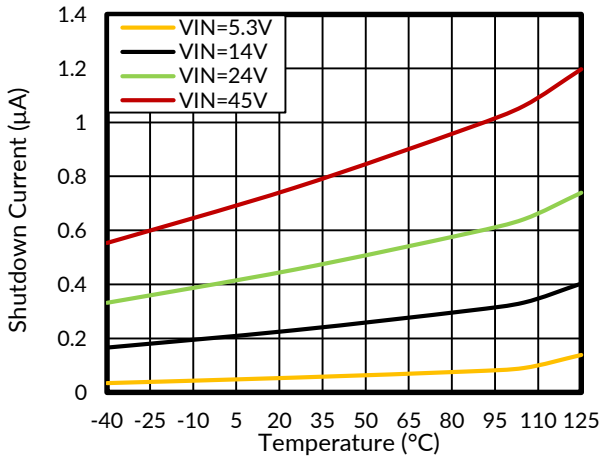


Figure 3. Shutdown Current vs Junction Temperature

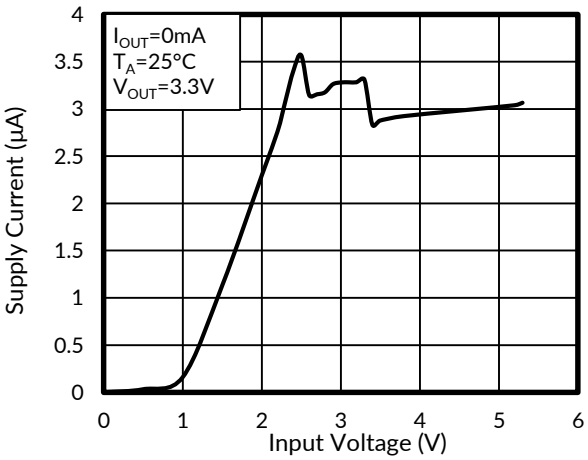


Figure 4. Supply Current vs Input Voltage

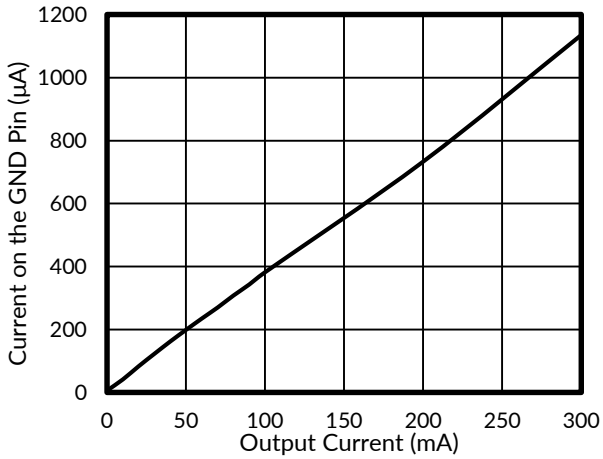


Figure 5. Ground Pin Current vs Output Current

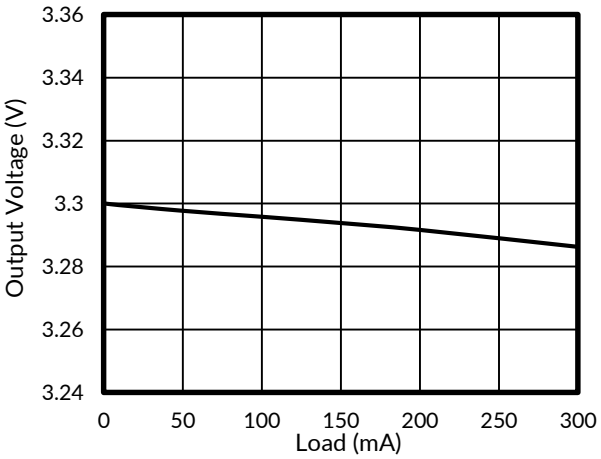


Figure 6. Load Regulation

Typical Characteristics

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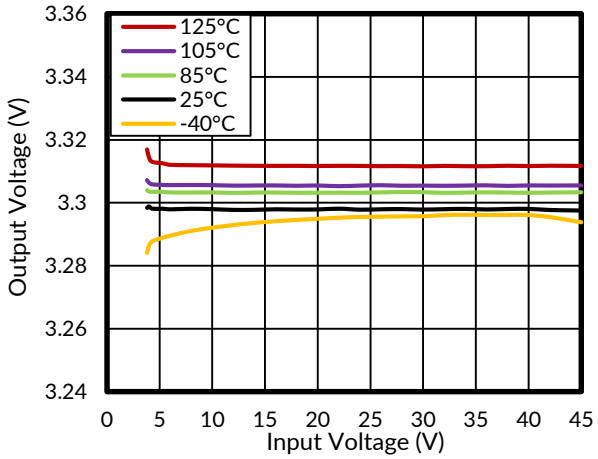


Figure 7. Line Regulation

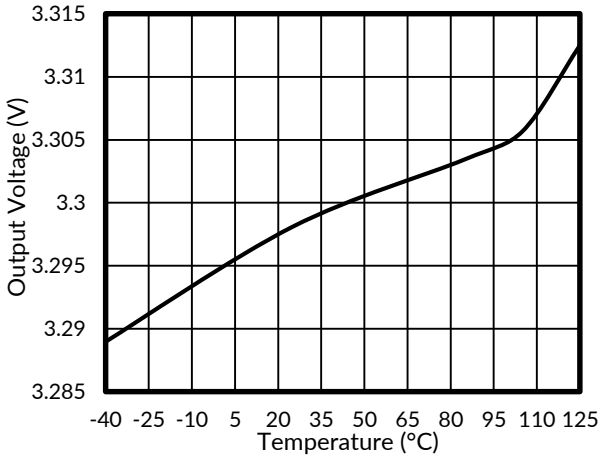


Figure 8. Output Voltage vs Junction Temperature

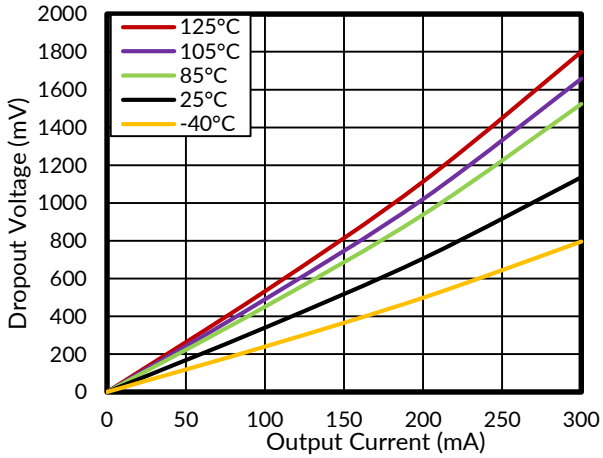


Figure 9. Dropout Voltage vs Output Current

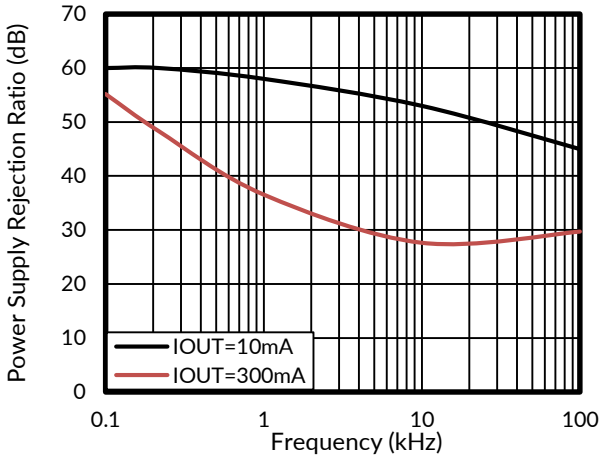


Figure 10. Power Supply Rejection Ratio vs Frequency

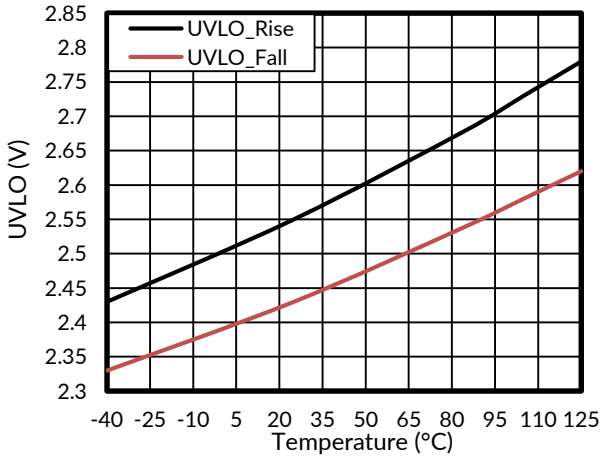


Figure 11. UVLO vs Junction Temperature

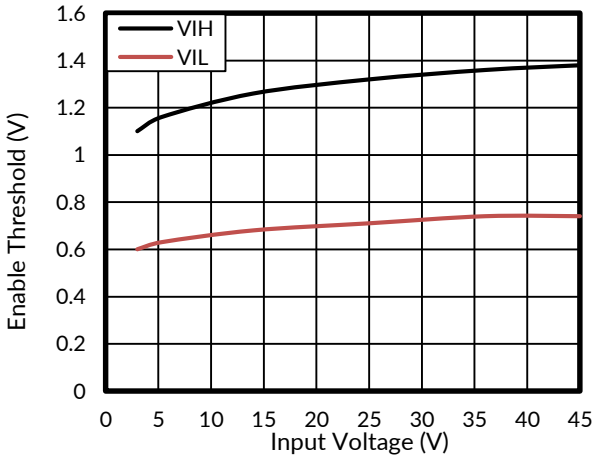


Figure 12. Enable Threshold vs Input Voltage

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

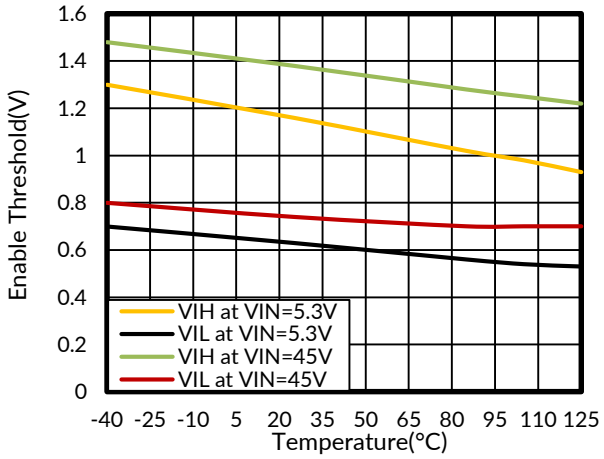


Figure 13. Enable Threshold vs Junction Temperature

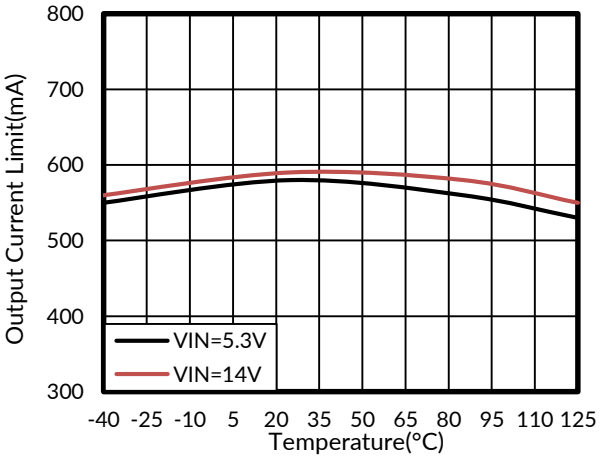


Figure 14. Output Current Limit vs Temperature

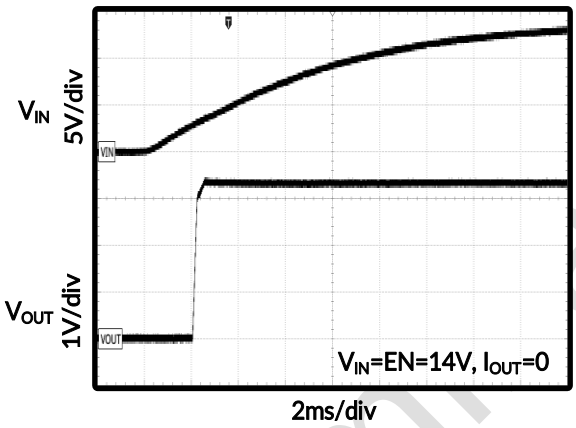


Figure 15. Power On

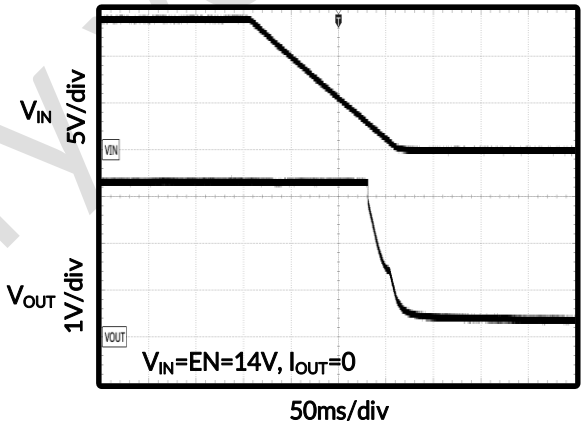


Figure 16. Power Off

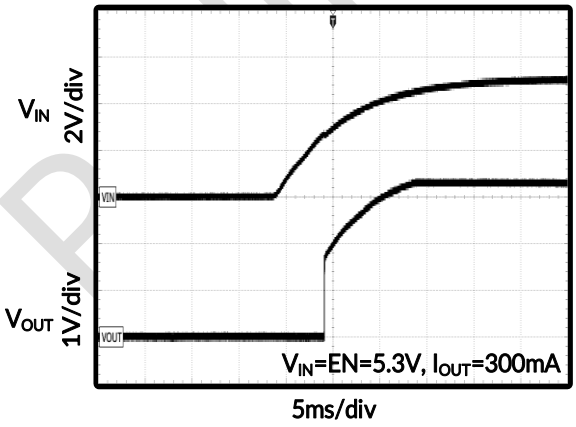


Figure 17. Power On

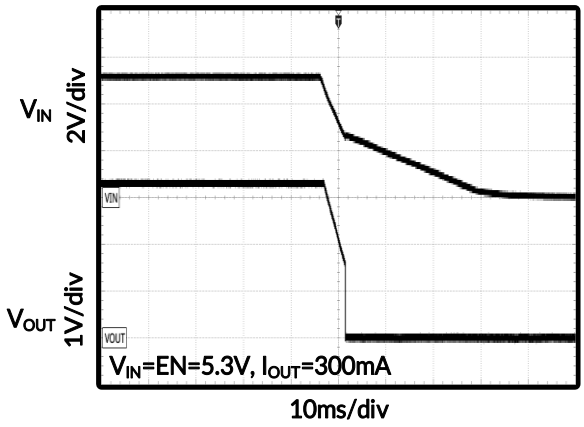


Figure 18. Power Off

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

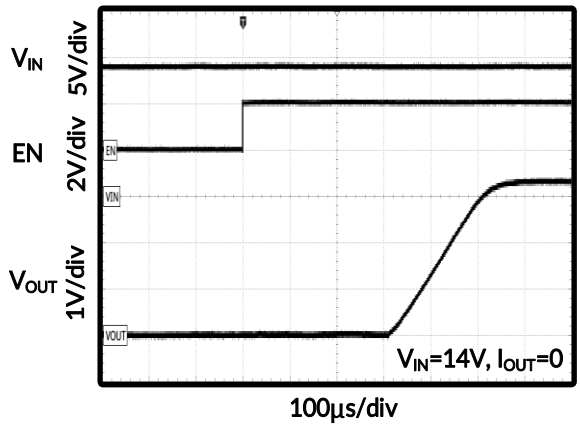


Figure 19. Turn On

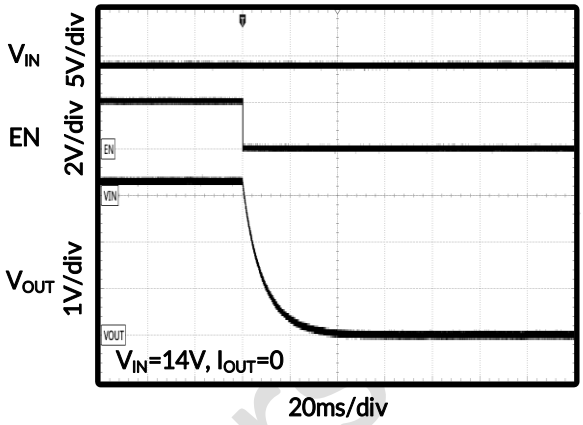


Figure 20. Turn Off

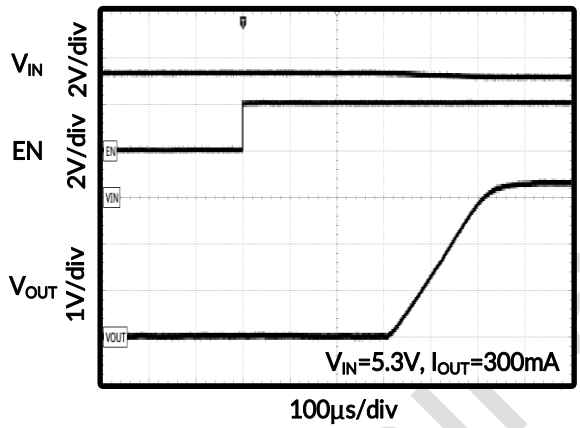


Figure 21. Turn On

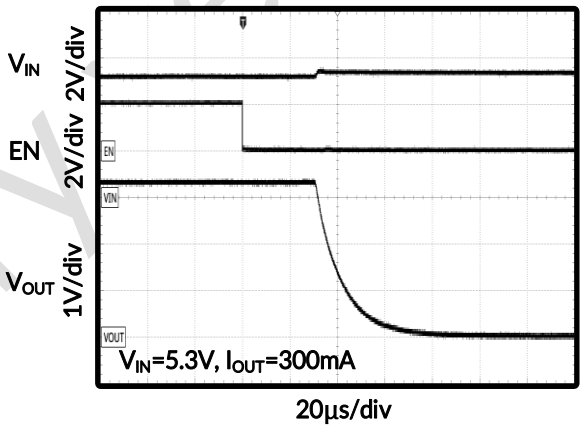


Figure 22. Turn Off

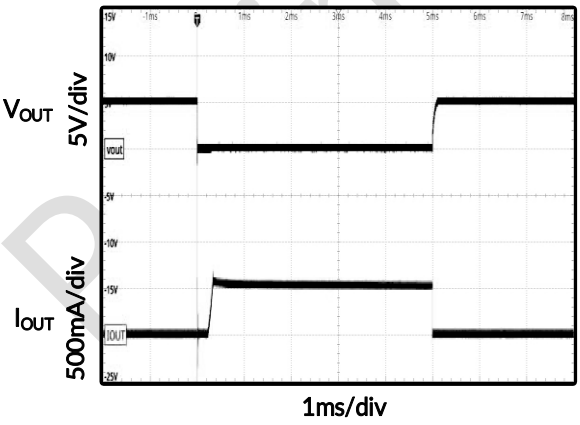


Figure 23. Turn On First, Then Short Circuit

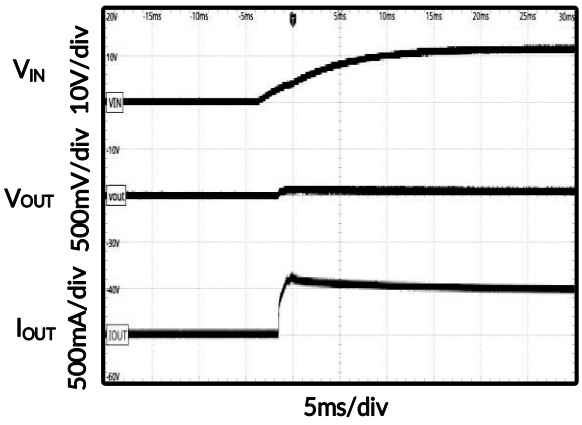


Figure 24. Short Circuit First, Then VIN Power ON

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

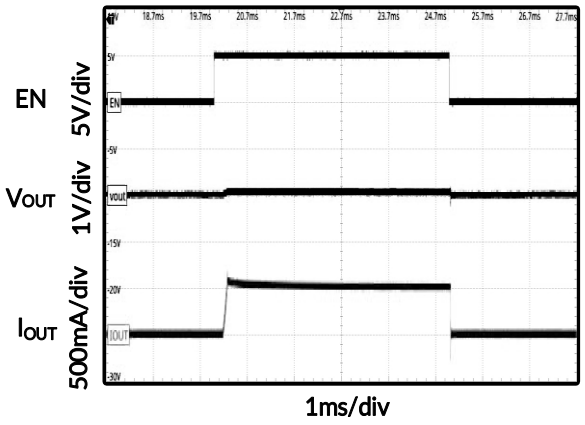


Figure 25. Short Circuit First, Then EN Turn ON

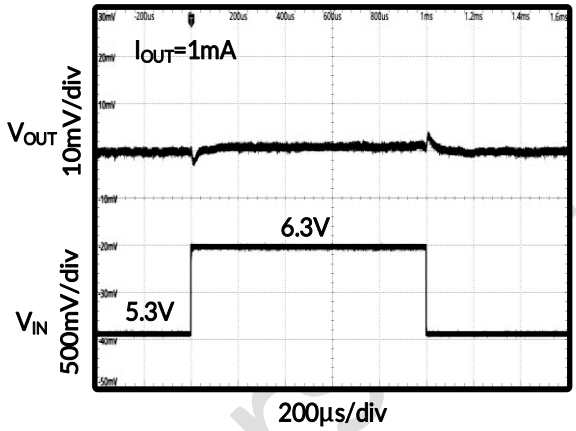


Figure 26. Line Transient Response

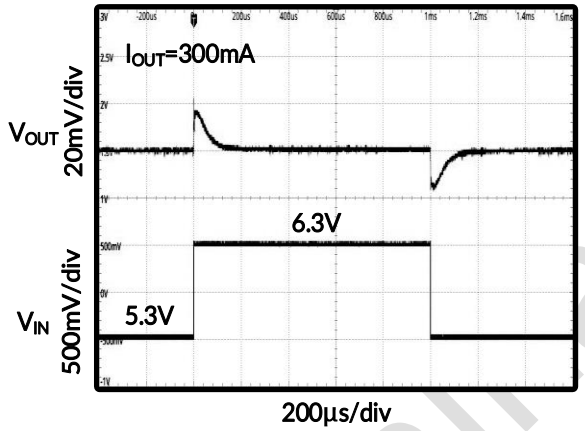


Figure 27. Line Transient Response

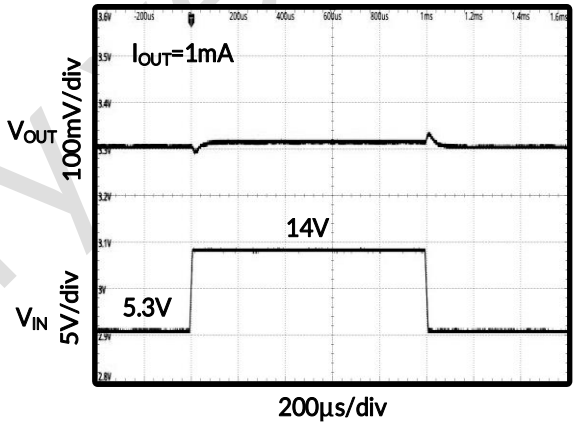


Figure 28. Line Transient Response

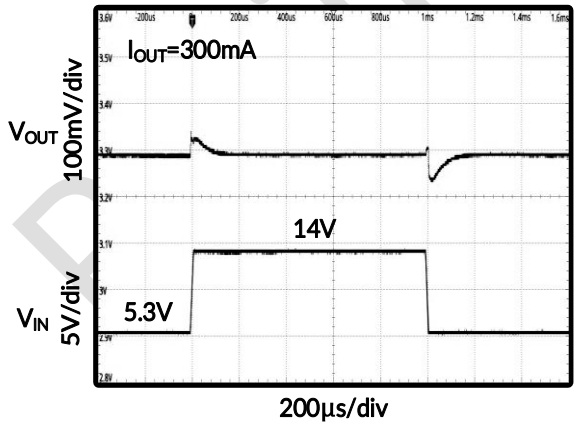


Figure 29. Line Transient Response

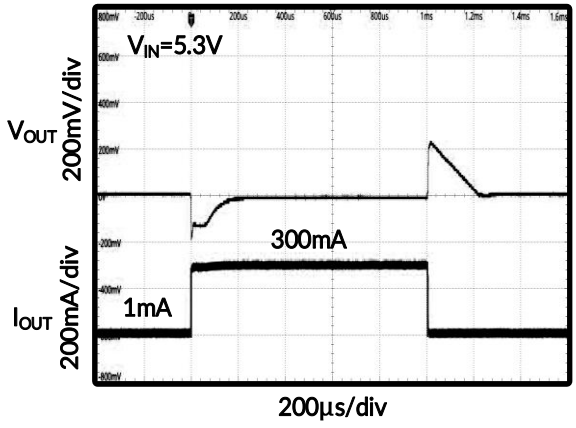


Figure 30. Load Transient Response

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

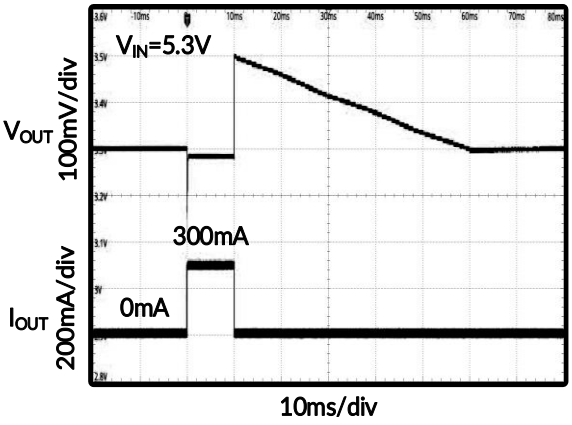


Figure 31. Load Transient Response

10 DETAILED DESCRIPTION

10.1 Overview

The RS3015-Q1 series is a Low Dropout Linear Regulator designed by CMOS technology. Which can provide 300 mA output current. The device allows input voltage as high as 45 V. It is very suitable for multi-cell battery systems, bus voltage power supply systems, Vehicle battery power supply system and other high DC voltage systems. Wide input voltage can make it well withstand the impact of surge voltage and ensure the stability of output voltage.

The RS3015-Q1 series only consume 3μA (typical), Which is particularly important in battery power system, can reduce the standby power consumption of the whole system.

10.2 Under Voltage Lockout (UVLO)

The RS3015-Q1 family of devices uses an under voltage lockout circuit to keep the output shut off until the internal circuitry is operating properly.

10.3 Shutdown

Enable input. A low voltage (< V_{IL}) on this pin turns the regulator off. A high voltage (> V_{IH}) on this pin enables the regulator output. The EN pin can be connected to the VIN pin if not used. Do not leave floating.

10.4 Thermal Overload Protection (T_{SD})

Thermal shutdown disables the output when the junction temperature rises to approximately 165°C which allows the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry enables.

Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The thermal shutdown circuitry of the RS3015-Q1 has been designed to protect against temporary thermal overload conditions. The T_{SD} circuitry was not intended to replace proper heat-sinking. Continuously running the RS3015-Q1 device into thermal shutdown may degrade device reliability.

10.5 Disabled

The device is disabled under the following conditions:

- The input voltage is less than the UVLO threshold minus V_{HYS}, or has not yet exceeded the UVLO threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

10.6 Current-Limit Protection

The RS3015-Q1 monitors the current flowing through the output PMOS and limits the maximum current to prevent load and RS3015-Q1 from damages during current overload conditions.

10.7 Input and Output Capacitor Requirements

Connecting a 1μF low-equivalent series resistance (ESR) capacitor across the input supply near the regulator is good analog design practice. This capacitor counteracts reactive input sources and improves transient response and ripple rejection. A higher value capacitor can be necessary if large, fast, rise-time load transients are anticipated or if the device is located several inches from the power source.

The RS3015-Q1 family of devices is designed to be stable with standard ceramic output capacitors of values 1μF or larger. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature.

11 POWER SUPPLY RECOMMENDATIONS

The device is designed to operate from an input voltage supply range between 3V and 45V. The input voltage range must provide adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve output noise.

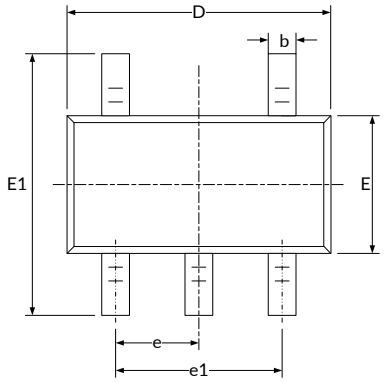
12 LAYOUT

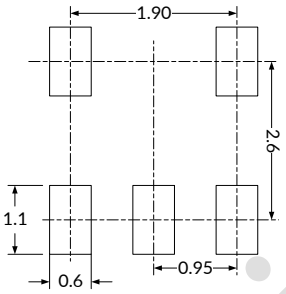
For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO component connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the printed circuit board (PCB) itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shields the LDO from noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the exposed thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

To improve ac performance (such as PSRR, output noise, and transient response), designing the board with separate ground planes for V_{IN} and V_{OUT} is recommended, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

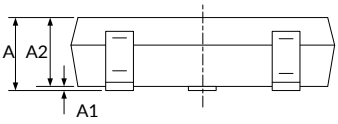
13 PACKAGE OUTLINE DIMENSIONS

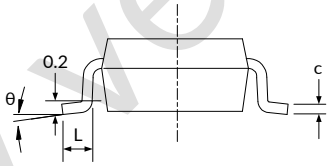
SOT23-5 (3)





RECOMMENDED LAND PATTERN (Unit: mm)



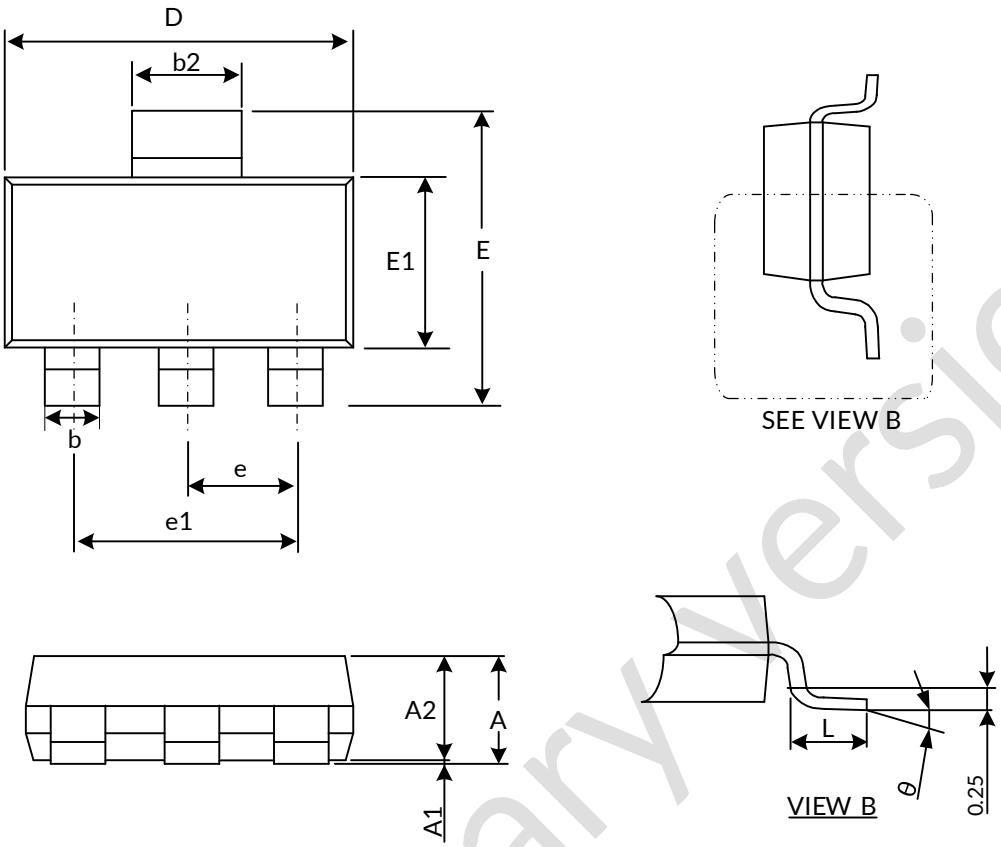


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.250		0.049
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.360	0.500	0.014	0.020
c	0.100	0.200	0.004	0.008
D (1)	2.826	3.026	0.111	0.119
E (1)	1.526	1.726	0.060	0.068
E1	2.600	3.000	0.102	0.118
e	0.950(BSC) (2)		0.037(BSC) (2)	
e1	1.800	2.000	0.071	0.079
L	0.350	0.600	0.014	0.024
θ	0°	8°	0°	8°

NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

SOT-223 (3)

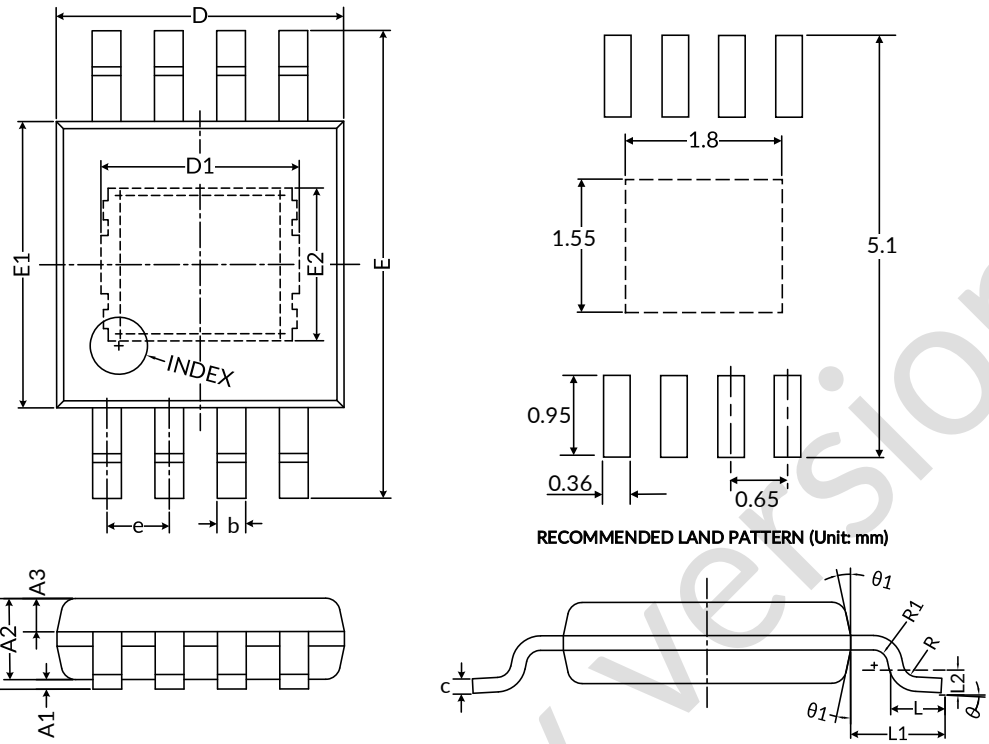


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	-	1.800	-	0.071
A1	0.02	0.10	0.001	0.004
A2	1.55	1.65	0.061	0.065
b	0.66	0.84	0.026	0.033
b2	2.90	3.10	0.114	0.122
D (1)	6.30	6.70	0.248	0.263
E	6.70	7.30	0.263	0.287
E1 (1)	3.30	3.70	0.130	0.145
e	2.30 BSC (2)		0.090 BSC (2)	
e1	4.60 BSC (2)		0.181 BSC (2)	
L	0.90	-	0.035	-

NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

EMSOP8 (4)

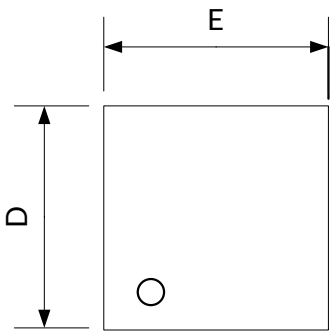


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	-	1.100	-	0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
A3	0.300	0.400	0.012	0.016
b	0.250	0.380	0.010	0.015
c	0.130	0.200	0.005	0.008
D (1)	2.900	3.100	0.114	0.122
D1	1.920	2.220	0.076	0.087
E	4.750	5.050	0.187	0.199
E1 (1)	2.900	3.100	0.114	0.122
E2	1.450	1.750	0.057	0.069
e	0.550	0.750	0.022	0.030
L	0.400	0.700	0.016	0.028
L1	0.950 REF (2)		0.037 REF (2)	
L2	0.250 BSC (3)		0.010 BSC (3)	
R	0.070	-	0.003	-
R1	0.070	-	0.003	-
θ	0°	8°	0°	8°
θ1	9°	15°	9°	15°

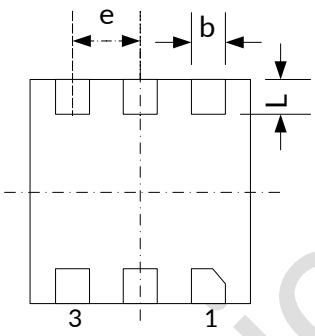
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. REF is the abbreviation for Reference.
3. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
4. This drawing is subject to change without notice.

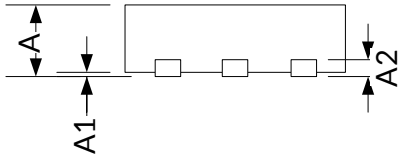
DFN2X2-6 (2)



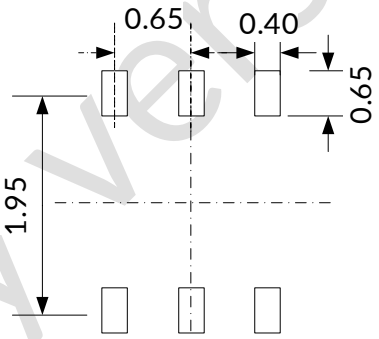
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203(TYP)		0.008(TYP)	
b	0.250	0.350	0.010	0.012
D (1)	1.900	2.100	0.075	0.083
E (1)	1.900	2.100	0.075	0.083
e	0.650(TYP)		0.026(TYP)	
L	0.250	0.400	0.010	0.018

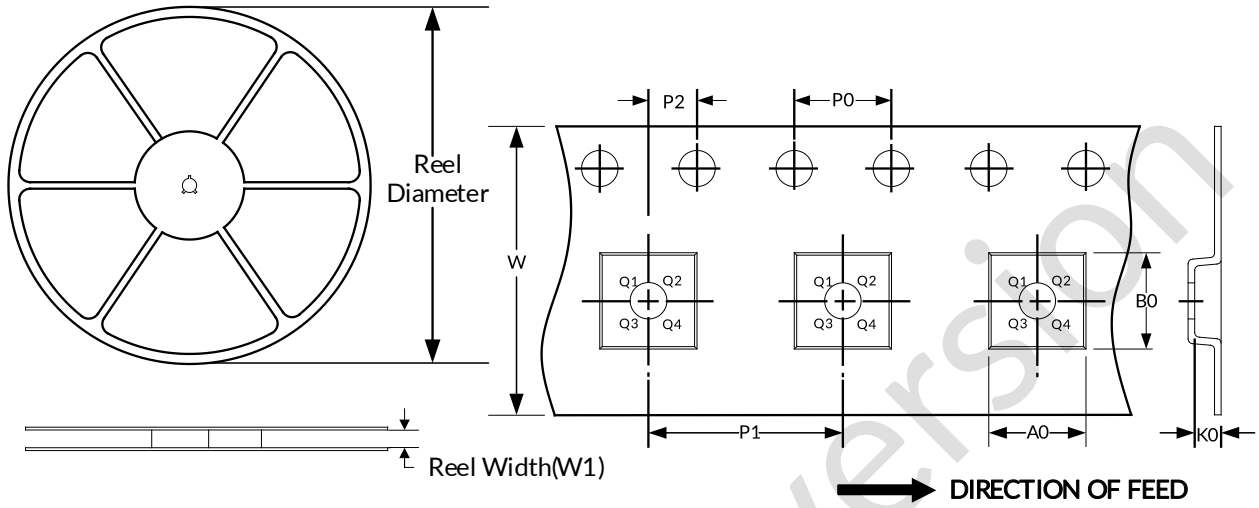
NOTE:

1. Plastic or metal protrusions of 0.075mm maximum per side are not included.
2. This drawing is subject to change without notice.

14 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT23-5	7”	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
SOT-223	13”	12.4	6.765	7.335	1.88	4.0	8.0	2.0	12.0	Q3
EMSOP8	13”	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1
DFN2X2-6	7”	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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