

# 10MHz, Rail-to-Rail I/O CMOS Operational Amplifier

## 1 FEATURES

- **High Gain Bandwidth: 10MHz**
- **Rail-to-Rail Input and Output**  
**±0.5mV Typical Vos**
- **Input Voltage Range: -0.1V to +5.6V**  
**with Vs = 5.5V**
- **Supply Range: +2.5V to +5.5V**
- **Specified Up to +125°C**
- **Micro Size Packages: SOT23-5**

## 2 APPLICATIONS

- **Sensors**
- **Photodiode Amplification**
- **Active Filters**
- **Test Equipment**
- **Driving A/D Converters**

## 3 DESCRIPTIONS

The RS72X families of products offer low voltage operation and rail-to-rail input and output, as well as excellent speed/power consumption ratio, providing an excellent bandwidth (10MHz) and slew rate of 7V/μs. The op-amps are unity gain stable and feature an ultra-low input bias current.

The devices are ideal for sensor interfaces, active filters and portable applications. The RS72X families of operational amplifiers are specified at the full temperature range of -40°C to +125°C under single or dual power supplies of 2.5V to 5.5V.

**Device Information <sup>(1)</sup>**

PART NUMBER	PACKAGE	BODY SIZE(NOM)
RS721	SOT23-5	2.90mm×1.60mm
	DFN2X2-6	2.00mm×2.00mm
RS722	SOP8	4.90mm×3.90mm
	MSOP8	3.00mm×3.00mm
	DFN2X2-8	2.00mm×2.00mm
	DFN3X3-8 (0303X0.75-0.65)	3.00mm×3.00mm
RS724	SOP14	8.65mm×3.90mm
	TSSOP14	5.00mm×4.40mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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## 4 REVISION HISTORY

Note: Page numbers for previous revisions may differ from page numbers in the current version.

<b>VERSION</b>	<b>Change Date</b>	<b>Change Item</b>
C.1	2021/06/16	Add TDFN3x3-8L(0303x0.75-0.5) package
C.2	2022/06/14	Add TDFN2X2-6L PACKAGE/ORDERING INFORMATION
C.3	2023/09/14	Add MSL on Page 8 in RevC.2
C.3.1	2024/03/01	Modify packaging naming
C.4	2025/01/08	1. Delete RS721XK/RS721XM/RS721SXH/RS721S XK/RS722SXN/ RS722XTDC8-B Orderable Device 2. Delete contents related to RS721S and RS722S

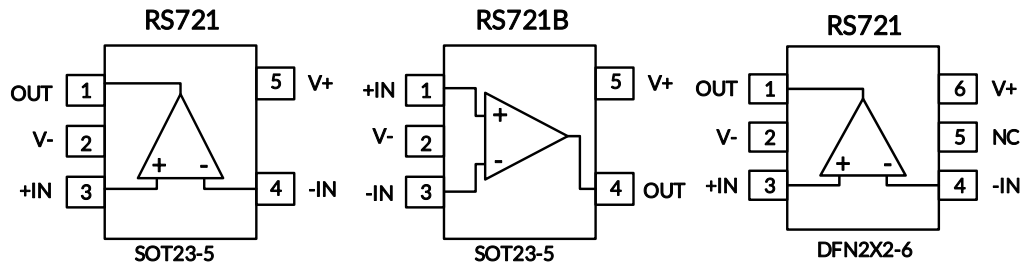
**5 PACKAGE/ORDERING INFORMATION (1)**

Orderable Device	Package Type	Pin	Channel	Op Temp(°C)	Device Marking (2)	MSL (3)	Package Qty
RS721XF	SOT23-5	5	1	-40°C ~125°C	721	MSL3	Tape and Reel,3000
RS721BXF	SOT23-5	5	1	-40°C ~125°C	721B	MSL3	Tape and Reel,3000
RS721XTDE6	DFN2X2-6	6	1	-40°C ~125°C	721	MSL3	Tape and Reel,3000
RS722XK	SOP8	8	2	-40°C ~125°C	RS722	MSL3	Tape and Reel,4000
RS722XM	MSOP8	8	2	-40°C ~125°C	RS722	MSL3	Tape and Reel,4000
RS722XTDE8	DFN2X2-8	8	2	-40°C ~125°C	722	MSL3	Tape and Reel,3000
RS722XTDC8	DFN3X3-8 (0303X0.75-0.65)	8	2	-40°C ~125°C	RS722	MSL3	Tape and Reel,5000
RS724XP	SOP14	14	4	-40°C ~125°C	RS724	MSL3	Tape and Reel,4000
RS724XQ	TSSOP14	14	4	-40°C ~125°C	RS724	MSL3	Tape and Reel,4000

**NOTE:**

- (1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.
- (2) There may be additional marking, which relates to the lot trace code information(data code and vendor code), the logo or the environmental category on the device.
- (3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

## 6 PIN CONFIGURATION AND FUNCTIONS



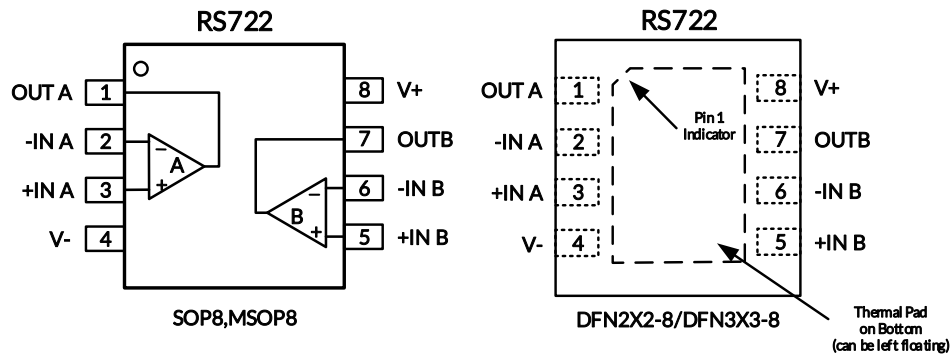
### Pin Description

NAME	PIN			I/O <sup>(1)</sup>	DESCRIPTION
	RS721	RS721B	RS721		
	SOT23-5	SOT23-5	DFN2X2-6		
-IN	4	3	4	I	Negative (inverting) input
+IN	3	1	3	I	Positive (noninverting) input
NC <sup>(2)</sup>	-	-	5	-	No internal connection (can be left floating)
OUT	1	4	1	O	Output
V-	2	2	2	-	Negative (lowest) power supply
V+	5	5	6	-	Positive (highest) power supply

(1) I = Input, O = Output.

(2) There is no internal connection. Typically, GND is the recommended connection to a heat spreading plane.

## PIN CONFIGURATION AND FUNCTIONS

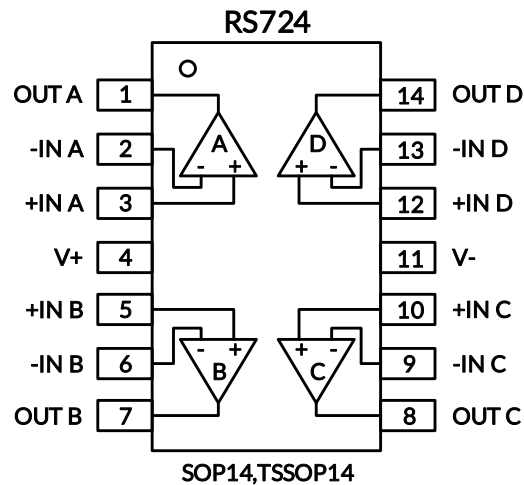


### Pin Description

NAME	PIN		I/O <sup>(1)</sup>	DESCRIPTION
	RS722			
	SOP8/MSOP8/ DFN2X2-8/DFN3X3-8			
-INA	2	I	Inverting input, channel A	
+INA	3	I	Noninverting input, channel A	
-INB	6	I	Inverting input, channel B	
+INB	5	I	Noninverting input, channel B	
OUTA	1	O	Output, channel A	
OUTB	7	O	Output, channel B	
V-	4	-	Negative (lowest) power supply	
V+	8	-	Positive (highest) power supply	
-	Thermal Pad	-	Connect thermal pad to V-	

(1) I = Input, O = Output.

## PIN CONFIGURATION AND FUNCTIONS



### Pin Description

NAME	PIN	I/O <sup>(1)</sup>	DESCRIPTION
	SOP14/TSSOP14		
-INA	2	I	Inverting input, channel A
+INA	3	I	Noninverting input, channel A
-INB	6	I	Inverting input, channel B
+INB	5	I	Noninverting input, channel B
-INC	9	I	Inverting input, channel C
+INC	10	I	Noninverting input, channel C
-IND	13	I	Inverting input, channel D
+IND	12	I	Noninverting input, channel D
OUTA	1	O	Output, channel A
OUTB	7	O	Output, channel B
OUTC	8	O	Output, channel C
OUTD	14	O	Output, channel D
V-	11	-	Negative (lowest) power supply
V+	4	-	Positive (highest) power supply

(1) I = Input, O = Output.

## 7 SPECIFICATIONS

### 7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT	
Voltage	Supply, $V_S=(V+) - (V-)$		7	V	
	Signal input pin <sup>(2)</sup>	(V-)-0.5	(V+) +0.5		
	Signal output pin <sup>(3)</sup>	(V-)-0.5	(V+) +0.5		
Current	Signal input pin <sup>(2)</sup>	-10	10	mA	
	Signal output pin <sup>(3)</sup>	-100	100	mA	
	Output short-circuits <sup>(4)</sup>	Continuous			
$\theta_{JA}$	Package thermal impedance <sup>(5)</sup>	SOT23-5		230	°C/W
		SOP8		110	
		MSOP8		170	
		SOP14		105	
		TSSOP14		90	
		DFN3X3-8		45	
		DFN2X2-8		80	
Temperature	Operating range, $T_A$	-40	125	°C	
	Junction, $T_J$ <sup>(6)</sup>	-40	150		
	Storage, $T_{stg}$	-65	150		

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.

(3) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.5V beyond the supply rails should be current-limited to  $\pm 100$ mA or less.

(4) Short-circuit to ground, one amplifier per package.

(5) The package thermal impedance is calculated in accordance with JESD-51.

(6) The maximum power dissipation is a function of  $T_{J(MAX)}$ ,  $R_{\theta JA}$ , and  $T_A$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$ . All numbers apply for packages soldered directly onto a PCB.

### 7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM)	$\pm 5000$
		Machine Model (MM)	$\pm 400$



#### ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, $V_S= (V+) - (V-)$	Single-supply	2.5		5.5	V
	Dual-supply	$\pm 1.25$		$\pm 2.75$	



## 7.4 Electrical Characteristics

(At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , and  $V_{OUT} = V_S/2$ ,  $V_{CM} = V_S/2$ , Full <sup>(9)</sup> =  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted.) <sup>(1)</sup>

PARAMETER		CONDITIONS	$T_J$	RS721, RS722, RS724			
				MIN <sup>(2)</sup>	TYP <sup>(3)</sup>	MAX <sup>(2)</sup>	UNIT
<b>POWER SUPPLY</b>							
$V_S$	Operating Voltage Range		25°C	2.5		5.5	V
$I_Q$	Quiescent Current Per Amplifier		25°C		1.15	1.4	mA
PSRR	Power-Supply Rejection Ratio	$V_S = 2.5\text{V to } 5.5\text{V}$ , $V_{CM} = (V_-) + 0.5\text{V}$	25°C	75	85		dB
			Full	65			
<b>INPUT</b>							
$V_{OS}$	Input Offset Voltage	$V_{CM} = V_S/2$	25°C	-2.5	$\pm 0.5$	2.5	mV
$V_{OS\ TC}$	Input Offset Voltage Average Drift	$V_{CM} = V_S/2$	Full		$\pm 2.6$		$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current <sup>(4) (5)</sup>		25°C		$\pm 1$	$\pm 10$	pA
$I_{OS}$	Input Offset Current <sup>(5)</sup>		25°C		$\pm 1$	$\pm 10$	pA
$V_{CM}$	Common-Mode Voltage Range	$V_S = 5.5\text{V}$	25°C	-0.1		5.6	V
CMRR	Common-Mode Rejection Ratio	$V_S = 5.5\text{V}$ , $V_{CM} = -0.1\text{V to } 4\text{V}$	25°C	73	85		dB
			Full	67			
		$V_S = 5.5\text{V}$ , $V_{CM} = -0.1\text{V to } 5.6\text{V}$	25°C	60	75		
			Full	57			
<b>OUTPUT</b>							
$A_{OL}$	Open-Loop Voltage Gain	$R_L = 2\text{k}\Omega$ , $V_O = 0.15\text{V to } 4.85\text{V}$	25°C	86	95		dB
			Full	65			
		$R_L = 10\text{k}\Omega$ , $V_O = 0.05\text{V to } 4.95\text{V}$	25°C	90	96		
			Full	66			
	Output Swing from Rail	$R_L = 2\text{k}\Omega$	25°C		52		mV
		$R_L = 10\text{k}\Omega$			7		
$I_{OUT}$	Output Short-Circuit Current <sup>(6) (7)</sup>		25°C		$\pm 70$		mA
<b>FREQUENCY RESPONSE</b>							
SR	Slew Rate <sup>(8)</sup>		25°C		7		$\text{V}/\mu\text{s}$
GBP	Gain-Bandwidth Product		25°C		10		MHz
PM	Phase Margin <sup>(5)</sup>		25°C		62		°
$t_s$	Settling Time, 0.1%				0.2		$\mu\text{s}$
	Overload Recovery Time	$V_{IN} \cdot \text{Gain} \geq V_S$			0.35		$\mu\text{s}$
<b>NOISE</b>							
$e_n$	Input Voltage Noise Density	$f = 1\text{KHz}$	25°C		9.5		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{KHz}$	25°C		6.5		$\text{nV}/\sqrt{\text{Hz}}$

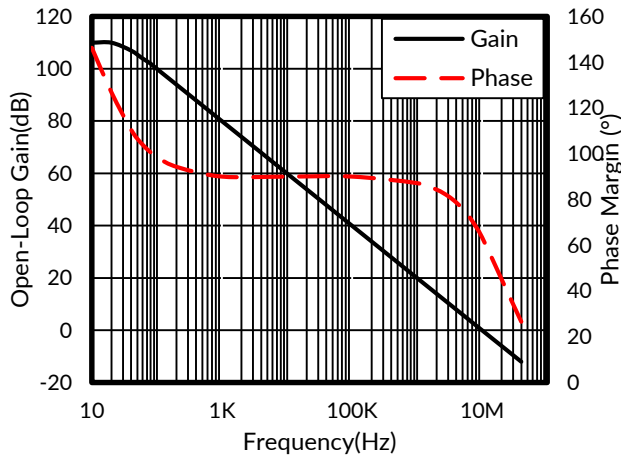
## NOTE:

- (1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
- (2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
- (3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
- (4) Positive current corresponds to current flowing into the device.
- (5) This parameter is ensured by design and/or characterization and is not tested in production.
- (6) The maximum power dissipation is a function of  $T_{J(MAX)}$ ,  $R_{\theta JA}$ , and  $T_A$ . The maximum allowable power dissipation at any ambient temperature is  $PD = (T_{J(MAX)} - T_A) / R_{\theta JA}$ . All numbers apply for packages soldered directly onto a PCB.
- (7) Short circuit test is a momentary test.
- (8) Number specified is the slower of positive and negative slew rates.
- (9) Specified by characterization only.

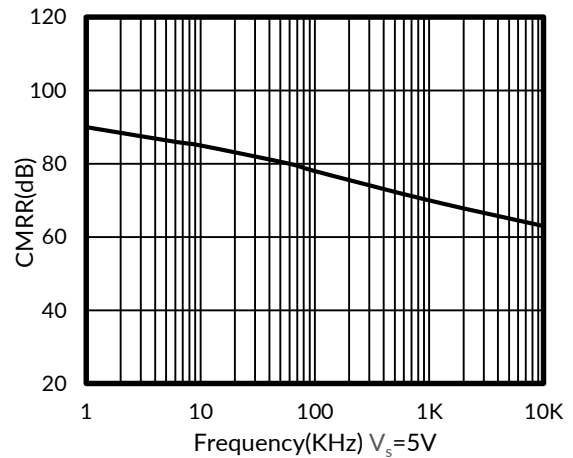
## 7.5 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

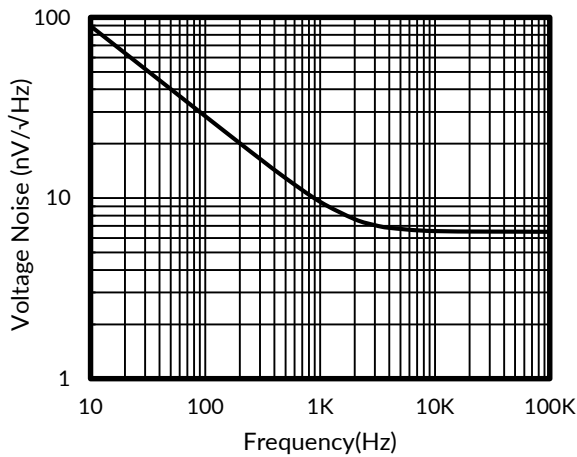
At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ ,  $V_{OUT} = V_S/2$ , unless otherwise noted.



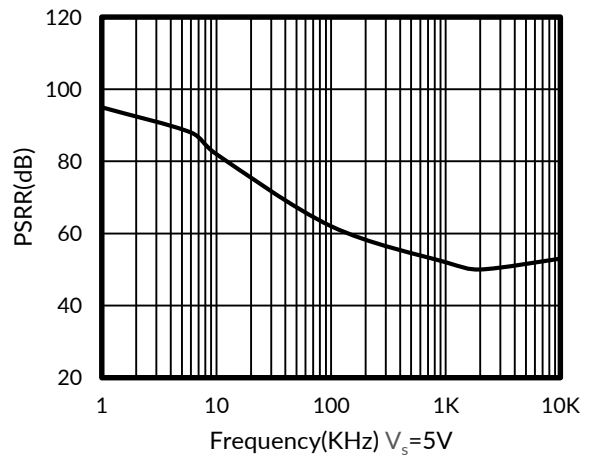
**Figure 1. Open-Loop Gain And Phase vs Frequency**



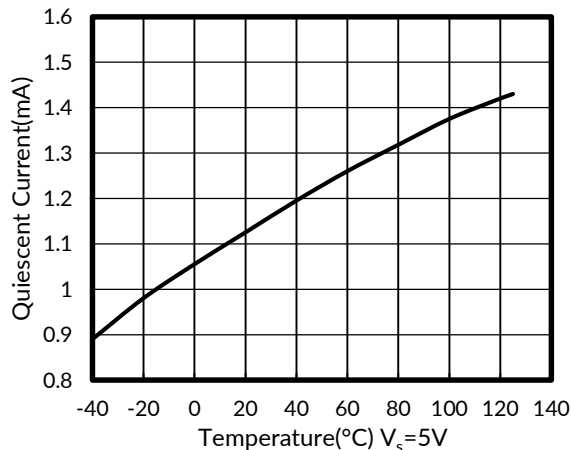
**Figure 2. Common-Mode Rejection Ratio vs Frequency**



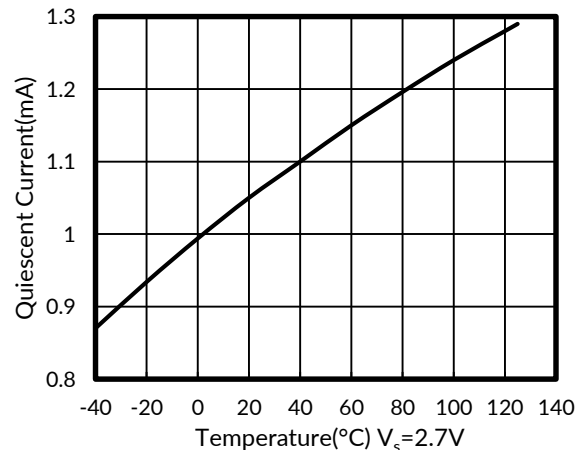
**Figure 3. Input Voltage Noise Spectral Density vs Frequency**



**Figure 4. Power-Supply Rejection Ratio vs Frequency**



**Figure 5. Quiescent Current Vs Temperature**

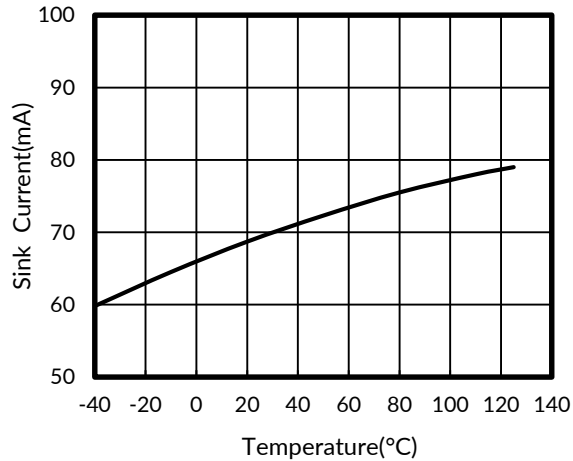


**Figure 6. Quiescent Current Vs Temperature**

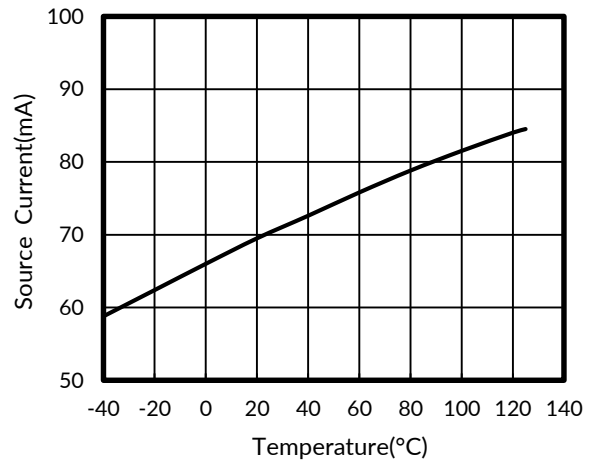
## Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

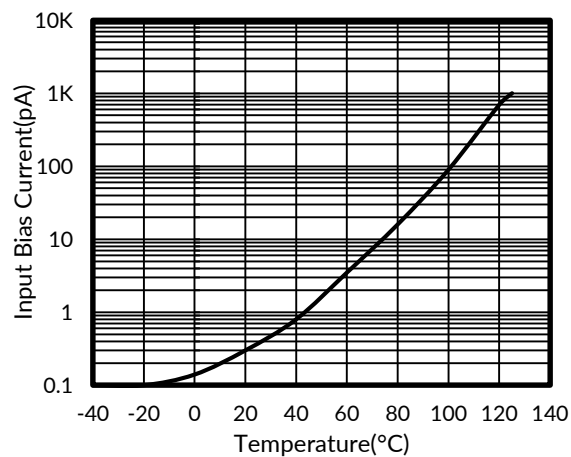
At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ ,  $V_{OUT} = V_S/2$ , unless otherwise noted.



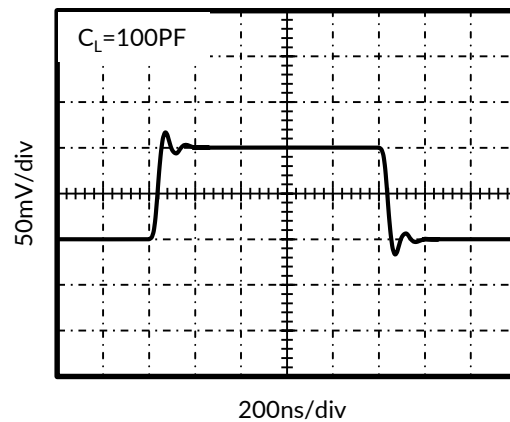
**Figure 7. Sink Current vs Temperature**



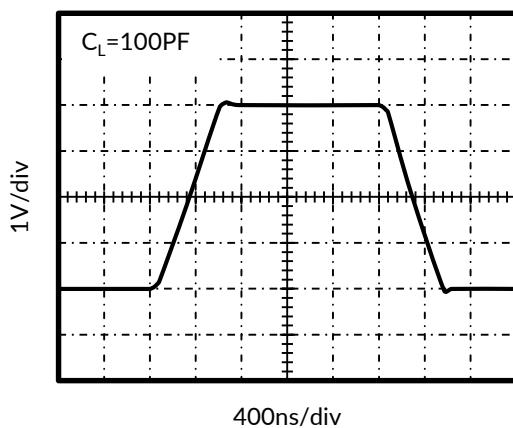
**Figure 8. Source Current vs Temperature**



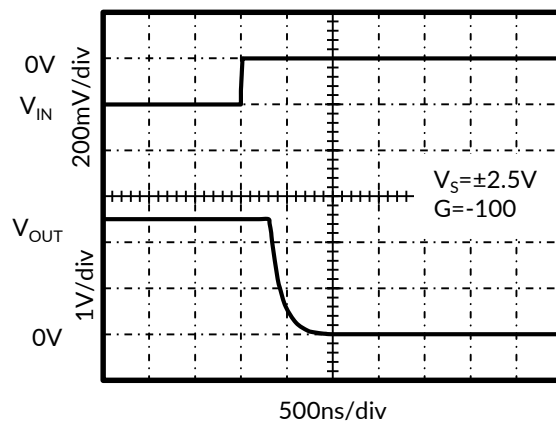
**Figure 9. Input Bias Current vs Temperature**



**Figure 10. Small-Signal Step Response**



**Figure 11. Large-Signal Step Response**



**Figure 12. Positive Overload Recovery**

### Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ ,  $V_{OUT} = V_S/2$ , unless otherwise noted.

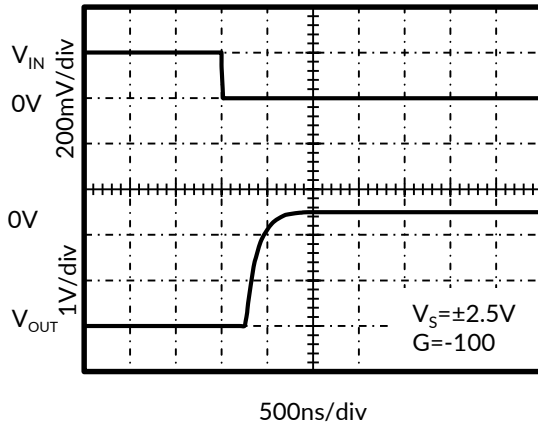


Figure 13. Negative Overload Recovery

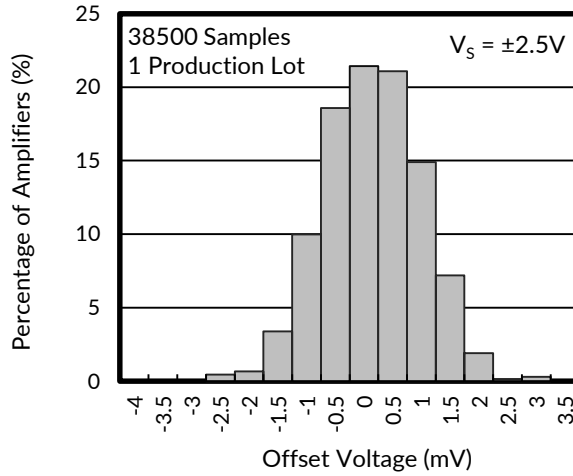


Figure 14. Offset Voltage Production Distribution

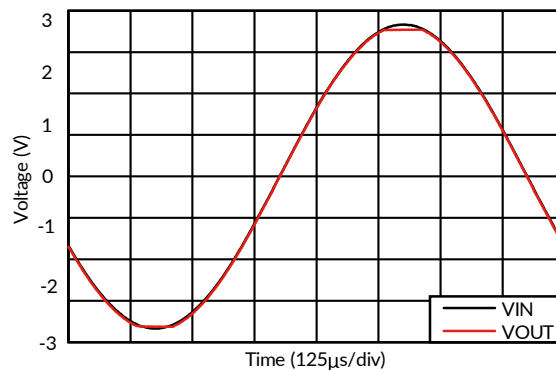
## 8 DETAILED DESCRIPTION

### 8.1 Overview

The RS721, RS722, RS724 are high precision, rail-to-rail operational amplifiers that can be run from a single-supply voltage 2.5V to 5.5V( $\pm 1.25V$  to  $\pm 2.75V$ ). Supply voltages higher than 7V(absolute maximum) can permanently damage the amplifier. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications. Good layout practice mandates use of a 0.1 $\mu$ F capacitor place closely across the supply pins.

### 8.2 Phase Reversal Protection

The RS72X family has internal phase-reversal protection. Many op amps exhibit phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the RS72X prevents phase reversal with excessive common-mode voltage. Instead, the appropriate rail limits the output voltage. This performance is shown in figure 15.



**Figure 15. Output Waveform Devoid of Phase Reversal During an Input Overdrive Condition**

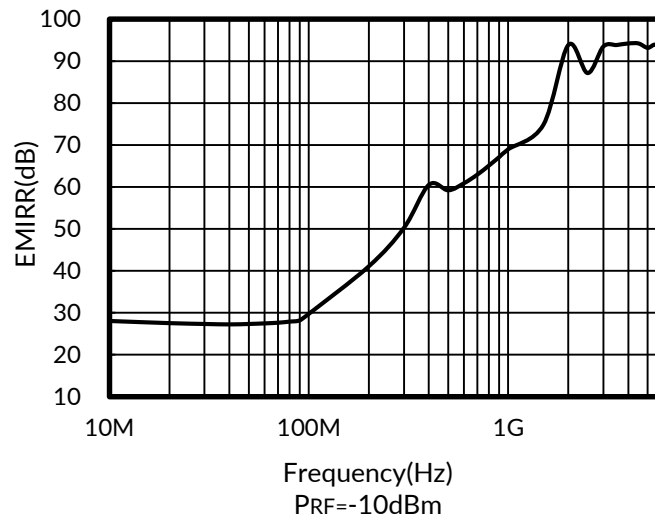
### 8.3 EMI Rejection Ratio (EMIRR)

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many operational amplifiers is a change in the offset voltage as a result of RF signal rectification. An operational amplifier that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this document provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the operational amplifier. In general, only the noninverting input is tested for EMIRR for the following three reasons:

- Operational amplifier input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
- The noninverting and inverting operational amplifier inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance.
- EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input pin can be isolated on a printed-circuit-board (PCB). This isolation allows the RF signal to be applied directly to the noninverting input pin with no complex interactions from other components or connecting PCB traces.

## Detailed Description(continued)

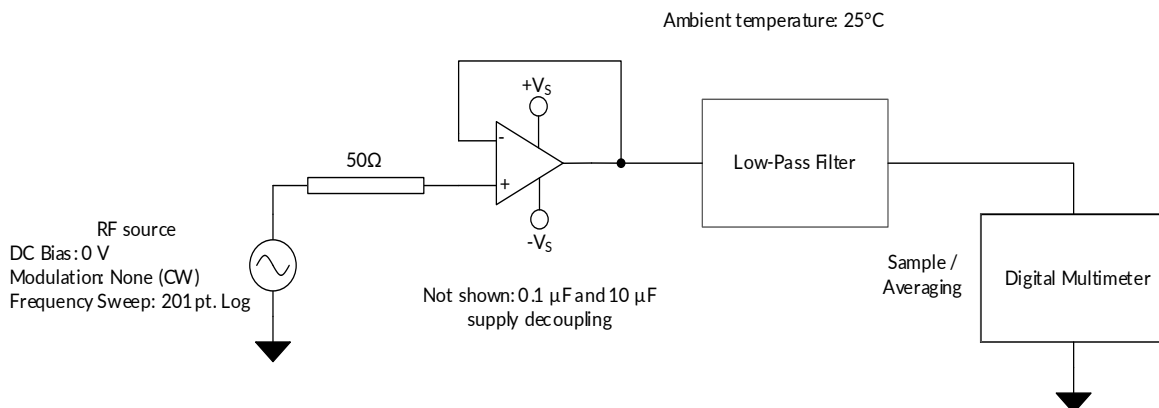
The EMIRR IN+ of the RS72X is plotted versus frequency in Figure 16. If available, any dual and quad operational amplifier device versions have approximately identical EMIRR IN+ performance. The RS72X unity-gain bandwidth is 10MHz. EMIRR performance below this frequency denotes interfering signals that fall within the operational amplifier bandwidth.



**Figure 16. RS72X EMIRR vs Frequency**

### 8.4 EMIRR IN+ Test Configuration

Figure 17 shows the circuit configuration for testing the EMIRR IN+. An RF source is connected to the operational amplifier noninverting input pin using a transmission line. The operational amplifier is configured in a unity-gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). A large impedance mismatch at the operational amplifier input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The resulting dc offset voltage is sampled and measured by the multimeter. The LPF isolates the multimeter from residual RF signals that can interfere with multimeter accuracy.



**Figure 17. EMIRR IN+ Test Configuration Schematic**

## 9 APPLICATION AND IMPLEMENTATION

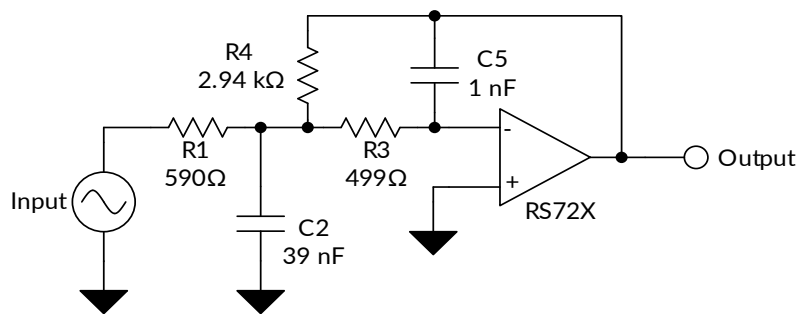
Information in the following applications sections is not part of the Runic component specification, and Runic does not warrant its accuracy or completeness. Runic's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Note

The RS72X are high precision, rail-to-rail operational amplifiers that can be run from a single-supply voltage 2.5V to 5.5V ( $\pm 1.25V$  to  $\pm 2.75V$ ). Supply voltages higher than 7V (absolute maximum) can permanently damage the amplifier. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications. Good layout practice mandates use of a 0.1 $\mu F$  capacitor place closely across the supply pins.

### Typical Applications

#### 9.2 25-kHz Low-pass Filter



**Figure 18. 25-kHz Low-Pass Filter**

### 9.3 Design Requirements

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The RS72X devices are ideally suited to construct high-speed, high-precision active filters. Figure 18 shows a second-order, low-pass filter commonly encountered in signal processing applications.

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

### 9.4 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in Figure 18. Use Equation 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1 R_3 C_2 C_5}{s^2 + (s/C_2) (1/R_1 + 1/R_3 + 1/R_4) + 1/R_3 R_4 C_2 C_5} \quad (1)$$

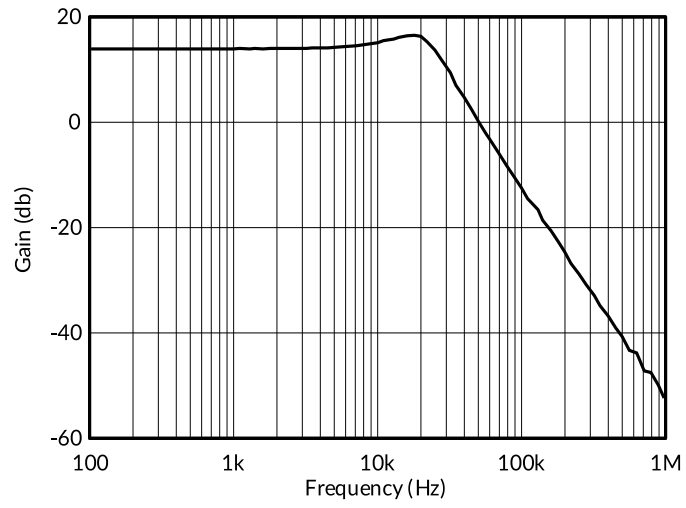
This circuit produces a signal inversion. For this circuit, the gain at dc and the low-pass cutoff frequency are calculated by Equation 2:

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_c = \frac{1}{2\pi} \sqrt{1/R_3 R_4 C_2 C_5} \quad (2)$$



### 9.5 Application Curve



**Figure 19. Low-Pass Filter Transfer Function**

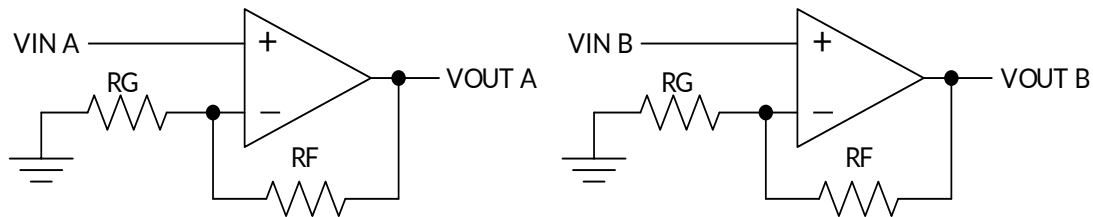
## 10 LAYOUT

### 10.1 Layout Guidelines

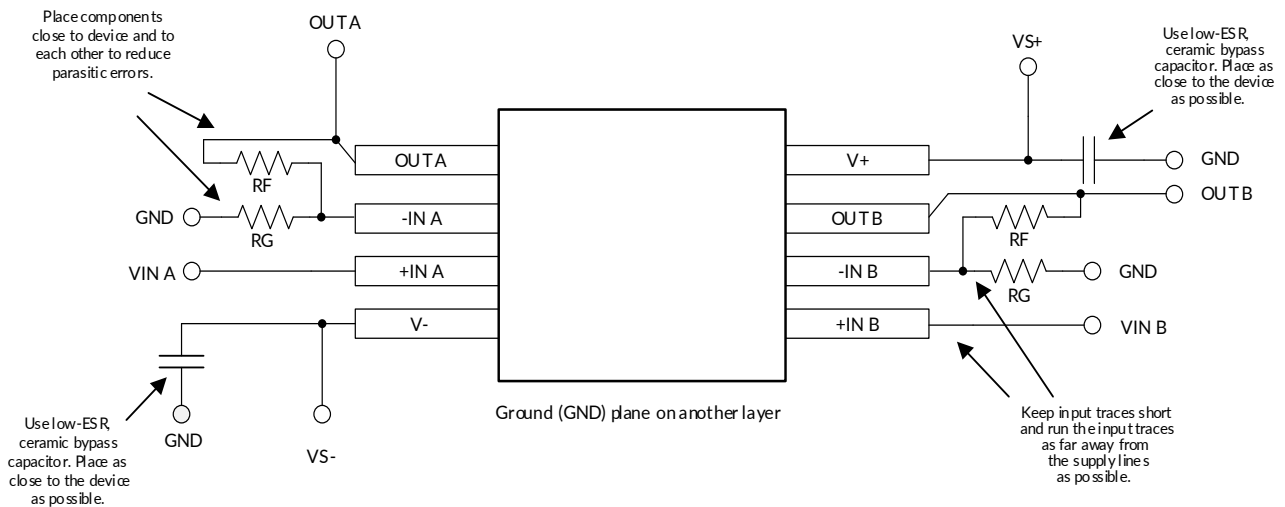
Attention to good layout practices is always recommended. Keep traces short. When possible, use a PCB ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1 $\mu$ F capacitor closely across the supply pins.

These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the EMI susceptibility.

### 10.2 Layout Example



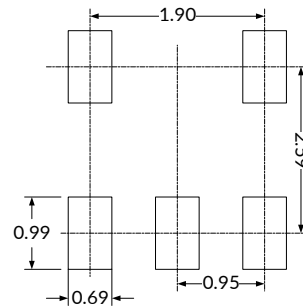
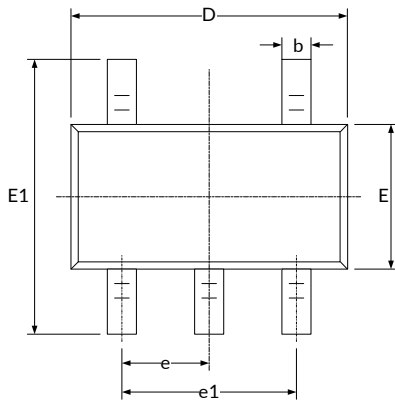
**Figure 20. Schematic Representation**



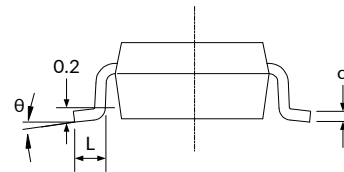
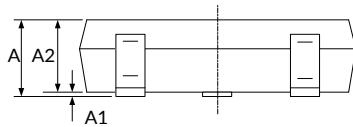
**Figure 21. Layout Example**

# 11 PACKAGE OUTLINE DIMENSIONS

## SOT23-5<sup>(3)</sup>



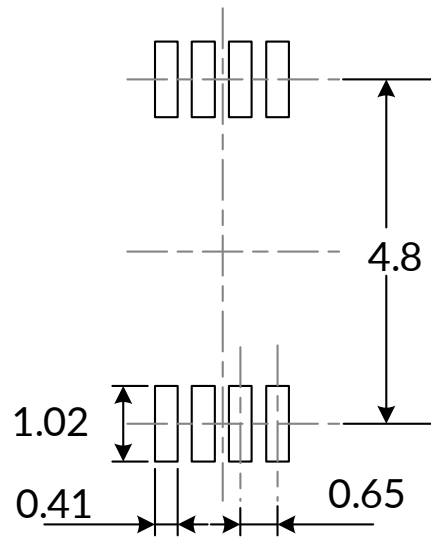
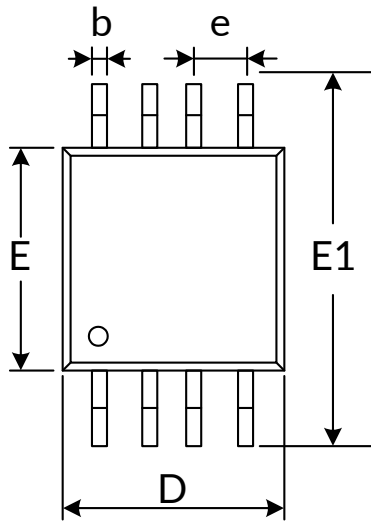
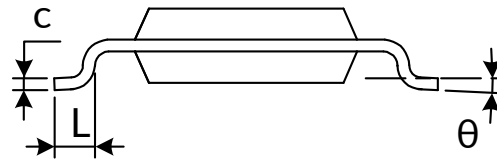
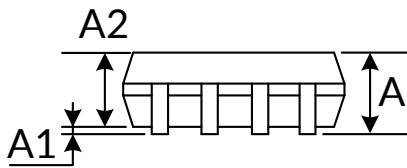
RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A <sup>(1)</sup>	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D <sup>(1)</sup>	2.820	3.020	0.111	0.119
E <sup>(1)</sup>	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC) <sup>(2)</sup>		0.037(BSC) <sup>(2)</sup>	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
$\theta$	0°	8°	0°	8°

NOTE:

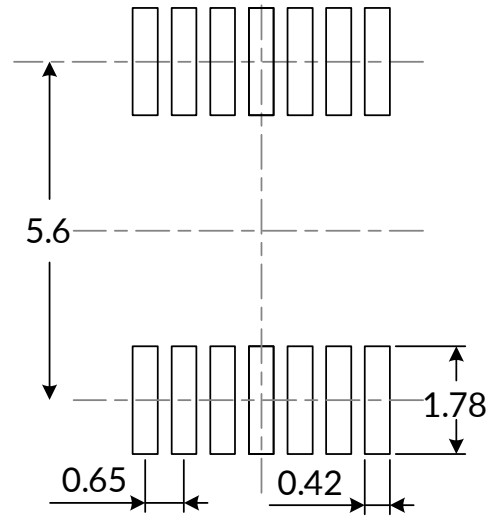
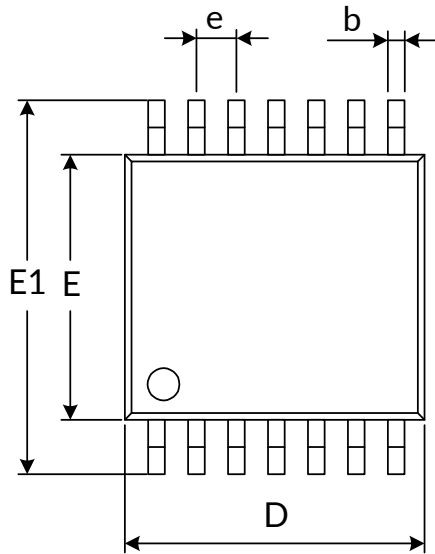
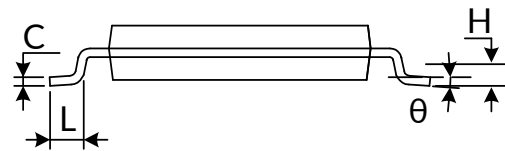
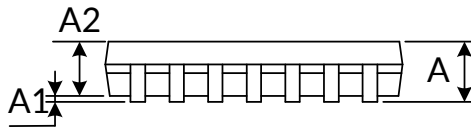
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

**MSOP8<sup>(3)</sup>**

**RECOMMENDED LAND PATTERN (Unit: mm)**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A <sup>(1)</sup>	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D <sup>(1)</sup>	2.900	3.100	0.114	0.122
e	0.650(BSC) <sup>(2)</sup>		0.026(BSC) <sup>(2)</sup>	
E <sup>(1)</sup>	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

**NOTE:**

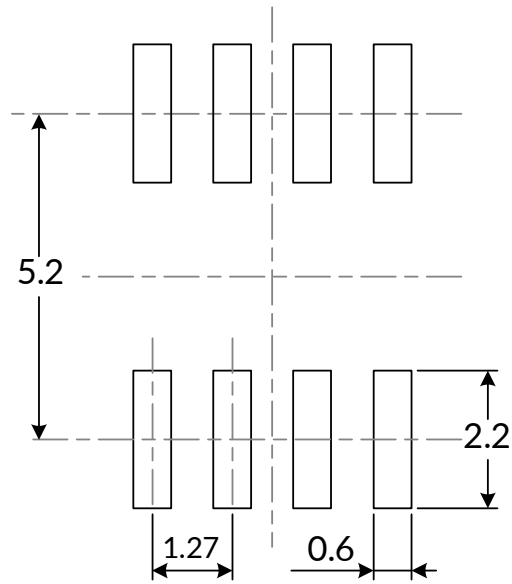
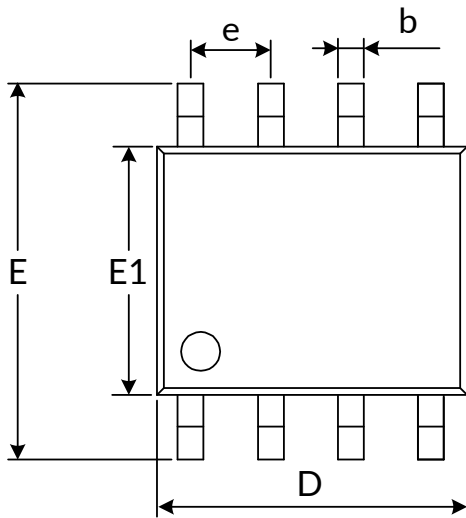
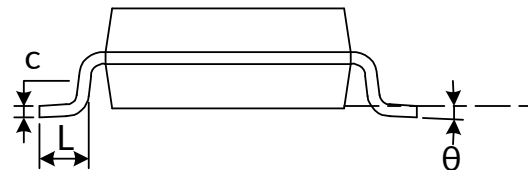
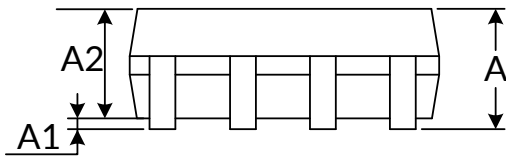
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

**TSSOP14 (3)**

**RECOMMENDED LAND PATTERN** (Unit: mm)


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A <sup>(1)</sup>		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D <sup>(1)</sup>	4.860	5.100	0.191	0.201
E <sup>(1)</sup>	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650(BSC) <sup>(2)</sup>		0.026(BSC) <sup>(2)</sup>	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
$\theta$	1°	7°	1°	7°

**NOTE:**

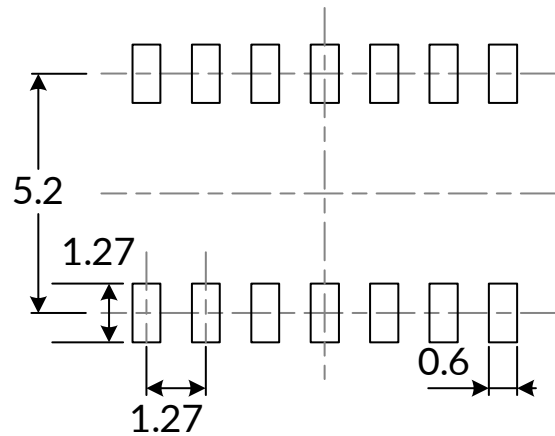
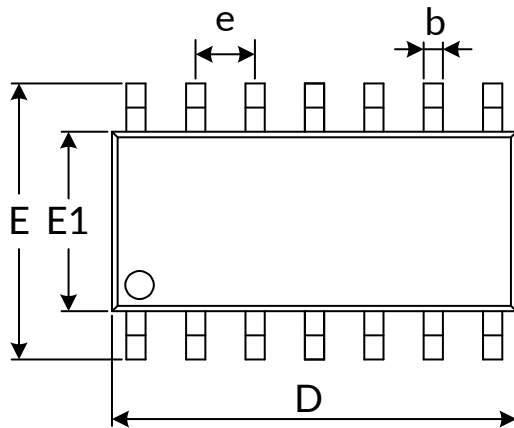
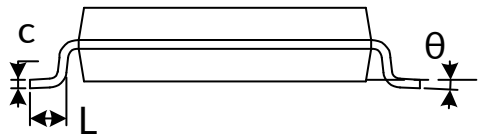
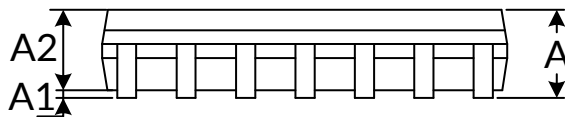
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

**SOP8<sup>(3)</sup>**

**RECOMMENDED LAND PATTERN (Unit: mm)**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A <sup>(1)</sup>	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D <sup>(1)</sup>	4.800	5.000	0.189	0.197
e	1.270(BSC) <sup>(2)</sup>		0.050(BSC) <sup>(2)</sup>	
E	5.800	6.200	0.228	0.244
E1 <sup>(1)</sup>	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
$\theta$	0°	8°	0°	8°

**NOTE:**

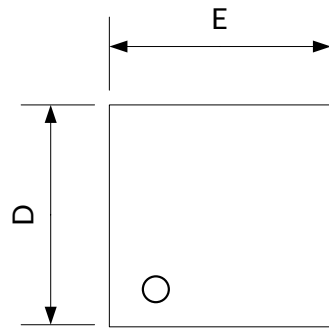
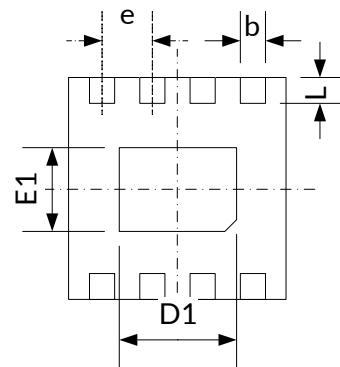
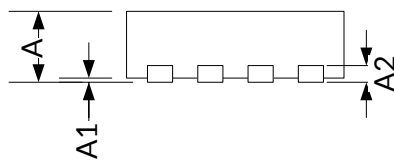
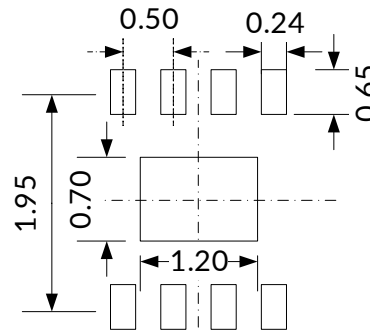
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

**SOP14<sup>(3)</sup>**

**RECOMMENDED LAND PATTERN (Unit: mm)**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A <sup>(1)</sup>	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D <sup>(1)</sup>	8.450	8.850	0.333	0.348
e	1.270(BSC) <sup>(2)</sup>		0.050(BSC) <sup>(2)</sup>	
E	5.800	6.200	0.228	0.244
E1 <sup>(1)</sup>	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
$\theta$	0°	8°	0°	8°

**NOTE:**

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

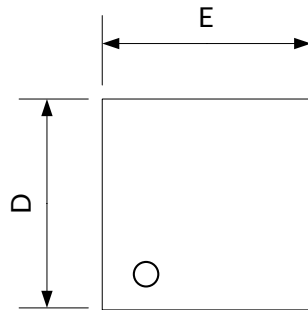
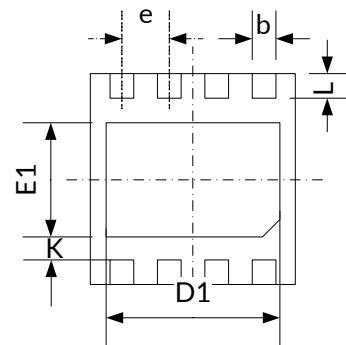
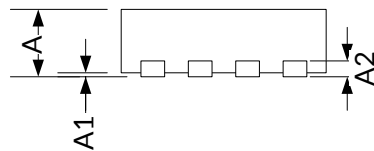
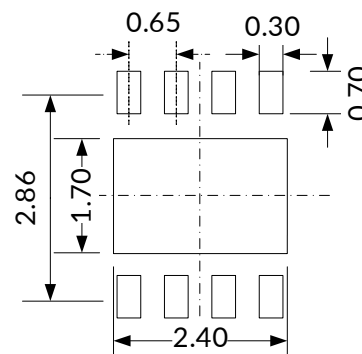
**DFN2X2-8<sup>(2)</sup>**

**TOP VIEW**

**BOTTOM VIEW**

**SIDE VIEW**

**RECOMMENDED LAND PATTERN (Unit: mm)**

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A <sup>(1)</sup>	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203(TYP)		0.008(TYP)	
b	0.180	0.300	0.007	0.012
D <sup>(1)</sup>	1.900	2.100	0.075	0.083
D1	1.100	1.300	0.043	0.051
E <sup>(1)</sup>	1.900	2.100	0.075	0.083
E1	0.600	0.800	0.024	0.031
e	0.500(TYP)		0.020(TYP)	
L	0.250	0.450	0.010	0.018

**NOTE:**

1. Plastic or metal protrusions of 0.075mm maximum per side are not included.
2. This drawing is subject to change without notice.

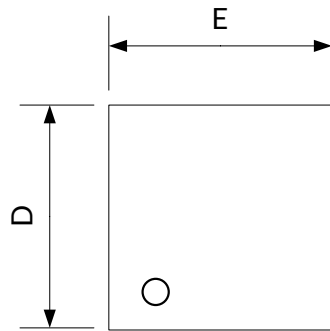
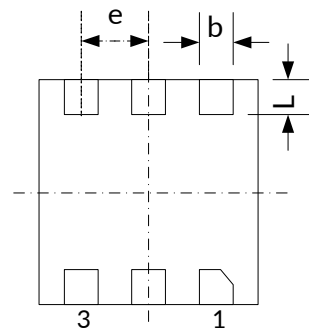
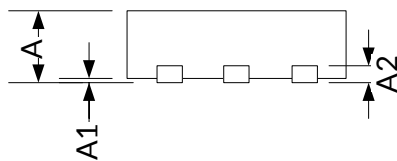
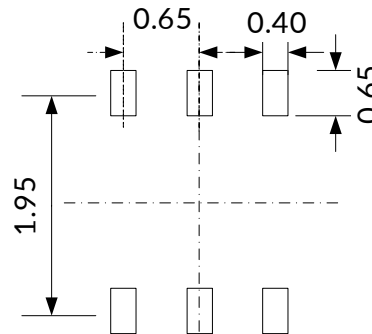


**DFN3X3-8 (0303X0.75-0.65)<sup>(3)</sup>**

**TOP VIEW**

**BOTTOM VIEW**

**SIDE VIEW**

**RECOMMENDED LAND PATTERN (Unit: mm)**

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A <sup>(1)</sup>	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF <sup>(2)</sup>		0.008 REF <sup>(2)</sup>	
b	0.200	0.300	0.008	0.012
D <sup>(1)</sup>	2.900	3.100	0.114	0.122
D1	2.250	2.350	0.089	0.093
E <sup>(1)</sup>	2.900	3.100	0.114	0.122
E1	1.450	1.550	0.057	0.061
e	0.650 TYP		0.026 TYP	
L	0.425	0.525	0.017	0.021
K	0.200 REF <sup>(2)</sup>		0.008 REF <sup>(2)</sup>	

**NOTE:**

1. Plastic or metal protrusions of 0.075mm maximum per side are not included.
2. REF is the abbreviation for Reference.
3. This drawing is subject to change without notice.

**DFN2X2-6<sup>(2)</sup>**

**TOP VIEW**

**BOTTOM VIEW**

**SIDE VIEW**

**RECOMMENDED LAND PATTERN (Unit: mm)**

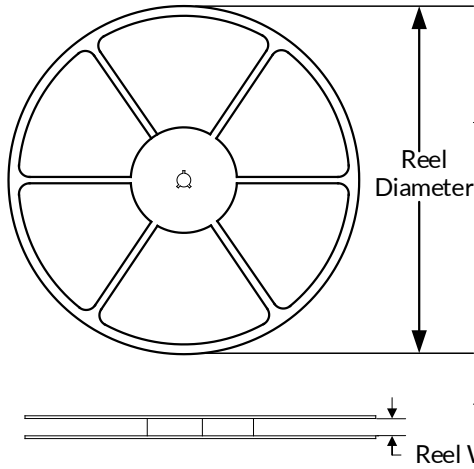
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A <sup>(1)</sup>	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203(TYP)		0.008(TYP)	
b	0.250	0.350	0.010	0.012
D <sup>(1)</sup>	1.900	2.100	0.075	0.083
E <sup>(1)</sup>	1.900	2.100	0.075	0.083
e	0.650(TYP)		0.026(TYP)	
L	0.250	0.400	0.010	0.018

**NOTE:**

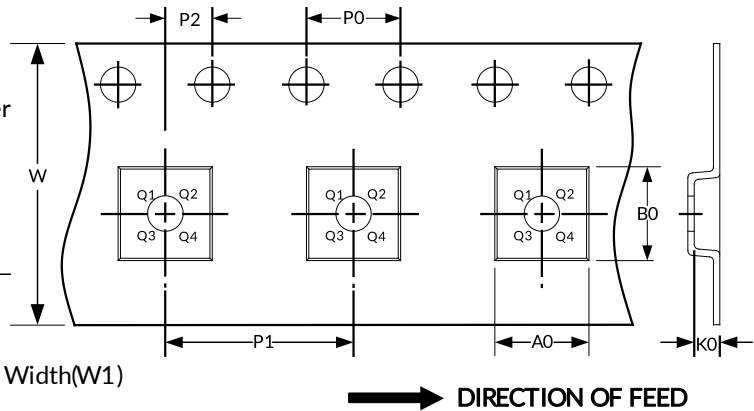
1. Plastic or metal protrusions of 0.075mm maximum per side are not included.
2. This drawing is subject to change without notice.

## 12 TAPE AND REEL INFORMATION

### REEL DIMENSIONS



### TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

### KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT23-5	7"	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
SOP8	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
MSOP8	13"	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1
SOP14	13"	16.4	6.60	9.30	2.10	4.0	8.0	2.0	16.0	Q1
TSSOP14	13"	12.4	6.95	5.60	1.20	4.0	8.0	2.0	12.0	Q1
DFN2X2-6	7"	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q1
DFN2x2-8	7"	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q2
DFN3X3-8 (0303X0.75-0.65)	13"	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q1

NOTE:

1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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