8-Bit Parallel-in, Serial-out Shift Register

1 FEATURES

- **8-bit parallel-in, serial-out shift**
- **Power-Supply Range: 1.65V to 5.5V**
- **High-current output drive ±10mA at 5V**
- **Low Power Consumption: 8μA(Max)**
- **Low Input Current: 1μA(Max)**
- **Gated Serial Data Input**
- **Asynchronous Master Reset**
- **Extended Temperature: -40°C to 125°C**

2 APPLICATIONS

- **Video Display Systems**
- **Programable Logic Controllers**
- **Enterprise and Communicatios**
- **Industrial**
- **Appliances**
- **LED Displays**
- **Output Expander**

3 DESCRIPTIONS

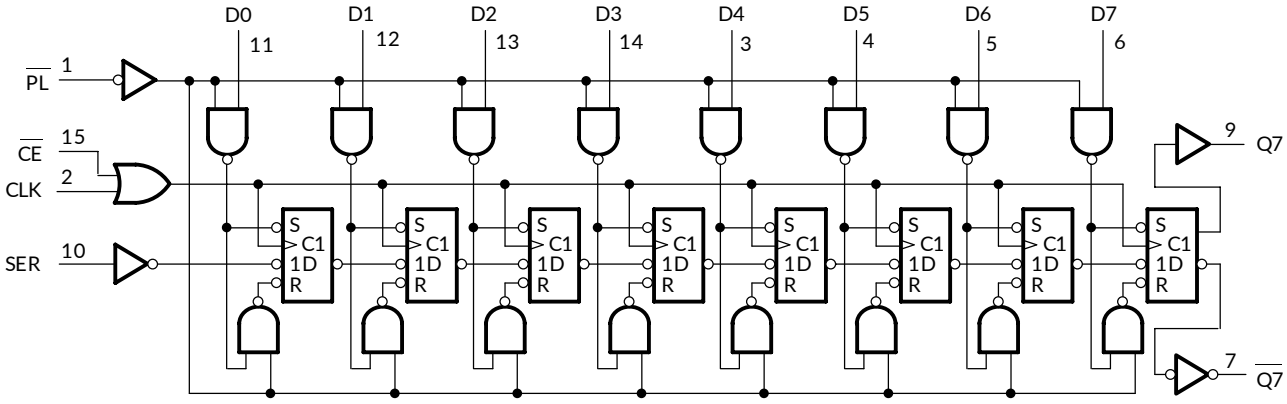
The RS165 is 8-bit serial or parallel-in/serial-out shift registers. The device features a serial data input (SER), eight parallel data inputs (D0 to D7) and two complementary serial outputs (Q7 and $\overline{Q7}$). When the parallel load input ($\overline{PL}$) is Low the data from D0 to D7 is loaded into the shift register asynchronously. When $\overline{PL}$ is High data enters the register serially at SER. When the clock enable input ($\overline{CE}$) is Low data is shifted on the Low-to-High transitions of the CLK input. A High on $\overline{CE}$ will disable the CLK input. Inputs are overvoltage tolerant to 15 V. This enables the device to be used in High-to-Low level shifting applications.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS165	TSSOP16	5.00mm×4.40mm
	SOP16	9.90mm×3.90mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 FUNCTIONAL BLOCK DIAGRAM



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5 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.1	2023/11/03	Initial version completed
A.1.1	2024/02/29	Modify packaging naming
A.2	2024/10/11	1. Modify the format of switching parameters 2. Add MIN MAX value for switching parameter
A.3	2024/11/11	Update Package thermal impedance

6 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING (2)	MSL(3)	PACKAGE OPTION
RS165	RS165XTSS16	-40°C ~125°C	TSSOP16	RS165	MSL3	Tape and Reel,4000
	RS165XS16	-40°C ~125°C	SOP16	RS165	MSL3	Tape and Reel,4000

NOTE:

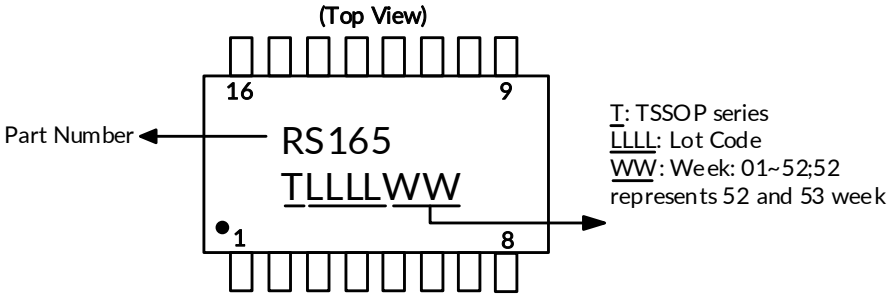
(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

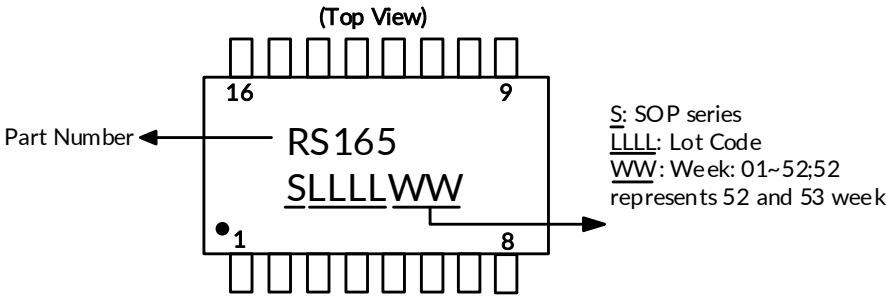
(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F, Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

Marking Information

(1) TSSOP16

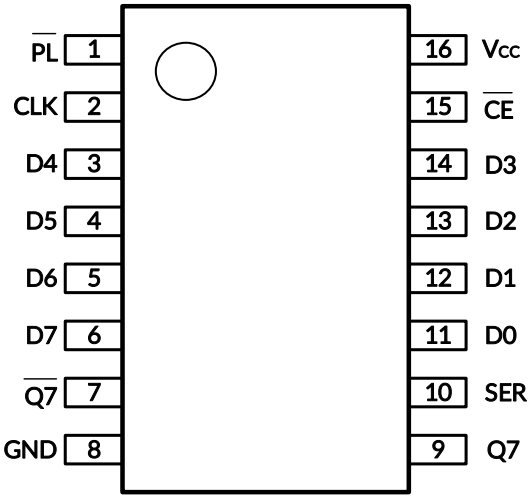


(2) SOP16



7 PIN CONFIGURATIONS

(TOP VIEW)



TSSOP16/SOP16

PIN DESCRIPTION

PIN	NAME	TYPE (1)	FUNCTION
TSSOP16/SOP16			
1	$\overline{PL}$	-	Asynchronous parallel load input (active Low)
2	CLK	I	Clock input (Low-to-High, edge-triggered)
11,12,13,14,3,4,5,6	D0~D7	O	Parallel data inputs
7	$\overline{Q7}$	O	Complementary output from the last stage
8	GND	G	Ground.
9	Q7	O	Serial output from the last stage
10	SER	I	Serial data input
15	$\overline{CE}$	I	Clock enable input (active Low)
16	V_{CC}	P	Supply voltage

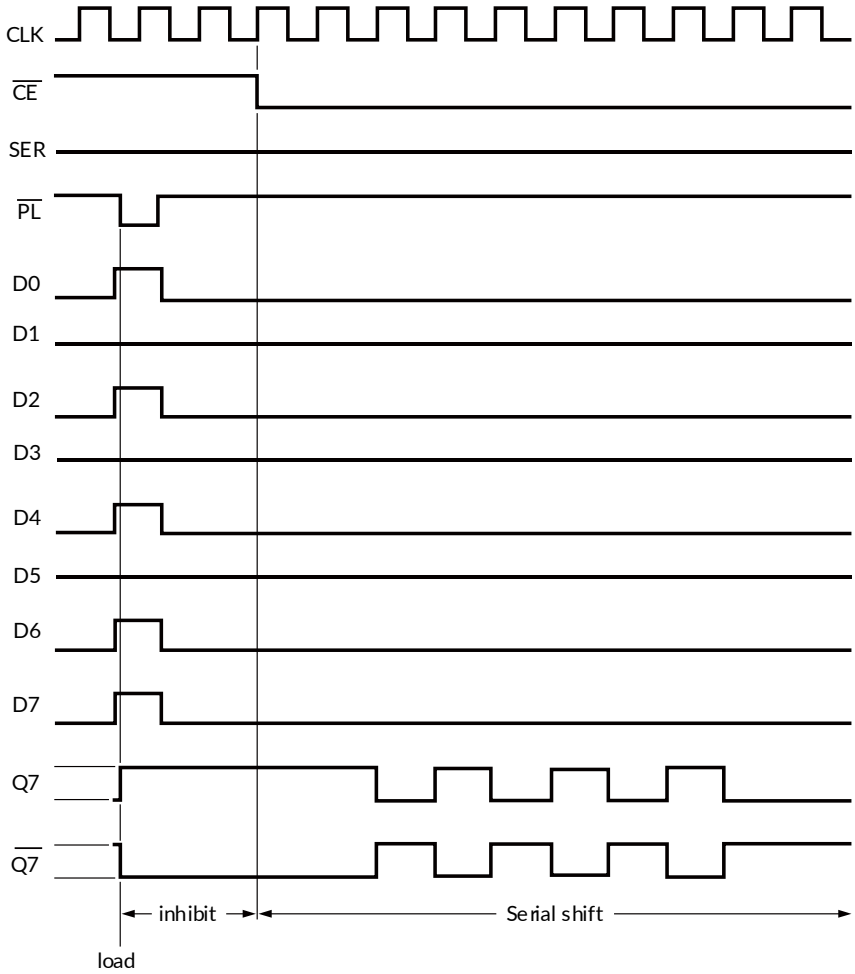
(1) I=input, O=output, P=power, G=Ground.

8 FUNCTIONAL TABLE

Operating modes	Input					Qn register		Output	
	$\overline{PL}$	$\overline{CE}$	CLK	SER	D0 to D7	Q0	Q1 to Q6	Q7	$\overline{Q7}$
Parallel load	L	X	X	X	L	L	L to L	L	H
	L	X	X	X	H	H	H to H	H	L
Serial shift	H	L	↑	I	X	L	q0 to q5	q6	$\overline{q6}$
	H	L	↑	h	X	H	q0 to q5	q6	$\overline{q6}$
	H	↑	L	I	X	L	q0 to q5	q6	$\overline{q6}$
	H	↑	L	h	X	H	q0 to q5	q6	$\overline{q6}$
Hold "Do nothing"	H	H	X	X	X	q0	q1 to q6	q7	$\overline{q7}$
	H	X	H	X	X	q0	q1 to q6	q7	$\overline{q7}$

H = High voltage level;
h = High voltage level one set-up time prior to the Low-to-High clock transition;
L = Low voltage level;
I = Low voltage level one set-up time prior to the Low-to-High clock transition;
q = Lower case letters indicate the state of the referenced input one set-up time prior to the Low-to-High clock transition;
↑ = Low-to-High clock transition;
X = don't care;

8.1 TIMING DIAGRAM



9 SPECIFICATIONS

9.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{CC}	Supply Voltage Range		-0.5	6.5	V
I_{IK}	Input Clamp Current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V		±20	mA
I_{OK}	Output Clamp Current	V_O < -0.4V or V_O > V_{CC}+0.4V		±20	mA
I_O	Output Current	-0.5 V < V_O < V_{CC} + 0.5 V		±25	mA
I_{CC}	Supply Current			50	mA
I_{GND}	Ground Current		-50		mA
θ_{JA}	Package thermal impedance (2)	TSSOP16		108	°C/W
		SOP16		76	
T_J	Junction Temperature (3)		-40	150	°C
T_{stg}	Storage Temperature		-65	150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The package thermal impedance is calculated in accordance with JESD-51.

(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

9.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), MIL-STD-883K METHOD 3015.9	±2000	V
		Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±1000	
		Machine Model (MM), JESD22-A115C (2010)	±200	

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.3 Recommended Operating Conditions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage	V_{CC}		1.65		5.5	V
Input voltage	V_I		0		V_{CC}	V
Output voltage	V_O		0		V_{CC}	V
Input transition rise or fall rate(Δt/Δv)	Data inputs	V_{CC}=1.65V to 1.95V			20	ns/V
		V_{CC}=2.3V to 2.7V			20	
		V_{CC}=3V to 3.6V			10	
		V_{CC}=4.5V to 5.5V			5	
Operating temperature	T_A		-40		125	°C

9.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	Vcc	TEMP	MIN(1)	TYP(2)	MAX(1)	UNIT
High-level input voltage	V_{IH}		1.65V to 1.95V	25°C	0.65xV_{CCI}			V
			2.3V to 2.7V		1.7			
			3V to 3.6V		2			
			4.5V to 5.5V		0.7xV_{CCI}			
Low-level input voltage	V_{IL}		1.65V to 1.95V	25°C			0.35xV_{CCI}	V
			2.3V to 2.7V				0.7	
			3V to 3.6V				0.8	
			4.5V to 5.5V				0.3xV_{CCI}	
High-level output voltage	V_{OH}	I_{OH} = -100μA	1.65V to 5.5V	25°C	V_{CC}-0.1			V
		I_{OH} = -4mA	3V		1.2			
		I_{OH} = -8mA	3.3V		1.9			
		I_{OH} = -10mA	5.0V		3.8			
Low-level output voltage	V_{OL}	I_{OL} = 100μA	1.65V to 5.5V	25°C			0.1	V
		I_{OL} = 4mA	3V				0.45	
		I_{OL} = 8mA	3.3V				0.3	
		I_{OL} = 10mA	5.0V				0.4	
Input leakage Current	I_I	V_I=5.5V or GND	0V to 5.5V	25°C		±0.1	±1	μA
				FULL			±5	
	I_{off}	VI or VO=5.5V	0	25°C		±0.1	±1	μA
				FULL			±10	
Supply current	I_{CC}	V_I=5.5V or GND; I_O=0	1.65V to 5.5V	25°C		0.1	8	μA
				FULL			160	
	ΔI_{CC}	One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND	3V to 5.5V	FULL			500	μA
Input capacitance	C_I	f=1MHZ	3.3V	25°C		3.7		pF

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

9.5 Switching Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS	25°C (1)			-40°C to 125°C (1)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd} (2)	Propagation delay	CLK or $\overline{CE}$ to Q7 or $\overline{Q7}$							
		V_{CC}=1.8V±0.15V		44				120	ns
		V_{CC}=2.5V±0.2V		20				60	
		V_{CC}=3.3V±0.3V		14				42	
		V_{CC}=5V±0.5V		9				33	
		D7 to Q7 or $\overline{Q7}$							
		V_{CC}=1.8V±0.15V		29				120	ns
		V_{CC}=2.5V±0.2V		17				36	
		V_{CC}=3.3V±0.3V		12				24	
		V_{CC}=5V±0.5V		9				18	
		$\overline{PL}$ to Q7 or $\overline{Q7}$							
		V_{CC}=1.8V±0.15V		32				120	ns
		V_{CC}=2.5V±0.2V		17				54	
		V_{CC}=3.3V±0.3V		12				36	
		V_{CC}=5V±0.5V		8				30	
t_t (3)	transition time	Q7 or $\overline{Q7}$ output							ns
		V_{CC}=1.8V±0.15V		19				30	
		V_{CC}=2.5V±0.2V		10				15	
		V_{CC}=3.3V±0.3V		8				12	
		V_{CC}=5V±0.5V		6				9	
t_h	Hold width	SER to CLK or $\overline{CE}$							
		V_{CC}=1.8V±0.15V		-12		5	3		ns
		V_{CC}=2.5V±0.2V		-5		5	3		
		V_{CC}=3.3V±0.3V		-5		5	3		
		V_{CC}=5V±0.5V		-3		5	3		
		Dn to $\overline{PL}$							
		V_{CC}=1.8V±0.15V		-5		5	3		ns
		V_{CC}=2.5V±0.2V		-5		5	3		
		V_{CC}=3.3V±0.3V		-1.5		5	3		
		V_{CC}=5V±0.5V		-1		5	3		
t_{su}	Set-up time	SER to CLK or $\overline{CE}$							
		V_{CC}=1.8V±0.15V		11		16.5			ns
		V_{CC}=2.5V±0.2V		5		7.5			
		V_{CC}=3.3V±0.3V		5		7.5			
		V_{CC}=5V±0.5V		3		4.5			
		Dn to $\overline{PL}$							
		V_{CC}=1.8V±0.15V		5		7.5			ns
		V_{CC}=2.5V±0.2V		5		7.5			
		V_{CC}=3.3V±0.3V		1.5		2.5			
		V_{CC}=5V±0.5V		1		1.5			

t_{rec}	Recovery time	$\overline{PL}$ to CLK or $\overline{CE}$							
		V_{CC}=1.8V±0.15V		5		15			ns
		V_{CC}=2.5V±0.2V		1.5		5			
		V_{CC}=3.3V±0.3V		1		3			
		V_{CC}=5V±0.5V		1		3			
f_{max}	Maximum frequency	For CLK CL=15pF							
		V_{CC}=1.8V±0.15V		20		4			MHz
		V_{CC}=2.5V±0.2V		25		10			
		V_{CC}=3.3V±0.3V		40		20			
		V_{CC}=5V±0.5V		50		24			
t_W	Pulse width	CLK							
		V_{CC}=1.8V±0.15V		30		80			ns
		V_{CC}=2.5V±0.2V		25		60			
		V_{CC}=3.3V±0.3V		20		40			
		V_{CC}=5V±0.5V		20		22			
		$\overline{PL}$							
		V_{CC}=1.8V±0.15V		30		80			ns
		V_{CC}=2.5V±0.2V		25		60			
		V_{CC}=3.3V±0.3V		20		40			
		V_{CC}=5V±0.5V		20		22			

NOTE:
(1) This parameter is ensured by design and/or characterization and is not tested in production.
(2) t_{pd} is the same as t_{PHL} and t_{PLH}.
(3) t_t is the same as t_{THL} and t_{TLH}.

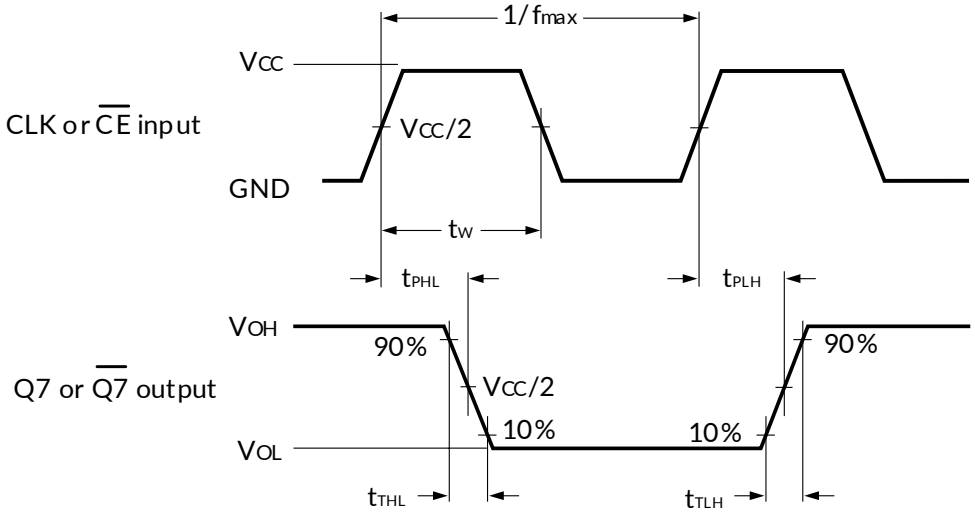
9.6 Operating Characteristics

T_A=25°C

PARAMETER	TEST CONDITIONS	V_{CC}=3.3V	V_{CC}=5V	UNIT
		TYP	TYP	
C_{pd} (1)	C_L=0, f=10MHz	11	17	pF

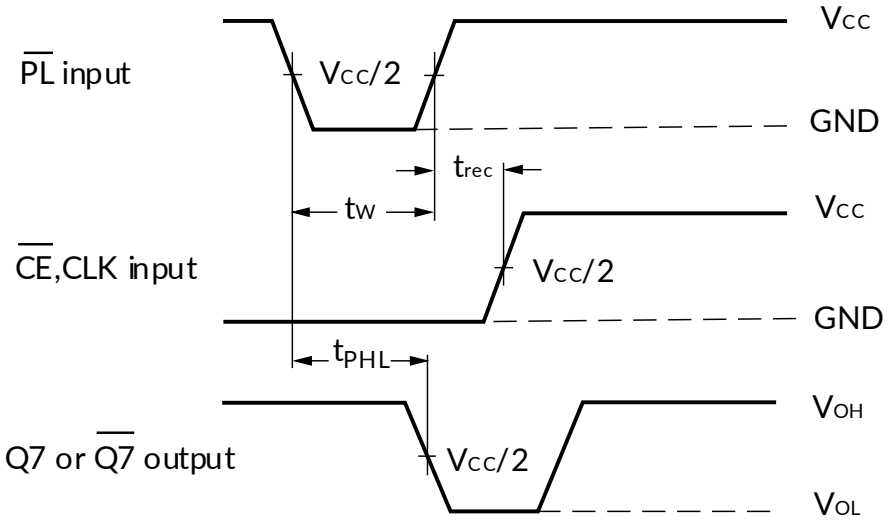
(1) Power dissipation capacitance per transceiver.

10 PARAMETER MEASUREMENT INFORMATION



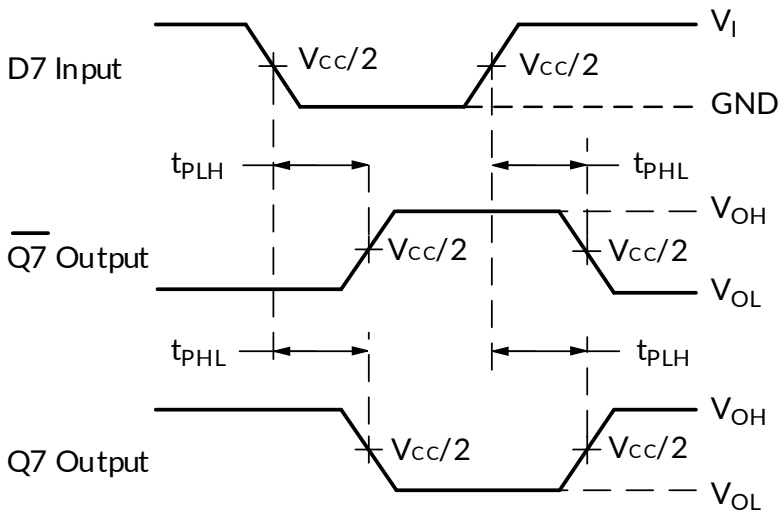
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 1. The clock (CLK) or clock enable ($\overline{CE}$) to output (Q7 or $\overline{Q7}$) propagation delays, the clock pulse width, the maximum clock frequency and the output transition times



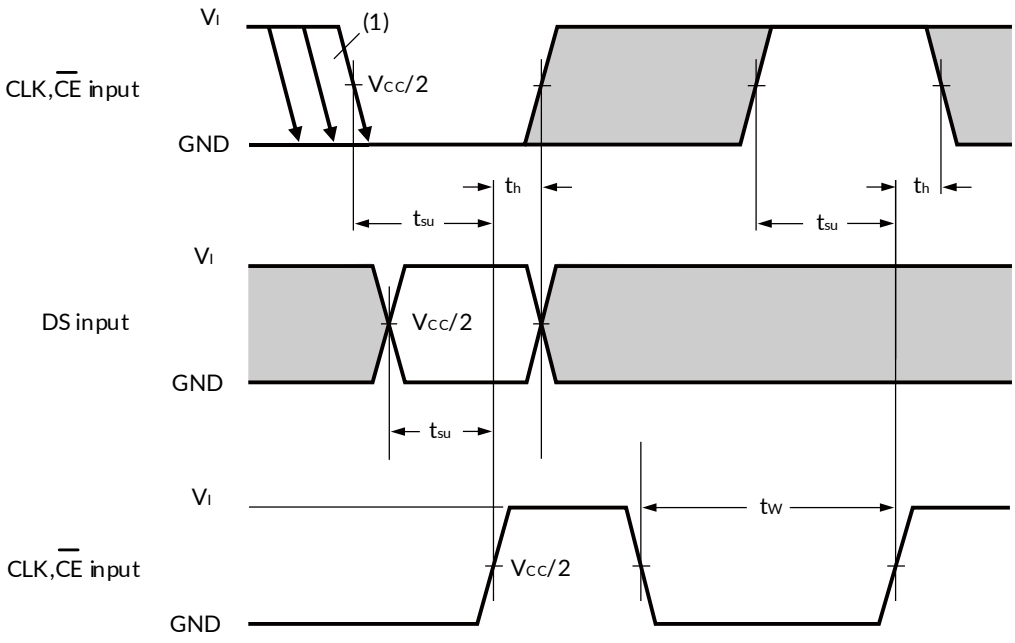
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 2. The parallel load ($\overline{PL}$) pulse width, the parallel load to output (Q7 or $\overline{Q7}$) propagation delays, the parallel load to clock (CLK) and clock enable ($\overline{CE}$) recovery time



V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

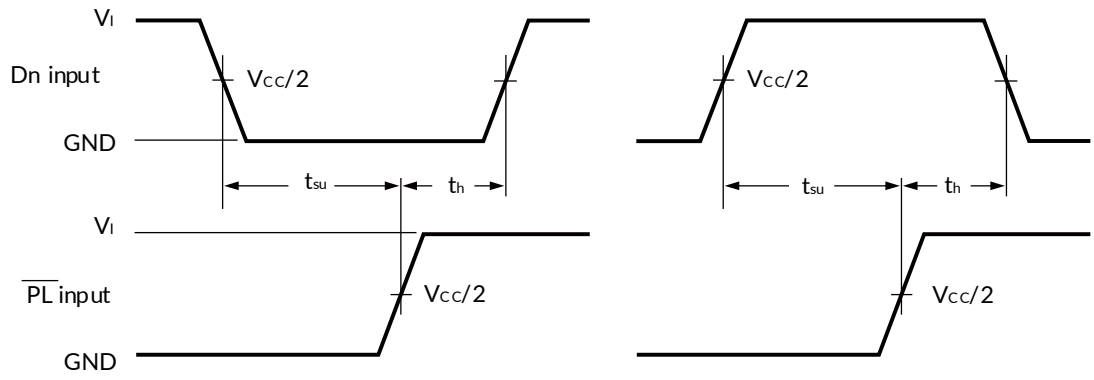
Figure 3. The data input (D7) to output (Q7 or $\overline{Q7}$) propagation delays when $\overline{PL}$ is LOW



The shaded areas indicate when the input is permitted to change for predictable output performance.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

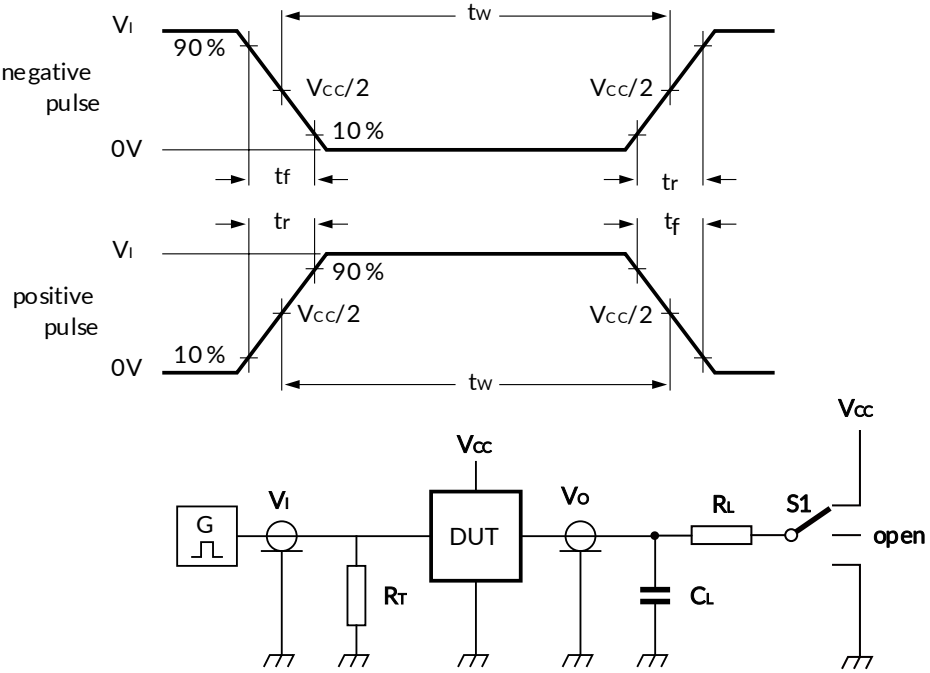
(1) $\overline{CE}$ may change only from HIGH-to-LOW while CLK is LOW, see Section 1.

Figure 4. The set-up and hold times from the serial data input (DS) to the clock (CLK) and clock enable ($\overline{CE}$) inputs, from the clock enable input ($\overline{CE}$) to the clock input (CLK) and from the clock input (CLK) to the clock enable input ($\overline{CE}$)



V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 5. The set-up and hold times from the data inputs (Dn) to the parallel load input ($\overline{PL}$)



Test data is given in Table 1.
Definitions test circuit:
R_T = termination resistance should be equal to output impedance Zo of the pulse generator.
C_L = load capacitance including jig and probe capacitance.
R_L = Load resistance.
S1 = Test selection switch.

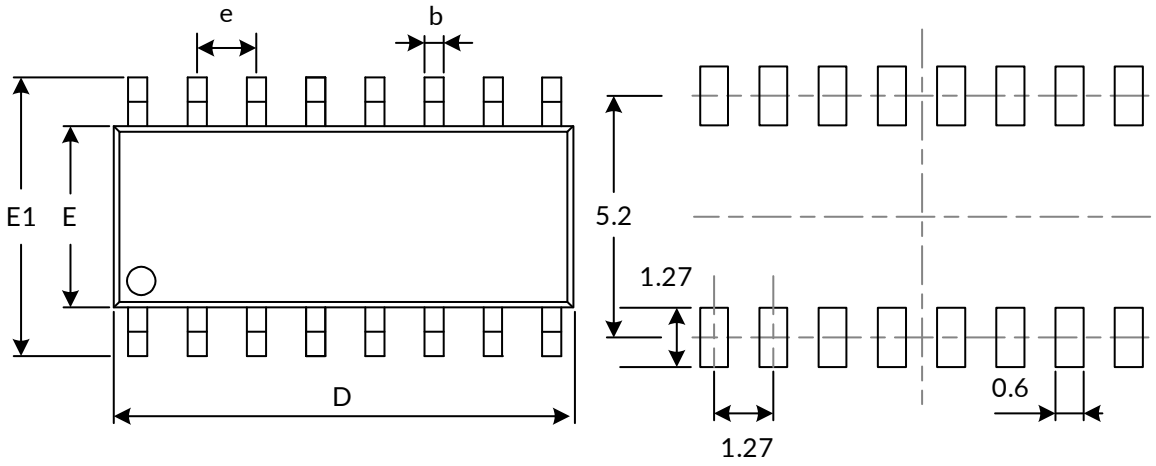
Figure 6. Test circuit for measuring switching times

Table 1. Test data

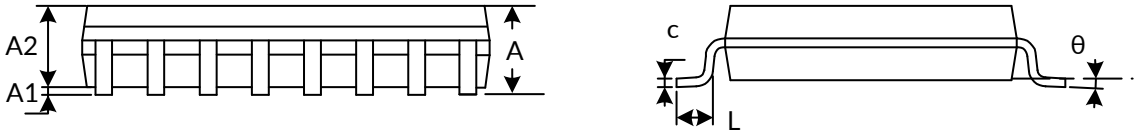
S1 position	Input		Load	
t_{PHL}/t_{PLH}	V_I	t_r, t_f	C_L	R_L
open	V_{CC}	6ns	15pF, 50pF	1kΩ

11 PACKAGE OUTLINE DIMENSIONS

SOP16 (3)



RECOMMENDED LAND PATTERN (Unit: mm)

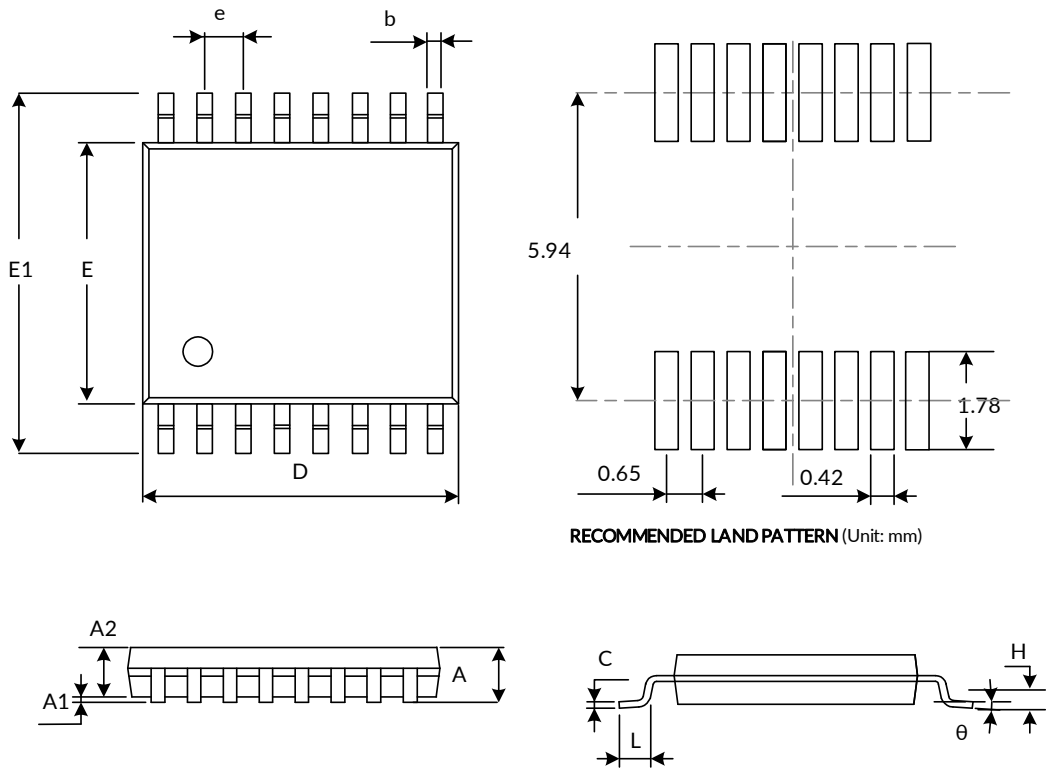


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.750		0.069
A1	0.100	0.225	0.004	0.009
A2	1.300	1.500	0.051	0.059
b	0.390	0.470	0.015	0.019
c	0.200	0.240	0.007	0.010
D (1)	9.800	10.00	0.386	0.394
E (1)	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC) (2)		0.050 (BSC) (2)	
L	0.500	0.800	0.020	0.032
θ	0°	8°	0°	8°

NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

TSSOP16 (3)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.900	1.050	0.035	0.041
b	0.200	0.280	0.007	0.011
c	0.130	0.170	0.005	0.007
D (1)	4.900	5.100	0.193	0.201
E (1)	4.300	4.500	0.169	0.177
E1	6.200	6.600	0.244	0.260
e	0.650(BSC) (2)		0.026(BSC) (2)	
L	0.450	0.750	0.017	0.030
H	0.250 TYP		0.010 TYP	
θ	0°	8°	0°	8°

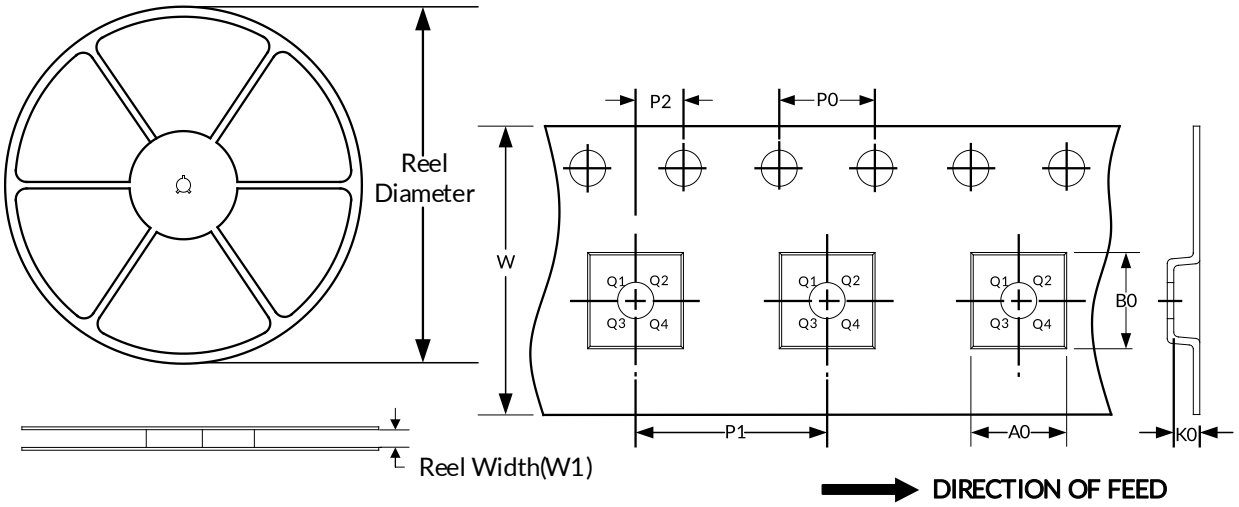
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

12 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOP16	13"	16.4	6.50	10.30	2.10	4.0	8.0	2.0	16.0	Q1
TSSOP16	13"	12.4	6.90	5.60	1.20	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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