24V, 1A Peak Output Current, Rail-to-Rail I/O Operational Amplifiers

1 FEATURES

- **Rail-to-Rail Input and Output**
- **Supply Voltage Range: 4.5V to 24V**
- **Unity-Gain Stable**
- **High Slew Rate: 65V/µs**
- **Peak Output Current: 1A**
- **Operating Temperature Range: -40°C to +85°C**
- **Micro SIZE PACKAGES: DFN3X3-8**

2 APPLICATIONS

- **TFT-LCD Panels**
- **LCD TVs**
- **Monitors**
- **Laptops**

3 DESCRIPTIONS

The RS8471 is high slew rate, low power operational amplifiers optimized for high voltage systems. These devices can operate on single or dual power supply. They support rail-to-rail input and output operation.

The RS8471 feature ±4.5mV maximum offset voltage, 1A peak output current, and 65V/µs high slew rate. The combination of characteristics makes them suitable for TFT-LCDs.

The RS8471 is available in a Green DFN3X3-8 package. The RS8471 is specified over the -40°C to +85°C temperature range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS8471	DFN3X3-8	3.00mm x 3.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 Revision History

Note: Page numbers for previous revisions may different from page numbers in the current version.

Version	Change Date	Change Item
A.0	2023/10/12	Preliminary version completed
A.0.1	2024/02/29	Modify packaging naming
A.1	2024/04/17	Initial version completed

5 PACKAGE/ORDERING INFORMATION [1]

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING [2]	MSL [3]	PACKAGE OPTION
RS8471	RS8471YTDC8	-40°C ~85°C	DFN3X3-8	RS8471	MSL3	Tape and Reel,5000

NOTE:

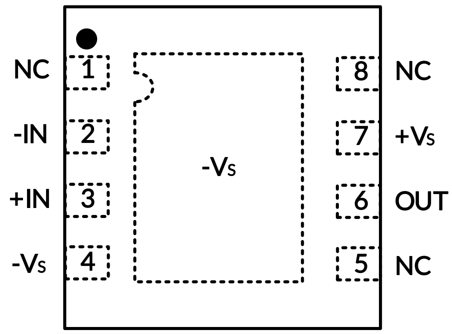
(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.

6 Pin Configuration and Functions (Top View)

TOP VIEW



DFN3X3-8

Pin Description

NAME	PIN	I/O [(1)]	DESCRIPTION
	DFN3X3-8		
NC	1,5,8	-	No connect
-IN	2	I	Negative (inverting) input
+IN	3	I	Positive (noninverting) input
-Vs	4	-	Negative (lowest) power supply or ground (for single supply operation)
OUT	6	O	Output
+Vs	7	-	Positive (highest) power supply

(1) I = Input, O = Output.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Voltage	Supply, Vs=(+V_S) - (-V_S)		-0.3	28	V
	Signal input pin (2)		(-V_S)-0.3	(+V_S)+0.3	
	Signal output pin (3)		(-V_S)-0.3	(+V_S)+0.3	
Current	Signal input pin (2)		-10	10	mA
θ_{JA}	Package thermal impedance (4)	DFN3X3-8		45	°C/W
Temperature	Operating range, T_A		-40	85	°C
	Junction, T_J (5)		-40	150	
	Storage, T_{stg}		-65	150	

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current-limited to 10mA or less.
(3) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.3V beyond the supply rails should be current-limited to ±500mA or less.
(4) The package thermal impedance is calculated in accordance with JESD-51.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), MIL-STD-883K METHOD 3015.9	±2000	V
		Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±1000	
		Machine Model (MM), JESD22-A115C (2010)	±300	

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage，Vs= (+V_S) - (-V_S)	Single-supply	4.5		24	V
	Dual-supply	±2.25		±12	

7.4 ELECTRICAL CHARACTERISTICS

(At T_A = +25°C, $+V_S$=24V, $-V_S$=0V, $+V_{IN}$=V_{OUT}=$+V_S/2$, FULL=-40°C ~+85°C, unless otherwise noted.) [1]

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN[2]	TYP[3]	MAX[2]	UNIT
POWER SUPPLY							
Supply Voltage Range	V_S		25°C	4.5		24	V
Quiescent Current Per Amplifier	I_Q	No load	25°C		5.5	8.5	mA
Power-Supply Rejection Ratio	PSRR	V_S=4.5V to 24V, V_{CM}=$+V_S/2$	25°C	80	90		dB
INPUT CHARACTERISTICS							
Input Offset Voltage	V_{OS}	V_{CM}=$+V_S/2$	25°C	-4.5	±1	4.5	mV
Input Offset Voltage Average Drift	$V_{OS}\ T_C$	V_{CM}=$+V_S/2$	25°C		±6		µV/°C
Input Bias Current [4] [5]	I_B	V_{CM}=$+V_S/2$	25°C		100		pA
Load Regulation	ΔV_{LOAD}	I_{OUT}=0mA to -80mA	25°C		0.01		mV/mA
		I_{OUT}=0mA to 80mA	25°C		-0.01		
Common-Mode Voltage Range	V_{CM}		25°C	$-V_S$		$+V_S$	V
Common-Mode Rejection Ratio	CMRR	0V≤V_{CM}≤($+V_S$)	25°C	60	68		dB
Open-Loop Voltage Gain	A_{OL}	0.1V≤V_{CM}≤($+V_S$)-0.1V, R_L = 10kΩ	25°C	110	130		dB
NOISE PERFORMANCE							
Input Voltage Noise	e_{np-p}	f= 0.1Hz to 10Hz	25°C		20		μV_{PP}
Input Voltage Noise Density	e_n	f= 1kHz	25°C		45		$nV/\sqrt{HZ}$
DYNAMIC PERFORMANCE							
Slew Rate [8]	SR	8V step, 20% to 80%, A_V=1	25°C		65		V/µs
Gain-Bandwidth Product	GBP		25°C		25		MHz
Phase Margin	φ_O	R_L = 10kΩ, C_L=40pF	25°C		32		°
Settling Time to ±0.1%	t_s	A_V = 1, V_{OUT} = 8V step, R_L = 10kΩ, C_L=40PF	25°C		350		ns
OUTPUT CHARACTERISTICS							
Output Voltage Swing	V_{OH}	I_L = 50mA	25°C	($+V_S$)-0.27	($+V_S$)-0.12		V
	V_{OL}	I_L = -50mA	25°C		($-V_S$)+0.08	($-V_S$)+0.17	
Continuous Output Current [6] [7]	I_{OUT}		25°C		±400		mA
Transient Peak Output Current	I_{PK}		25°C		±1		A
Thermal Protection							
Thermal Shutdown Temperature	T_{SHDN}				150		°C
Thermal Shutdown Hysteresis	ΔT_{SHDN}				25		°C

NOTE:

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

(4) Positive current corresponds to current flowing into the device.

(5) This parameter is ensured by design and/or characterization and is not tested in production.

(6) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is PD = ($T_{J(MAX)}$ - T_A) / $R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

(7) Short circuit test is a momentary test.

(8) Number specified is the slower of positive and negative slew rates.

7.5 TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

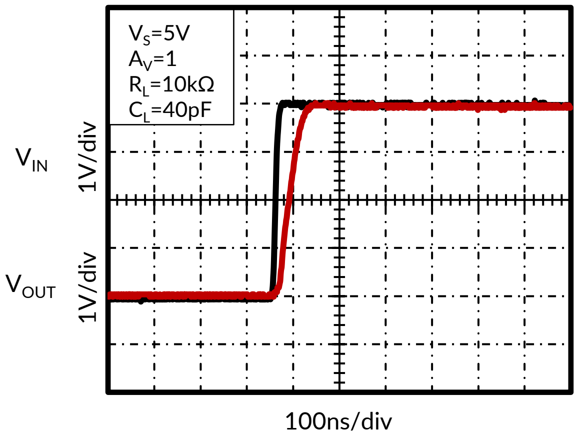


Figure 1. Large-Signal Transient Response

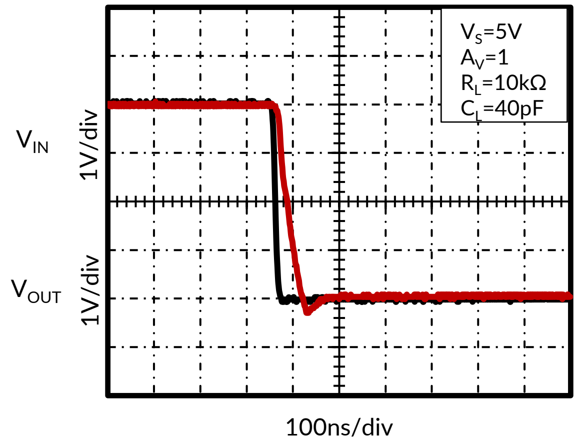


Figure 2. Large-Signal Transient Response

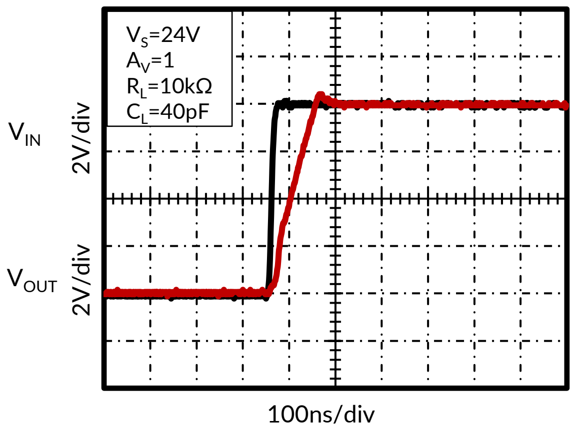


Figure 3. Large-Signal Transient Response

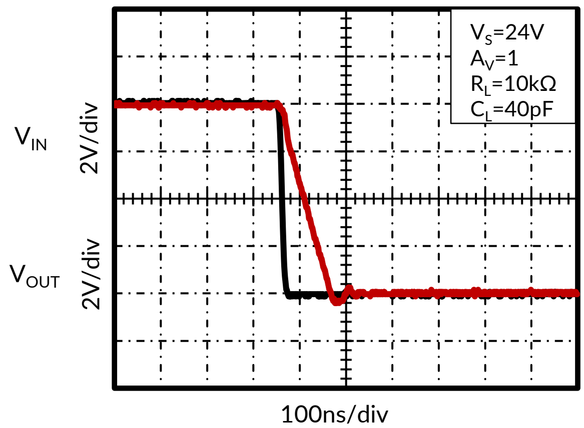


Figure 4. Large-Signal Transient Response

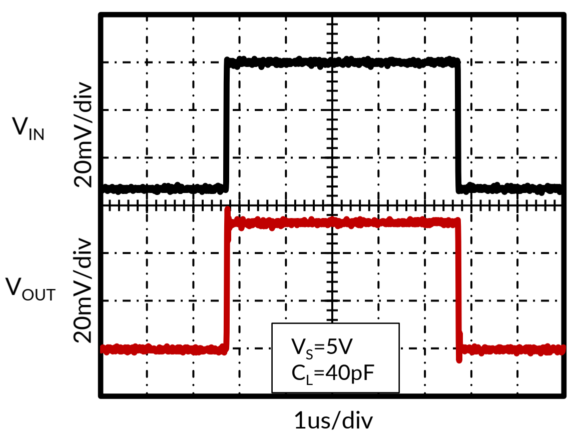


Figure 5. Small-Signal Transient Response

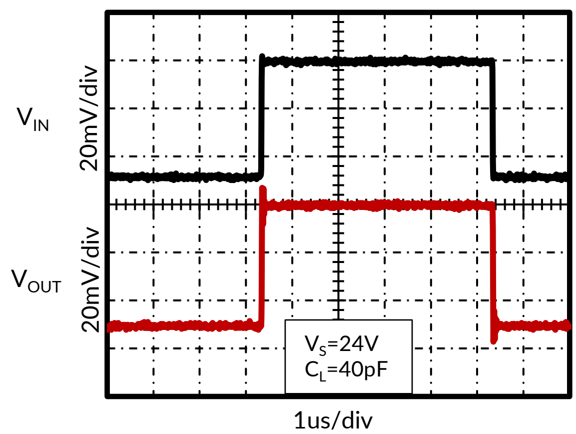


Figure 6. Small-Signal Transient Response

8 Application and Implementation

Information in the following applications sections is not part of the RUNIC component specification, and RUNIC does not warrant its accuracy or completeness. RUNIC's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The RS8471 are specifically designed to drive high current load. These devices support rail-to-rail input and output operation, and consume low quiescent current. They can also provide a high slew rate. The combination of characteristics makes RS8471 suitable for LCD applications.

8.2 Operating Voltage

The RS8471 are guaranteed to operate from 4.5V to 24V, and the operation is extremely stable over the whole specified range of the temperature. The output voltage swing can be closer to the supply rail by reducing the load current.

8.3 LCD Panel Application

The RS8471 can provide optimal performance in LCD V_{COM} buffer. They feature ±1A transient peak source/sink current.

8.4 Output Current Limit

The RS8471 can drive ±1A transient peak output current. These devices have a ±1A (TYP) current limit, which is accomplished with the characteristics of the internal metal interconnects. Maximum reliability is maintained if the output continuous current never exceeds ±400mA.

8.5 Thermal Consideration

When operating the devices, the users need to make sure that the junction temperature is below the absolute maximum one. The junction temperature is increasing because the power dissipation is higher than before. And a lot of possibilities can cause the thermal considerations, such as the width of trace in PCB, the package of the devices, the gap between ambient and junction temperature and rate of environmental airflow.

The following equation indicates the calculation of power dissipation:

$$P_{D(MAX)}=(T_{J(MAX)}-T_A) / \theta_{JA} \quad (1)$$

where:

$T_{J(MAX)}$ = Maximum junction temperature.

T_A = Ambient temperature.

θ_{JA} = Junction to ambient thermal resistance.

It is recommended that the junction temperature should not exceed +125℃ for normal operation. The parameter of ambient thermal resistance is determined by the width of trace in PCB layout.

In addition, the ambient temperature and thermal resistance will affect the power dissipation of RS8471.

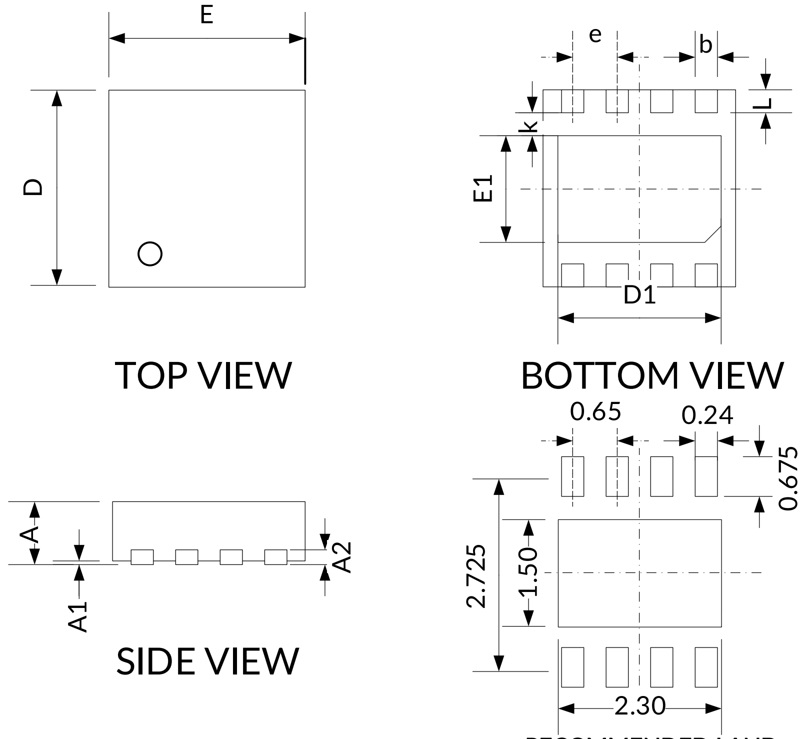
9 Layout

For the circuits with high power path, a good PCB design is essential. It is recommended to use the following layout method to improve the performance of RS8471 at most.

- The power component should be close enough to RS8471 for better performance. Also, if the high current is necessary, the corresponding trace in PCB should be short and wide.
- For some applications such as filtering, a series resistor is necessary to be added at the output of the devices.
- Choosing a suitable bypass capacitor can enhance the stability when driving the loads with high transient. For single-supply operation, the bypass capacitor should be placed as close to $+V_S$ pin as possible. For dual-supply operation, both $+V_S$ and $-V_S$ supplies should be bypassed to ground with separate 0.1μF ceramic capacitors. Using a 10μF tantalum capacitor is a good choice to improve the operating stability of the devices when driving high transient load.
- A 0.1μF capacitor should be connected with +IN pin to GND for better operation of RS8471 and the distance between this capacitor and +IN pin should be minimized.
- It is recommended to connect exposed pad to $-V_S$ directly in the PCB.

10 PACKAGE OUTLINE DIMENSIONS

DFN3X3-8 (3)



RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203REF (2)		0.008REF (2)	
b	0.180	0.300	0.007	0.012
k	0.200MIN		0.008MIN	
D (1)	2.900	3.100	0.114	0.122
D1	2.200	2.400	0.087	0.094
E (1)	2.900	3.100	0.114	0.122
E1	1.400	1.600	0.055	0.063
e	0.650 TYP		0.026 TYP	
L	0.375	0.575	0.015	0.023

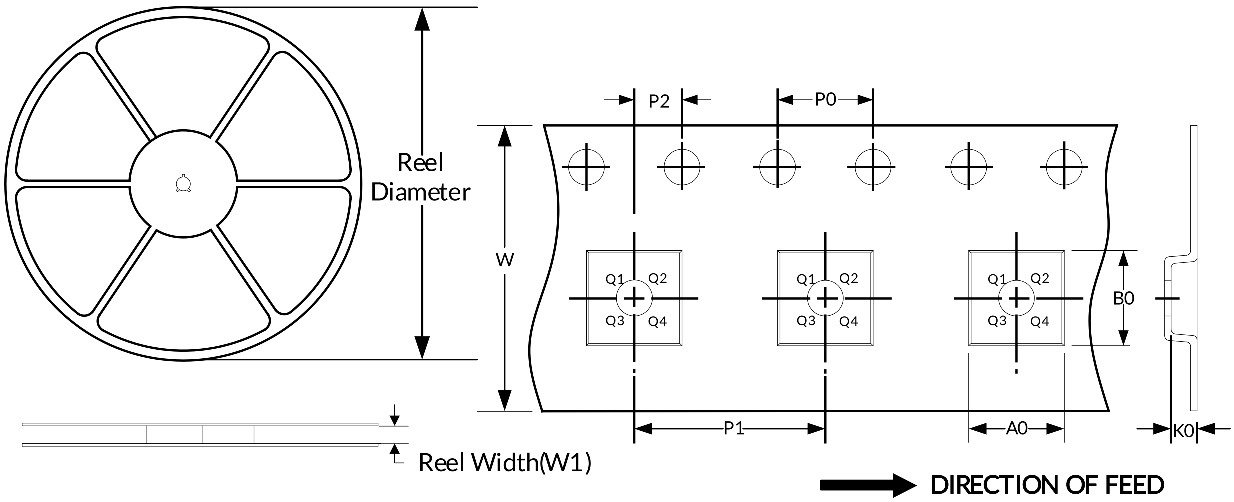
NOTE:

1. Plastic or metal protrusions of 0.075mm maximum per side are not included.
2. REF is the abbreviation for Reference.
3. This drawing is subject to change without notice.

11 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
DFN3X3-8	13”	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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