

# Octal Buffer/Driver With 3-State Outputs

## 1 FEATURES

- **Power-Supply Range: 4.5V to 5.5V**
- **3-State Outputs Drive Bus Lines**
- **Low Power Consumption: 40uA I<sub>cc</sub>(Max)**
- **TTL Input are compatible**
- **V<sub>CC</sub> Isolation: If V<sub>CC</sub> is at GND, Both Ports are in the High-Impedance State**
- **I<sub>OFF</sub>: Supports Partial-Power-Down Mode Operation**
- **Extended Temperature: -40°C to +125°C**
- **Micro Size Packages: TSSOP20, SOP20**

## 2 APPLICATIONS

- Servers
- LED Displays
- Network Switches
- Power Infrastructure
- Motor Drivers
- I/O Expanders
- Tests and Measurements

## 3 DESCRIPTIONS

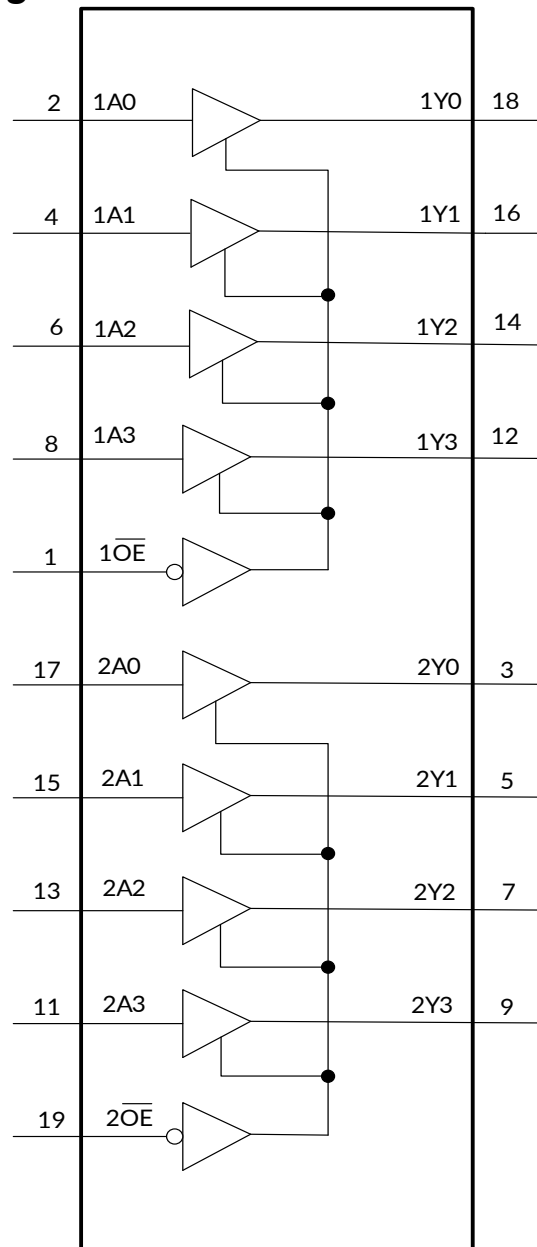
The RS244T is organized as two 4-bit buffers or drivers with separate output enable ( $\overline{OE}$ ) inputs. The 3-state outputs are controlled by the output enable inputs  $1\overline{OE}$  and  $2\overline{OE}$ . A HIGH on  $\overline{OE}$  causes the outputs are in the high-impedance state. While A Low on  $\overline{OE}$ , the devices passes data from input A to output Y. Supply voltage operates from 4.5 V to 5.5 V.

**Device Information** <sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS244T	TSSOP20	6.50mm×4.40mm
	SOP20	12.80mm×7.50mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### 4 Functional Block Diagram



**Function Table**

INPUTS		OUTPUT
$\overline{OE}$	A PORT	Y PORT
L	H	H
L	L	L
H	X	Hi-Z

NOTE:  
H=HIGH voltage level  
L=LOW voltage level  
X=Don't care  
Z=High impedance OFF-state

## Table of Contents

<b>1 FEATURES</b>	1
<b>2 APPLICATIONS</b>	1
<b>3 DESCRIPTIONS</b>	1
<b>4 Functional Block Diagram</b>	2
<b>5 Revision History</b>	4
<b>6 PACKAGE/ORDERING INFORMATION</b> <sup>(1)</sup>	5
<b>7 PIN CONFIGURATIONS</b>	6
<b>8 SPECIFICATIONS</b>	7
8.1 Absolute Maximum Ratings	7
8.2 ESD Ratings	7
8.3 Recommended Operating Conditions	8
8.4 Electrical Characteristics	8
8.5 Switching Characteristics	9
8.6 Operating Characteristics	9
8.7 Typical Characteristics	9
<b>9 Parameter Measurement Information</b>	10
<b>10 Detailed Description</b>	11
10.1 Overview	11
10.2 Feature Description	11
<b>11 Application and Implementation</b>	12
11.1 Application Information	12
11.2 Typical Application	12
11.3 Design Requirements	12
<b>12 Power Supply Recommendations</b>	12
<b>13 Layout</b>	13
13.1 Layout Guidelines	13
13.2 Layout Example	13
<b>14 PACKAGE OUTLINE DIMENSIONS</b>	14
<b>15 TAPE AND REEL INFORMATION</b>	16

## 5 Revision History

Note: Page numbers for previous revisions may differ from page numbers in the current version.

VERSION	Change Date	Change Item
A.1	2023/04/24	Initial version completed
A.2	2023/09/06	Update PACKAGE OUTLINE DIMENSIONS
A.2.1	2024/02/26	Modify packaging naming
A.3	2024/05/17	Update KEY PARAMETER LIST OF TAPE AND REEL

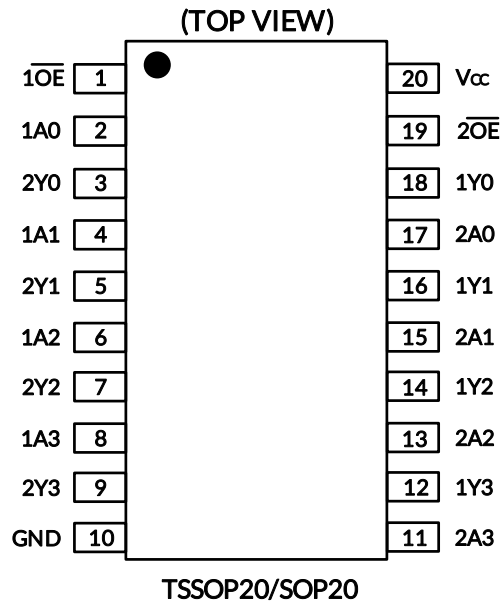
**6 PACKAGE/ORDERING INFORMATION (1)**

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING (2)	MSL (3)	PACKAGE OPTION
RS244T	RS244TXTSS20	-40°C ~+125°C	TSSOP20	RS244T	MSL3	Tape and Reel,4000
	RS244TXS20	-40°C ~+125°C	SOP20	RS244T	MSL3	Tape and Reel,1500

## NOTE:

- (1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.
- (2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.
- (3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.

## 7 PIN CONFIGURATIONS



### PIN DESCRIPTION

PIN	NAME	TYPE <sup>(1)</sup>	FUNCTION
TSSOP20/SOP20			
1	$\overline{10E}$	I	Output Enable (Active Low). Pull $\overline{10E}$ high to place all outputs in 3-state mode
2	1A0	I	Input
3	2Y0	O	Output
4	1A1	I	Input
5	2Y1	O	Output
6	1A2	I	Input
7	2Y2	O	Output
8	1A3	I	Input
9	2Y3	O	Output
10	GND	G	Ground
11	2A3	I	Input
12	1Y3	O	Output
13	2A2	I	Input
14	1Y2	O	Output
15	2A1	I	Input
16	1Y1	O	Output
17	2A0	I	Input
18	1Y0	O	Output
19	$\overline{20E}$	I	Output Enable (Active Low). Pull $\overline{20E}$ high to place all outputs in 3-state mode
20	V <sub>cc</sub>	P	Supply voltage. 4.5V ≤ V <sub>cc</sub> ≤ 5.5V

(1) I=input, O=output, P=power, G= Ground.

## 8 SPECIFICATIONS

### 8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

SYMBOL	PARAMETER		MIN	MAX	UNIT
V <sub>CC</sub>	Supply Voltage Range		-0.5	7	V
V <sub>I</sub> <sup>(2)</sup>	Input Voltage Range		-0.5	V <sub>CC</sub> +0.5	V
V <sub>O</sub> <sup>(2)(3)</sup>	Output Voltage Range		-0.5	V <sub>CC</sub> +0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> <0 or V <sub>I</sub> >V <sub>CC</sub>		±20	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> <0 or V <sub>O</sub> >V <sub>CC</sub>		±20	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		±50	mA
	Continuous current through V <sub>CC</sub> or GND			±200	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(4)</sup>	TSSOP20		40	°C/W
		SOP20		40	
T <sub>J</sub>	Junction Temperature <sup>(5)</sup>		-40	150	°C
T <sub>stg</sub>	Storage temperature		-65	150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V<sub>CC</sub> are provided in the recommended operating conditions table.

(4) The package thermal impedance is calculated in accordance with JESD-51.

(5) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, R<sub>θJA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(MAX)</sub> - T<sub>A</sub>) / R<sub>θJA</sub>. All numbers apply for packages soldered directly onto a PCB.

### 8.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-Body Model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-Device Model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1000	V
		Machine Model (MM)	±200	V

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.



#### ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.3 Recommended Operating Conditions

V<sub>CC</sub> is the supply voltage associated with the input port and output port. <sup>(1)(2)</sup>

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V <sub>CC</sub>		4.5		5.5	V
High-Level Input Voltage	V <sub>IH</sub>	V <sub>CC</sub> =4.5V to 5.5V	2			V
Low-Level Input Voltage	V <sub>IL</sub>	V <sub>CC</sub> =4.5V to 5.5V			0.8	V
Input Voltage	V <sub>I</sub>		0		V <sub>CC</sub>	V
Output Voltage	V <sub>O</sub>		0		V <sub>CC</sub>	V
High-Level Output Current	I <sub>OH</sub>	V <sub>CC</sub> =4.5V to 5.5V			-24	mA
Low-Level Output Current	I <sub>OL</sub>	V <sub>CC</sub> =4.5V to 5.5V			24	mA
Input transition rise or fall rate	Δt/Δv	V <sub>CC</sub> =4.5V to 5.5V			8	ns/V
Operating free-air Temperature	T <sub>A</sub>		-40		125	°C

(1) All unused or driven (floating) data inputs (I/Os) of the device must be held at logic HIGH or LOW (preferably V<sub>CC</sub> or GND) to ensure proper device operation and minimize power.

(2) All unused control inputs must be held at V<sub>CC</sub> or GND to ensure proper device operation and minimize power consumption.

### 8.4 Electrical Characteristics

over recommended operating free-air temperature range (TYP values are at T<sub>A</sub> = +25°C, Full=-40°C to 125°C, unless otherwise noted).

PARAMETER	CONDITIONS	V <sub>CC</sub>	TEMP	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -50μA	4.5V	Full	4.4			V
		5.5V		5.4			
	I <sub>OH</sub> = -24mA	4.5V		3.76			
		5.5V		4.76			
	I <sub>OH</sub> = -50mA	5.5V		3.85			
	V <sub>OL</sub>	I <sub>OL</sub> = 50μA		4.5V			
5.5V					0.1		
I <sub>OL</sub> = 24mA		4.5V			0.73		
		5.5V			0.69		
I <sub>OL</sub> = 50mA		5.5V			1.65		
I <sub>I</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	5.5V	+25°C			±1
	Full					±2	
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5V	0V	+25°C			±1	μA
			Full			±2	
I <sub>oz</sub> <sup>(3)</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	5.5V	+25°C			±1	μA
			Full			±2.5	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(4)</sup> I <sub>O</sub> = 0	5.5V	+25°C			4	μA
			Full			40	
ΔI <sub>CC</sub>	One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>	5.5V	+25°C		0.6		mA
			Full			1.5	
C <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5V	+25°C		3.3		pF
C <sub>O</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5V	+25°C		5.5		pF

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

(3) For I/O ports, the parameter I<sub>oz</sub> includes the input leakage current.

(4) Hold all unused data inputs of the device at V<sub>CC</sub> or GND to assure proper device operation.



## 8.5 Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted).

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A=25^\circ\text{C}^{(1)}$			$T_A=-40\sim 125^\circ\text{C}^{(1)}$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PLH}$	An	Yn	2.5	5.1	8.1	2.4		9.3	ns
$t_{PHL}$			2.4	5.0	8.0	2.3		9.0	
$t_{PHZ}$	$\overline{OE}$	Yn	2.1	4.6	7.8	2.0		8.4	ns
$t_{PLZ}$			2.6	5.4	8.4	2.4		9.9	
$t_{PZH}$	$\overline{OE}$	Yn	3.0	6.4	12.0	2.0		13.0	ns
$t_{PZL}$			1.4	3.3	5.7	1.1		9.5	

(1) This parameter is ensured by design and/or characterization and is not tested in production.

## 8.6 Operating Characteristics

$T_A=25^\circ\text{C}$

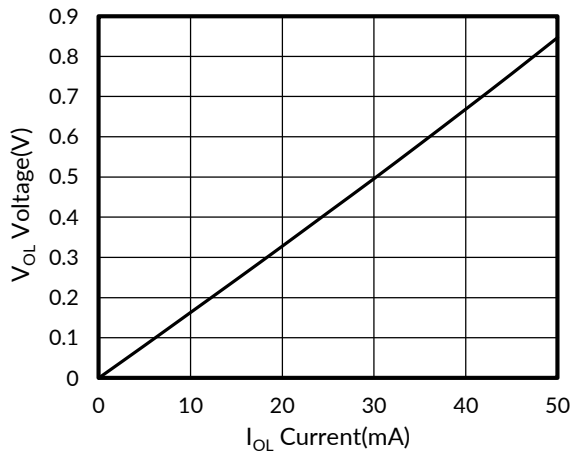
PARAMETER		TEST CONDITIONS	$V_{CC}=5\text{V}$	UNIT
			TYP	
$C_{pd}^{(1)}$	Power dissipation capacitance per buffer/driver	$C_L = 50\text{ pF}, f = 1\text{ MHz}$	39	pF

(1) Power dissipation capacitance per transceiver.

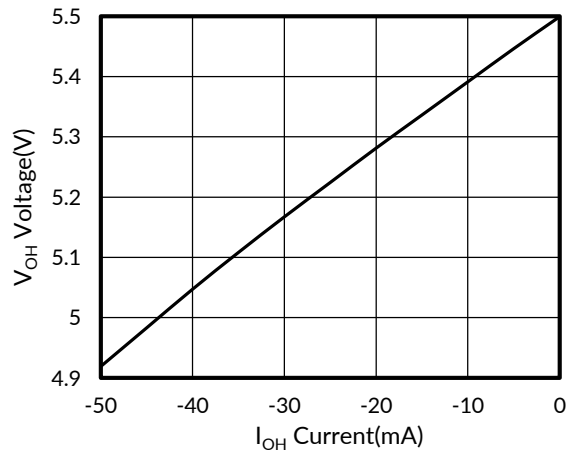
## 8.7 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At  $T_A = +25^\circ\text{C}$ ,  $V_{CC}=5.5\text{V}$ , unless otherwise noted.

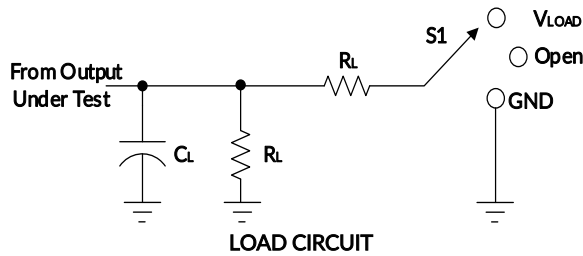


**Figure 1. Voltage vs Current**



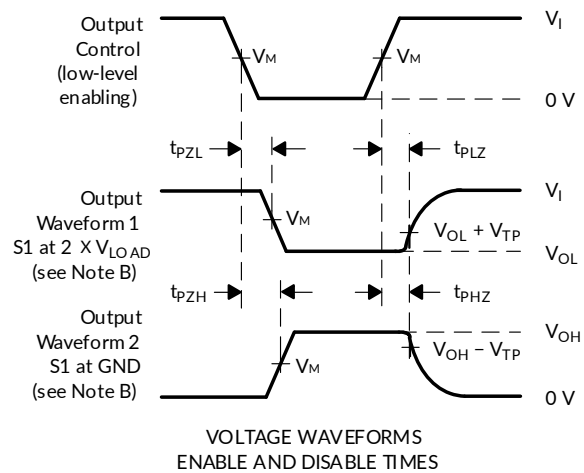
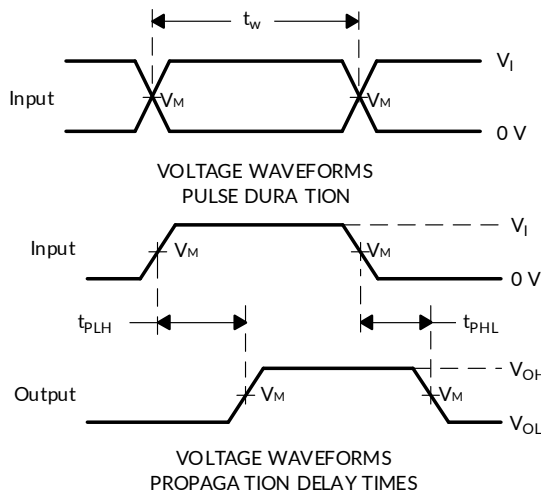
**Figure 2. Voltage vs Current**

## 9 Parameter Measurement Information



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	$V_I$	$V_M$	$C_L$	$R_L$	$V_{TP}$
$5V \pm 0.5V$	2.7V	1.5V	15pF	2k $\Omega$	0.3V



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_o = 50 \Omega$ ,  $dv/dt \geq 1V/ns$ .

D. The outputs are measured one at a time, with one transition per measurement.

E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .

F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

H. All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**

## 10 Detailed Description

### 10.1 Overview

The RS244T is organized as two 4-bit buffers or drivers with separate output enable ( $\overline{OE}$ ) inputs. The 3-state outputs are controlled by the output enable inputs  $1\overline{OE}$  and  $2\overline{OE}$ . A HIGH on  $\overline{OE}$  causes the outputs are in the high-impedance state. While A Low on  $\overline{OE}$ , the devices passes data from input A to output Y. To ensure the high-impedance state during power up or power down,  $\overline{OE}$  must be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 10.2 Feature Description

The RS244T device can drive up to 15 LSTTL loads. This device has low power consumption of  $40\mu A I_{CC}$ . The RS244T also has 3 state outputs that allow the outputs to go to high impedance, low or high.

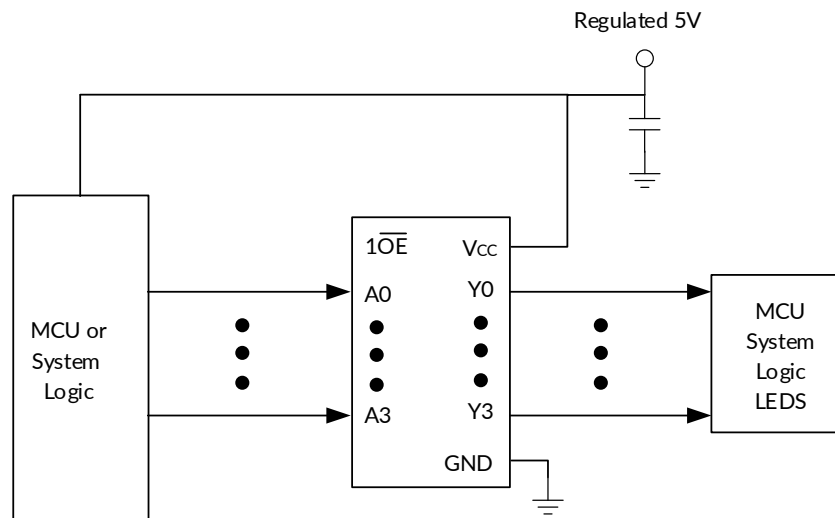
## 11 Application and Implementation

Information in the following applications sections is not part of the Runic component specification, and Runic does not warrant its accuracy or completeness. Runic's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 11.1 Application Information

The RS244T is a high-drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern.

### 11.2 Typical Application



**Figure 4. Application Schematic**

### 11.3 Design Requirements

This device uses CMOS technology and has balanced output drive. Avoid bus contention because it can drive currents in excess of maximum limits. The high drive creates fast edges into light loads, so consider routing and load conditions to prevent ringing.

## 12 Power Supply Recommendations

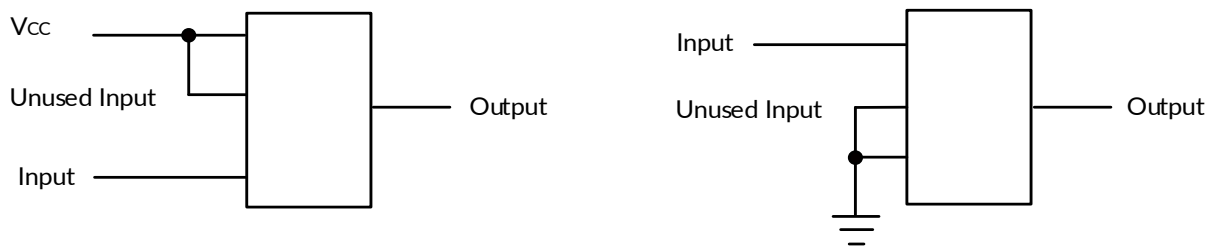
The power supply pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1uF capacitor is recommended and if there are multiple V<sub>cc</sub> terminals then 0.01uF or 0.022uF capacitors are recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor must be installed as close to the power terminal as possible for the best results.

## 13 Layout

### 13.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally, they will be tied to GND or  $V_{CC}$  whichever make more sense or is more convenient.

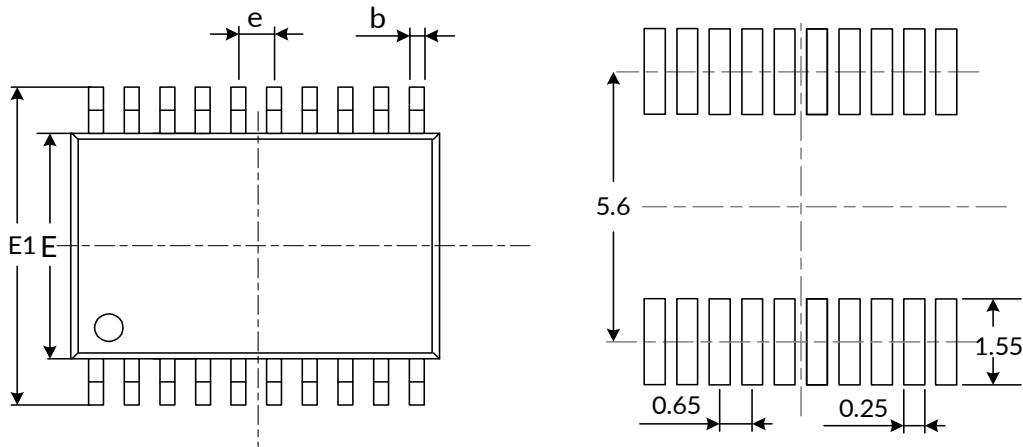
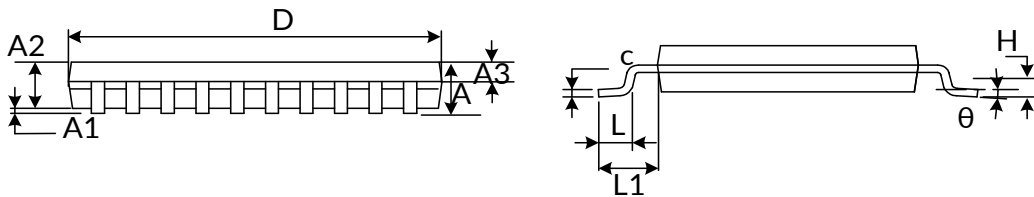
### 13.2 Layout Example



**Figure 5. Layout Diagram**

# 14 PACKAGE OUTLINE DIMENSIONS

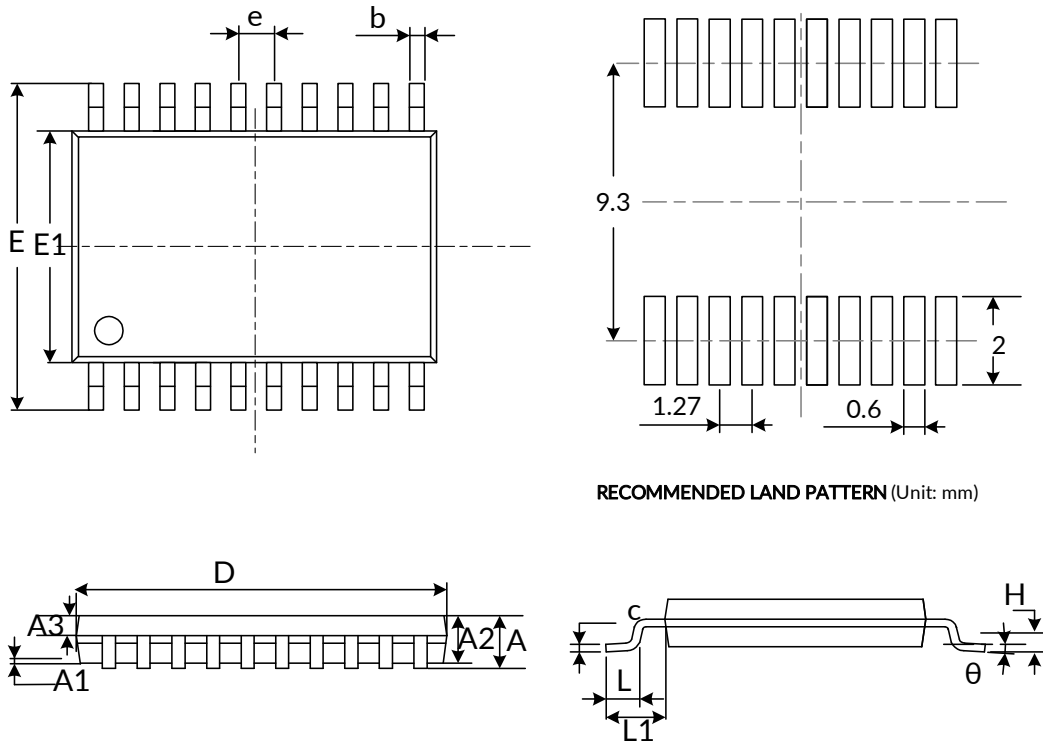
## TSSOP20<sup>(4)</sup>


**RECOMMENDED LAND PATTERN (Unit: mm)**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A <sup>(1)</sup>		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
A3	0.390	0.490	0.015	0.020
b	0.200	0.290	0.008	0.011
c	0.130	0.170	0.005	0.007
D <sup>(1)</sup>	6.400	6.600	0.252	0.260
E <sup>(1)</sup>	4.300	4.500	0.169	0.177
E1	6.200	6.600	0.244	0.260
e	0.650(BSC) <sup>(2)</sup>		0.026(BSC) <sup>(2)</sup>	
L	0.450	0.750	0.018	0.030
H	0.250(TYP)		0.010(TYP)	
θ	0°	8°	0°	8°
L1	1.00(REF) <sup>(3)</sup>		0.039(REF) <sup>(3)</sup>	

**NOTE:**

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. REF is the abbreviation for Reference.
4. This drawing is subject to change without notice.

**SOP20<sup>(4)</sup>**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A <sup>(1)</sup>		2.650		0.104
A1	0.100	0.300	0.004	0.012
A2	2.250	2.350	0.089	0.093
A3	0.970	1.070	0.038	0.042
b	0.390	0.470	0.015	0.019
c	0.250	0.290	0.010	0.011
D <sup>(1)</sup>	12.700	12.900	0.500	0.508
E	10.100	10.500	0.398	0.413
E1 <sup>(1)</sup>	7.400	7.600	0.291	0.299
e	1.270(BSC) <sup>(2)</sup>		0.050(BSC) <sup>(2)</sup>	
L	0.700	1.000	0.028	0.039
H	0.250(TYP)		0.010(TYP)	
θ	0°	8°	0°	8°
L1	1.400(REF) <sup>(3)</sup>		0.055(REF) <sup>(3)</sup>	

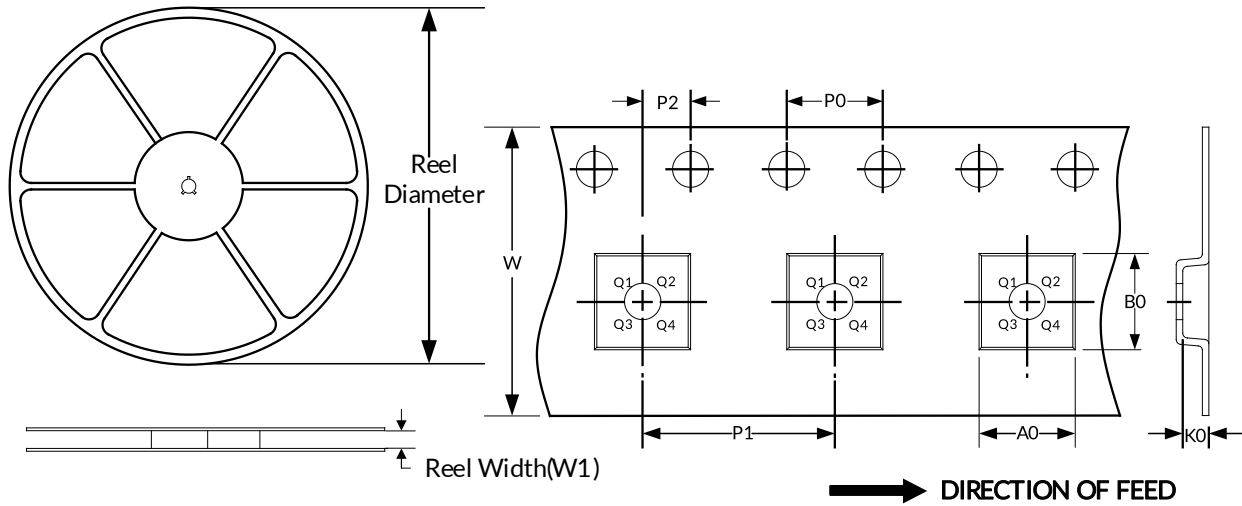
**NOTE:**

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. REF is the abbreviation for Reference.
4. This drawing is subject to change without notice.

# 15 TAPE AND REEL INFORMATION

## REEL DIMENSIONS

## TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

### KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP20	13"	12.4	6.75	6.95	1.20	4.0	8.0	2.0	16.0	Q1
SOP20	13"	24.4	10.75	13.55	2.65	4.0	12.0	2.0	24.0	Q1

NOTE:

1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.



## IMPORTANT NOTICE AND DISCLAIMER

Jiangsu Runic Technology Co., Ltd. will accurately and reliably provide technical and reliability data (including data sheets), design resources (including reference designs), application or other design advice, WEB tools, safety information and other resources, without warranty of any defect, and will not make any express or implied warranty, including but not limited to the warranty of merchantability Implied warranty that it is suitable for a specific purpose or does not infringe the intellectual property rights of any third party.

These resources are intended for skilled developers designing with Runic products You will be solely responsible for: (1) Selecting the appropriate products for your application; (2) Designing, validating and testing your application; (3) Ensuring your application meets applicable standards and any other safety, security or other requirements; (4) Runic and the Runic logo are registered trademarks of Runic Incorporated. All trademarks are the property of their respective owners; (5) For change details, review the revision history included in any revised document. The resources are subject to change without notice. Our company will not be liable for the use of this product and the infringement of patents or third-party intellectual property rights due to its use.