High-speed CAN Transceiver with standby mode

1 FEATURES

- **Fully compatible with the ISO11898-2 standard**
- **I/O voltage range supports 3.3V and 5V MCU**
- **Power supply voltage**
  - VIO: 3V to 5.5V
  - VCC: 4.5V to 5.5V
- **Bus fault protection of -70V to +70V**
- **Transmit data (TXD) dominant time out function**
- **Bus dominant time out function in standby mode**
- **Very low-current Standby mode with wake-up capability**
- **Over current and over temperature protection**
- **Date rate: up to 5Mbps**
- **Low loop delay: <250ns**
- **Operating Temperature Range: -40°C to 125°C**
- **Micro Size Packages: SOP8**

2 APPLICATIONS

- **5Mbps operation in highly loaded CAN networks down to 10 kbps networks using TXD DTO**
- **Industrial automation, control, sensors, and drive systems**
- **Building, security, and climate control automation**
- **CAN bus standards such as CANopen, DeviceNet, NMEA2000, ARNIC825, ISO11783 and CANaerospace**

3 DESCRIPTIONS

The RS1042 is a high-speed CAN transceiver that provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The RS1042 implements the CAN physical layer as defined in ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s. The RS1042 provides thermal protection and transmit data dominant time out function.

This device available in Green SOP8 packages. It operates over an ambient temperature range of -40°C to 125°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS1042	SOP8	4.90mm×3.90mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2025/09/15	Preliminary version completed
A.0.1	2026/11/09	1. Add ESD Ratings 2. Update Electrical Characteristics and Switching Electrical Characteristics

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5 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING (2)	MSL (3)	PACKAGE OPTION
RS1042	RS1042XK	-40°C ~125°C	SOP8	RS1042	MSL3	Tape and Reel, 4000

NOTE:

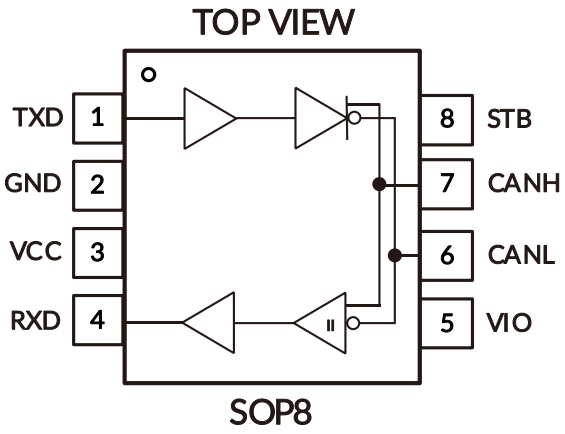
(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F, Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

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6 PIN CONFIGURATION AND FUNCTIONS



PIN DESCRIPTION

PIN	NAME	FUNCTION
SOP8		
1	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
2	GND	Ground
3	VCC	Power Supply
4	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
5	VIO	Logic I/O supply voltage
6	CANL	Low-level CAN bus line
7	CANH	High-level CAN bus line
8	STB	STB (standby mode) select pin (active high)

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7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

SYMBOL	PARAMETER		MIN	MAX	UNIT
VCC, VIO	Power Supply Voltage		-0.3	7	V
TXD, RXD, STB	Logic I/O Voltage		-0.3	7	V
V_{ID}	Differential input voltage		-27	27	V
V_{CANH}, V_{CANL}	Maximum BUS Pin Voltage		-70	70	V
θ_{JA}	Package thermal impedance (2)	SOP8		110	°C/W
T_{opr}	Operating Temperature		-40	125	°C
T_J	Junction Temperature (3)		-40	150	°C
T_{stg}	Storage Temperature		-40	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The package thermal impedance is calculated in accordance with JESD-51.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), ANSI/ESDA/JEDEC JS-001-2023	±8000	V
		Charged-Device Model (CDM), ANSI/ESDA/JEDEC JS-002-2022	±1500	



ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	MAX	UNIT
VCC	Power Supply Voltage	4.5	5.5	V
VIO		3	5.5	V
V_{ID}	Differential input voltage	-3	8	V
$I_{OH(CAN)}$	CAN bus terminal HIGH level output current	-50		mA
$I_{OL(CAN)}$	CAN bus terminal LOW level output current		50	mA
$I_{OH(RXD)}$	RXD terminal HIGH level output current	-2		mA
$I_{OL(RXD)}$	RXD terminal LOW level output current		2	mA

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7.4 Electrical Characteristics

(V_{CC}=4.5V~5.5V, V_{IO}=3V~5.5V, T_A=-40°C to 125°C. Unless otherwise noted, Typical values are at VCC=5V, VIO=3.3V, T_A = 25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNITS
Supply Voltage	V_{CC}		4.5		5.5	V
Undervoltage Detection Voltage on Pin VCC	$V_{uvd\ (VCC)}$		3.5		4.5	V
Supply Voltage on Pin VIO	V_{IO}		3		5.5	V
Undervoltage Detection Voltage on Pin VIO	$V_{uvd\ (VIO)}$		1.5		2.7	V
Supply Current	I_{CC}	Normal mode, dominant, TXD=0, STB=0, R_L=60Ω		48	70	mA
		Normal mode, recessive, TXD=V_{IO}, STB=0		1.6	5	mA
		Standby mode, STB=V_{IO}, TXD=V_{IO}		0.5	5	μA
Supply Current on Pin VIO	I_{IO}	Normal mode, dominant, V_{TXD}=0V		60	500	μA
		Normal mode, recessive, V_{TXD}=V_{IO}		30	100	μA
		Standby mode; V_{TXD}=V_{IO}		6.5	15	μA
Thermal-Shutdown Threshold	T_{TS}		135	150	165	°C
Logic Side						
High Level Input Voltage	V_{IH}	TXD &STB pin	0.7×V_{IO}			V
Low Level Input Voltage	V_{IL}	TXD &STB pin			0.3×V_{IO}	V
High Level Input Current	I_{IH}	TXD &STB pin	-5		5	μA
Low Level Input Current	I_{IL}	TXD pin	-50		-2	μA
		STB pin	-15		-1	μA
Output High Voltage	V_{OH}	RXD, IO=-2mA	0.8×V_{IO}			V
Output Low Voltage	V_{OL}	RXD, IO=2mA			0.2×V_{IO}	V
Input Capacitance	C_{IN}	TXD pin		10		pF
Driver						
CANH Output Voltage (Dominant)	$V_{OH(D)}$	STB=0, TXD=0V, R_{Load} =60Ω	2.8	3.6	4.5	V
CANL Output Voltage (Dominant)	$V_{OL(D)}$	STB=0, TXD=0V, R_{Load} =60Ω	0.5	1.33	2.25	V
CAN Bus Output Voltage (Recessive)	$V_{O(R)}$	TXD=V_{IO}; recessive; no load	2	0.5×VCC	3	V
		Standby mode, no load	-0.1		0.1	V
Differential Output Voltage (Dominant)	$V_{OD(D)}$	VCC=5V, TXD=0, R_{Load} =60Ω, see Figure 1	1.5		3	V
Differential Output Voltage (Recessive)	$V_{OD(R)}$	VCC=5V, TXD=VIO, R_{Load} =60Ω, see Figure 1	-0.05		0.05	V
		VCC=5V, TXD=V_{IO}, no Load, see Figure 1	-0.1		0.1	V
Short- Circuit Output Current	I_{OS}	Dominant, CANH=-30V, CANL open, see Figure 9	-150	-80		mA
		Recessive, CANH=30V, CANL open, see Figure 9		1.4	5	mA
		Recessive, CANL=-30V, CANH open, see Figure 9	-5	-1.7		mA
		Dominant, CANL=30V, CANH open, see Figure 9		95	150	mA
Receiver						
Positive-Going Bus Input Threshold Voltage	V_{IT+}	$V_{COM(CAN)}$=0V		700	900	mV

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Negative-Going Bus Input Threshold Voltage	V_{IT-}	$V_{COM(CAN)}$=0V	400	570		mV
Hysteresis Voltage	V_{HYS}			100		mV
Power-Off (Unpowered) Bus Input Leakage Current	$I_{IOFF(LKG)}$	V_{CANH} / V_{CANL}=5V, VCC=0V, VIO=0V	-5		5	μA
Input Capacitance to Ground	C_I	CANH or CANL		13		pF
Differential Input	C_{ID}			5		pF
Differential Input Resistance	R_{ID}		19		52	kΩ
Input Resistance	R_{IN}		9	20	35	kΩ
Input Resistance Matching	R_{Imatch}	CANH=CANL	-3		3	%
Common-Mode Voltage Range	V_{COM}		-30		30	V

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

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7.5 Switching Electrical Characteristics

(V_{CC}=4.5V~5.5V, V_{IO}=3V~5.5V, T_A=-40°C to 125°C. Unless otherwise noted, Typical values are at VCC=5V, VIO=3.3V, T_A = 25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNITS
Loop Delay1	T_{loop1}	Driver input to receiver output, Recessive to Dominant, see Figure 7		75	220	ns
Loop Delay2	T_{loop2}	Driver input to receiver output, Dominant to Recessive, see Figure 7		150	240	ns
Transmitted Recessive Bit Width	$t_{bit(bus)}$	$t_{bit(TXD)}$ = 500 ns	320		540	ns
		$t_{bit(TXD)}$ = 200 ns	50		200	ns
Bit Time on Pin RXD	$t_{bit(RXD)}$	$t_{bit(TXD)}$ = 500 ns	350		530	ns
		$t_{bit(TXD)}$ = 200 ns	60		220	ns
Driver						
Propagation Delay Time from TXD to Bus Dominant	t_{PLH}	Normal mode, see Figure 4		50		ns
Propagation Delay Time from TXD to Bus Recessive	t_{PHL}	Normal mode, see Figure 4		130		ns
Differential Output Signal Rise Time	t_r	see Figure 4		15		ns
Differential Output Signal Fall Time	t_f	see Figure 4		75		ns
Bus Dominant Time-Out Time	t_{TXD_DTO}	see Figure 8	800	2000	4000	µs
Receiver						
Propagation Delay Time from Bus Dominant to RXD	t_{PLH}	see Figure 6		40		ns
Propagation Delay Time from Bus Recessive to RXD	t_{PHL}	see Figure 6		25		ns
RXD Signal Rise Time	t_r	see Figure 6		15		ns
RXD Signal Fall Time	t_f	see Figure 6		10		ns
Receiver Dominant Time Out	t_{RXD_DTO}	Standby mode	800	1900	4000	µs
Bus Wake-Up Filter Time	$t_{fltr(wake)bus}$	Standby mode	0.5		5	µs
Standby to Normal Mode Delay Time	$t_{d(stb-norm)}$	standby to normal mode delay time	2		20	µs

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

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8 PARAMETER MEASUREMENT INFORMATION

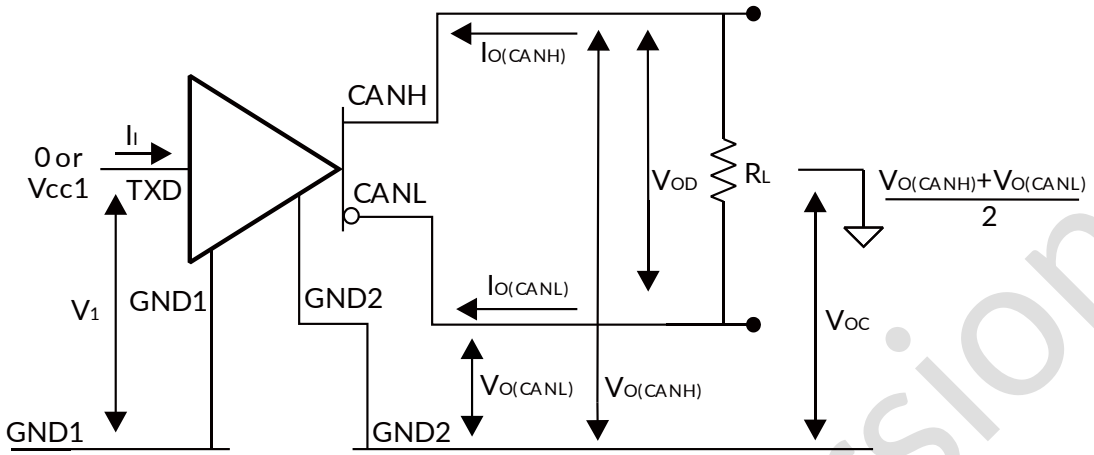


Figure 1. Driver Voltage, Current and Test Definitions

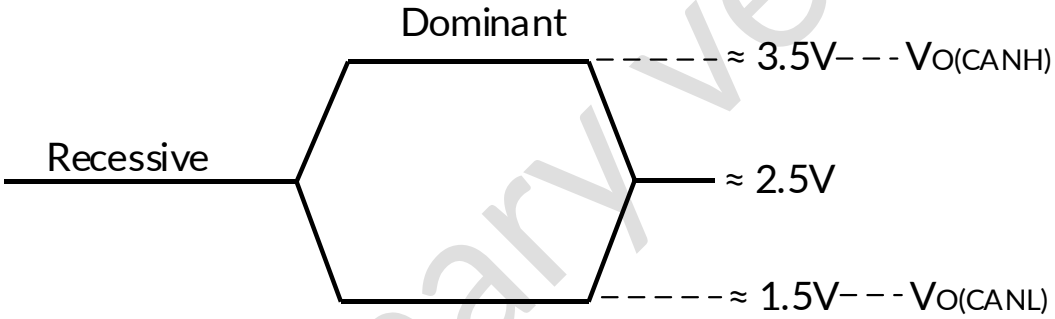


Figure 2. Bus Logic State Voltage Definitions

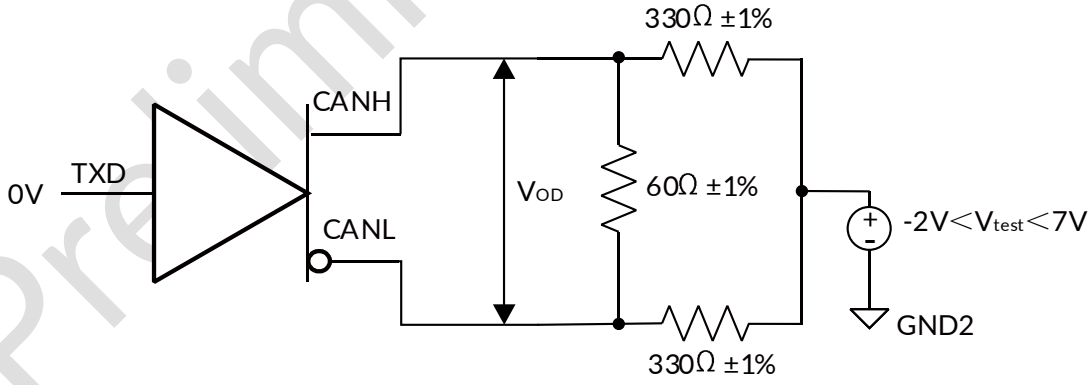
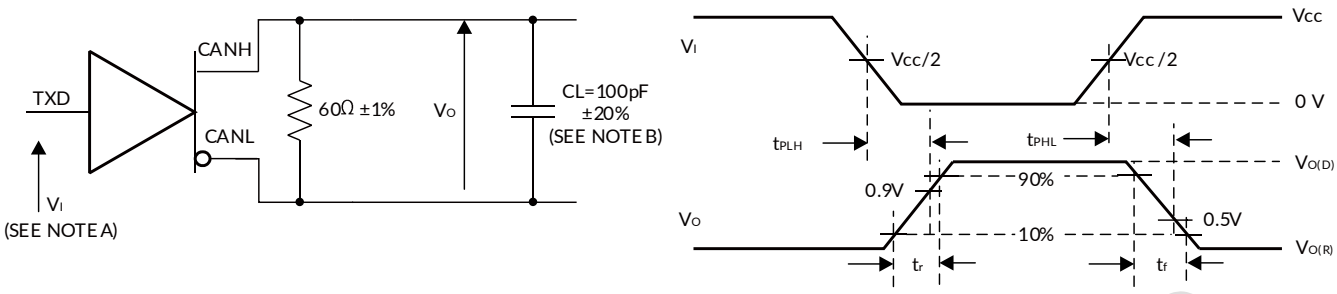


Figure 3. Driver V_{OD} With Common-Mode Loading Test Circuit

Preliminary version



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 4. Driver Test Circuit and Voltage Waveforms

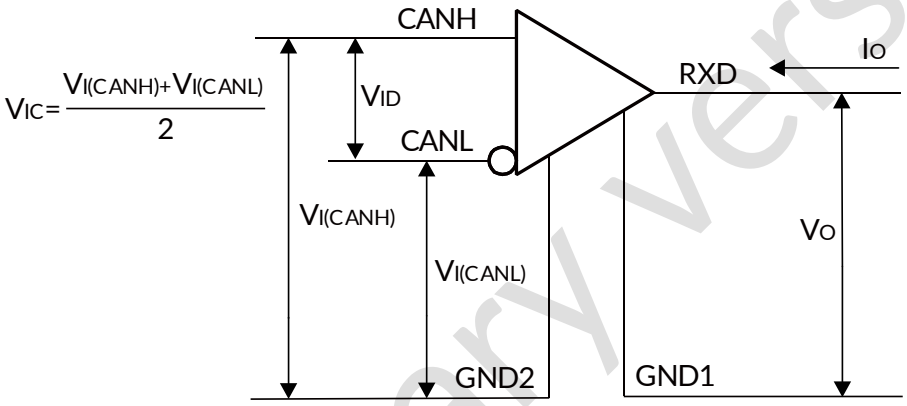
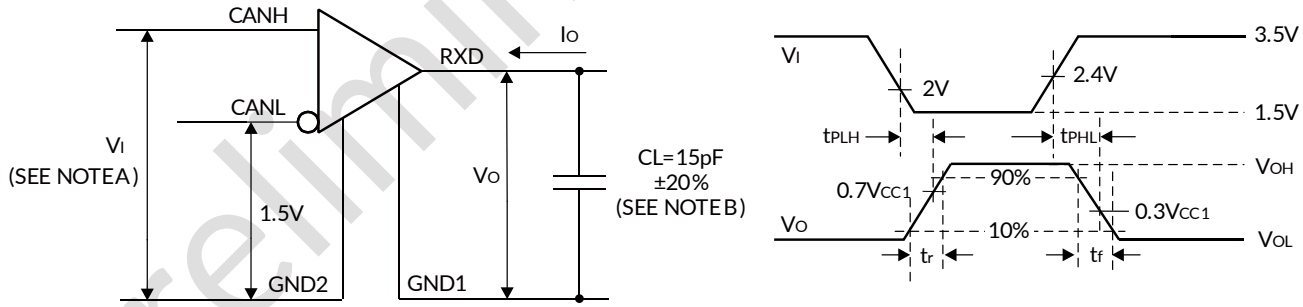


Figure 5. Receiver Voltage and Current Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 6. Receiver Test Circuit and Voltage Waveforms

Preliminary version

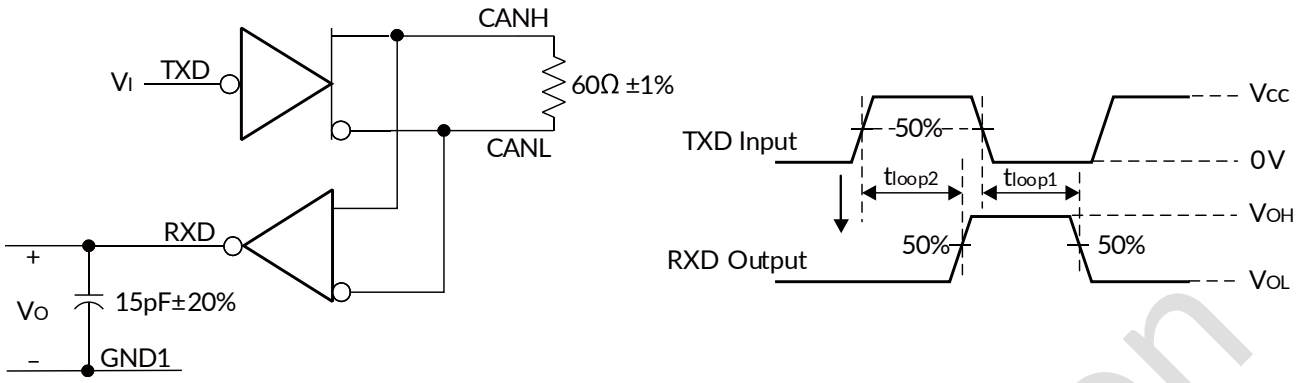
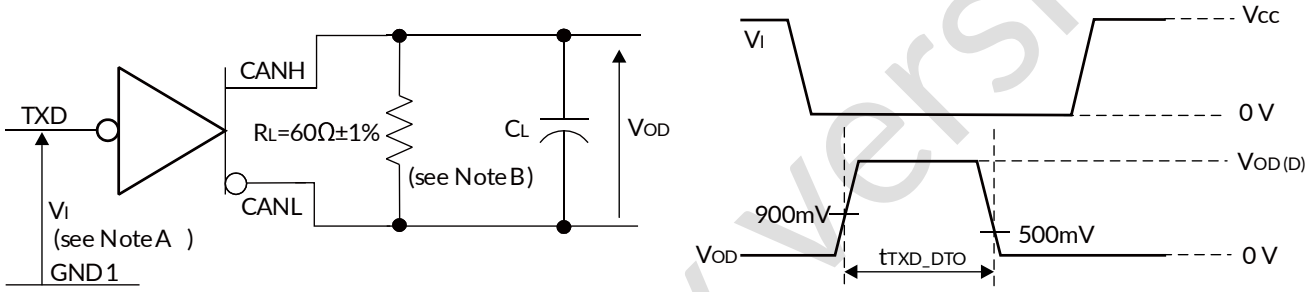


Figure 7. t_{LOOP} Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 8. Dominant Time-out Test Circuit and Voltage Waveforms

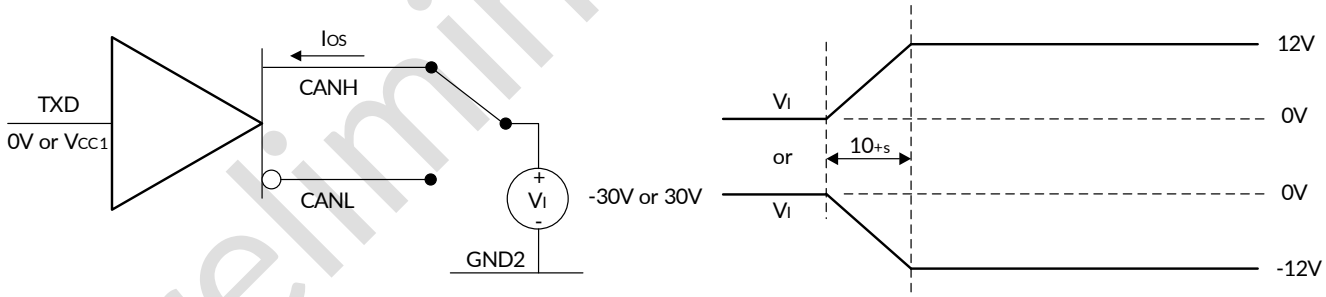


Figure 9. Driver Short-Circuit Current Test Circuit and Waveforms

Preliminary version

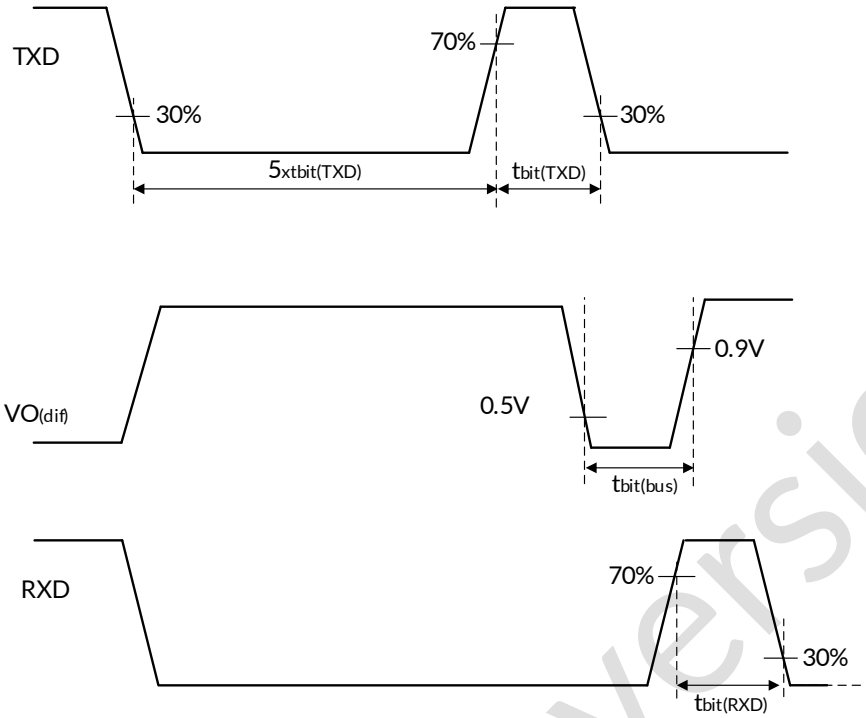


Figure 10. $t_{bit(RXD)}$ Test Circuit and Waveforms

Preliminary version

9 FUNCTION DESCRIPTION

9.1 Overview

The RS1042 is a CAN transceiver which fully compatible with the ISO11898-2 standard. The RS1042 is providing high electromagnetic immunity and low emissions. The data rate of the RS1042 is up to 5Mbps. The RS1042 provides thermal protection and transmit data dominant time out function.

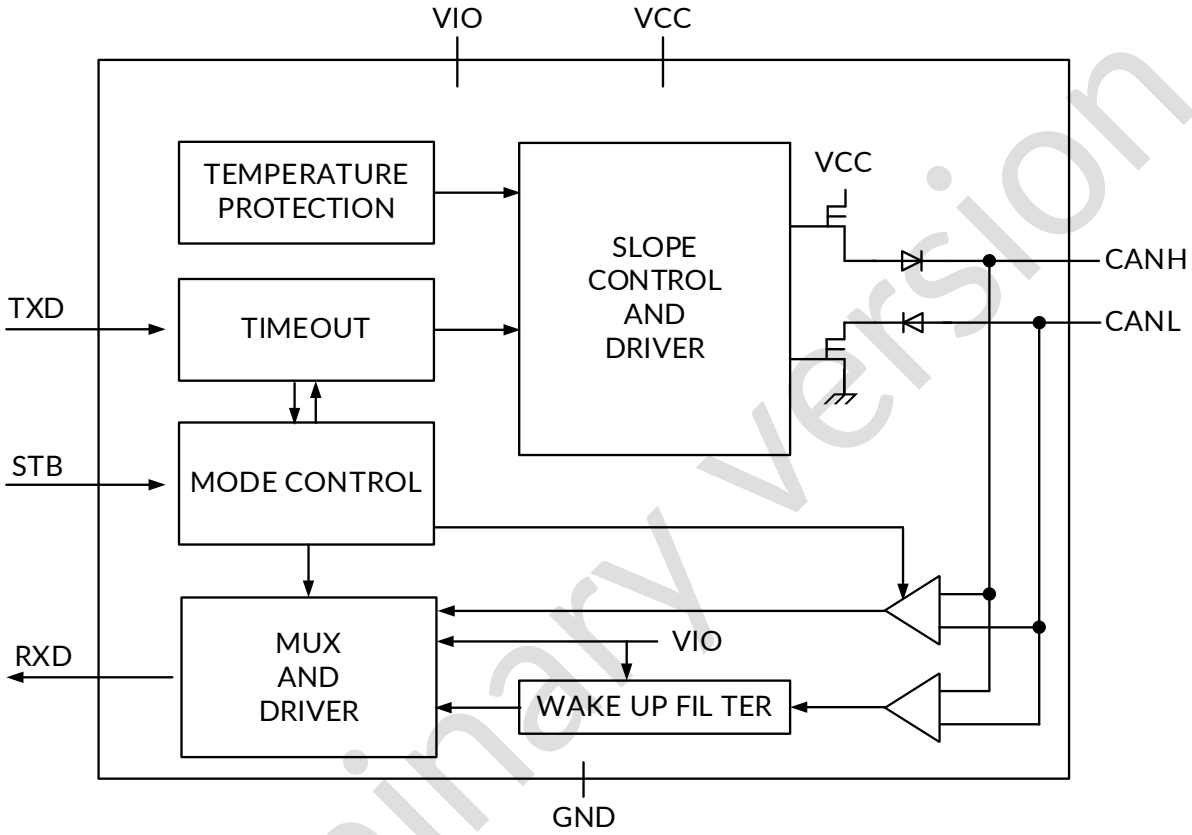


Figure 11. Block diagram of RS1042

9.2 Device Functional Modes

Table 1. Driver Function Table

TXD	CANH	CANL	BUS STATE
L (1)	H (1)	L (1)	Dominant
H (1)	Z (1)	Z (1)	Recessive
Open	Z (1)	Z (1)	Recessive

(1) H=high level; L=low level; Z=common mode(recessive) bias to $V_{CC}/2$.

Table 2. Receiver Function Table

V_{ID}=CANH-CAHL	RXD	BUS STATE
V_{ID} ≥0.9V	L (2)	Dominant
0.5< V_{ID} <0.9V	X (2)	Uncertain
V_{ID} ≤0.5V	H (2)	Recessive
Open	H (2)	Recessive

(2) H=high level; L=low level; X=uncertain.

Preliminary version

9.3 Normal mode

A LOW level on pin STB selects Normal mode. In this mode, the transceiver can transmit and receive data via the bus lines CANH and CANL (see Figure 11 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME.

9.4 Standby mode

A HIGH level on pin STB selects Standby mode. In Standby mode, the transceiver is not able to transmit or correctly receive data via the bus lines. The transmitter and Normal-mode receiver blocks are switched off to reduce supply current, and only a low power differential receiver monitors the bus lines for activity. The wake-up filter on the output of the low-power receiver does not latch bus dominant states, but ensures that only bus dominant and bus recessive states that persist longer than $t_{filtr(wake)}$ bus are reflected on pin RXD. In Standby mode, the bus lines are biased to ground to minimize the system supply current. The low-power receiver is supplied by VIO, and is capable of detecting CAN bus activity even if VIO is the only supply voltage available. When pin RXD goes LOW to signal a wake-up request, a transition to Normal mode will not be triggered until STB is forced LOW.

9.5 TXD dominant time-out function

A 'TXD dominant time-out' timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD.
If the duration of the LOW level on pin TXD exceeds the internal timer value (t_{TXD_DTO}), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD. The TXD dominant time-out time also defines the minimum possible bit rate of 10 kbit/s.

9.6 RXD dominant time-out function

In Standby mode a 'bus dominant time-out' timer is started when the CAN bus changes from recessive to dominant state. If the dominant state on the bus persists for longer than t_{RXD_RTO}, the RXD pin is reset to HIGH. This function prevents a clamped dominant bus (due to a bus short-circuit or a failure in one of the other nodes on the network) from generating a permanent wake-up request. The bus dominant time-out timer is reset when the CAN bus changes from dominant to recessive state.

9.7 Current Protection

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

9.8 Over Temperature Protection

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature T_{TS}, the output drivers will be disabled until the virtual junction temperature becomes lower than T_{TS} and TXD becomes recessive again.
By including the TXD condition, the occurrence of output driver oscillation due to temperature drifts is avoided.

9.9 VIO Output Supply

Pin VIO should be connected to the microcontroller supply voltage (see Figure 12). This will adjust the signal levels of pins TXD, RXD and STB to the I/O levels of the microcontroller. This sets the signal levels of pins TXD, RXD and STB to levels compatible with 3.3 V microcontrollers.

Preliminary version

10 APPLICATION NOTE

10.1 Typical Application

The RS1042 requires a 0.1μF bypass capacitors between VCC and GND. The capacitor should be placed as close as possible to the package. The figure 12 is the basic schematic of RS1042.

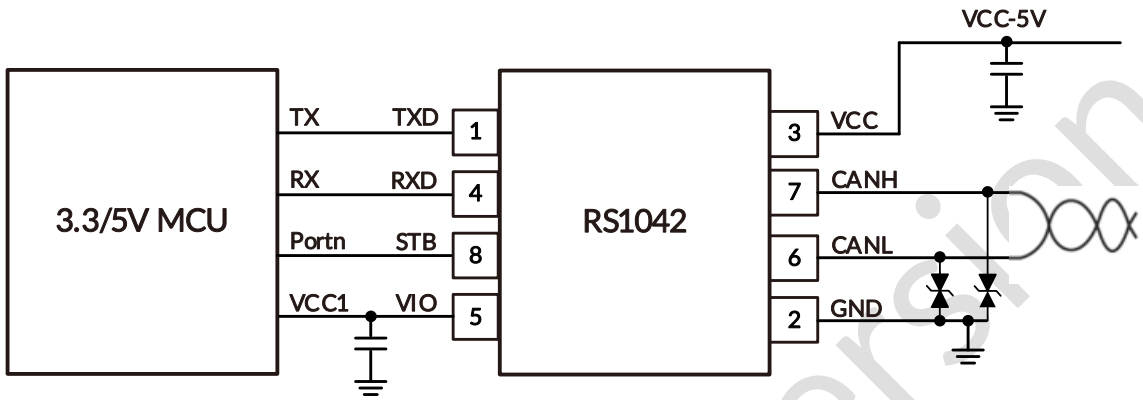
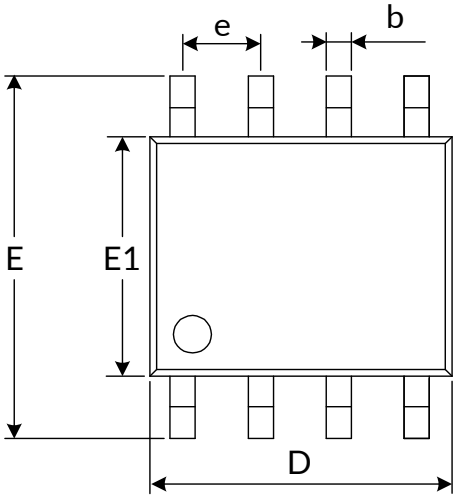


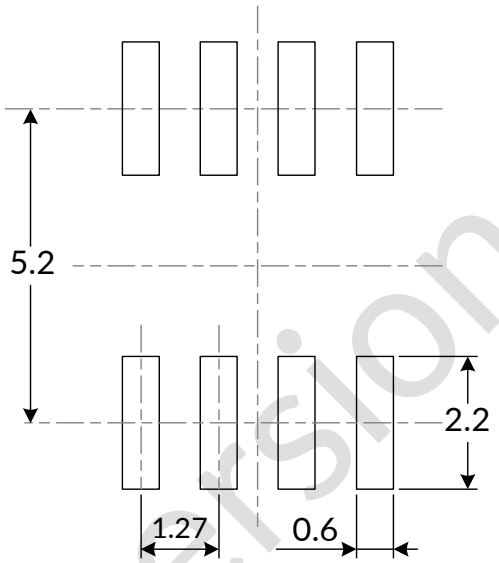
Figure 12. Basic schematic of RS1042

Preliminary version

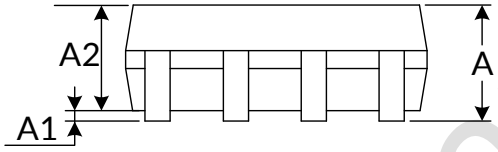
11 PACKAGE OUTLINE DIMENSIONS

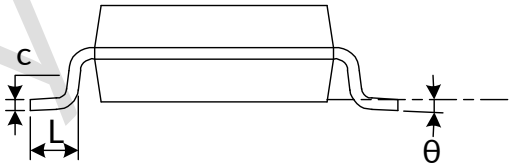
SOP8 (3)





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D (1)	4.800	5.000	0.189	0.197
e	1.270(BSC) (2)		0.050(BSC) (2)	
E	5.800	6.200	0.228	0.244
E1 (1)	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTE:

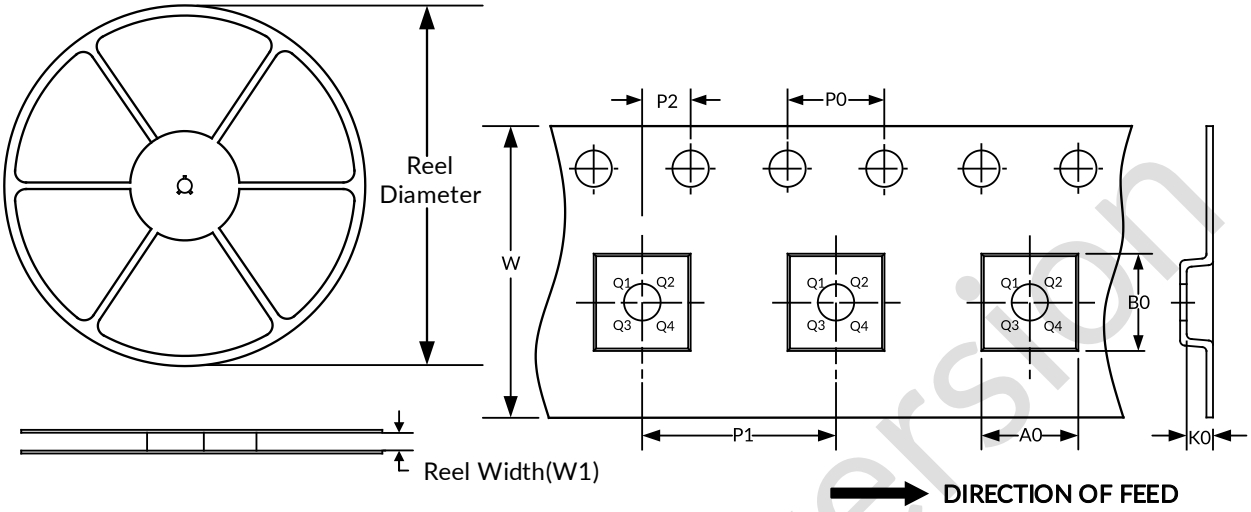
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

Preliminary version

12 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOP8	13”	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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